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Информация о владельце:
ФИО: Порохня Андрей Алексеевич
Должность: И.о. директора института перспективной инженерии
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MINISTRY OF SCIENCE AND HIGHER EDUCATION OF THE RUSSIAN FEDERATION
Federal State Autonomous Educational Institution
Higher Education
"NORTH CAUCASUS FEDERAL UNIVERSITY"

APPROVED BY
Acting Director of the Institute
Advanced Engineering
Cand. Tech. Sci., Associate Professor
A.A. Porokhnya

DISCIPLINE ASSESSMENT TOOLS FUND
Analog Electronic Technology

Field of study	11.03.02 Infocommunication Technologies and Communication Systems
Profile	Intelligent Data Processing in Infocommunication Systems and Networks
Year of start of training	2026
Form of study	Full-time
Implemented in a semester	3

Introduction

1. Purpose

The fund of assessment tools in the discipline "Analog Electronic Technology" is intended for an objective assessment of the level of competence formation.

2. FOS is an appendix to the program of the discipline "Analog Electronic Technology".

3. Developer V.I. Nikulin, Associate Professor of the Department of Digital, Robotic Systems and Electronics of the Institute of Advanced Engineering.

4. An examination of the FOC was carried out.

Members of the expert group:

Chairman: V.P. Mochalov, Professor of the Department of Digital, Robotic Systems and Electronics of the Institute of Advanced Engineering.

Members of the Commission:

S.V. Yakovlev, Associate Professor of the Department of Digital, Robotic Systems and Electronics of the Institute of Advanced Engineering.

S.V. Melnikov, Senior Researcher of the Interdisciplinary Training and Research Center for Agricultural Technologies, Associate Professor of the Department of Digital, Robotic Systems and Electronics of the Institute of Advanced Engineering.

Representative of the employer's organization:

Mironov V.A., General Director of Orintex LLC.

Expert opinion: The FAT for the discipline allows you to assess the level of competence formation. Start approbation.

5. The validity period of the FAT is determined by the period of implementation of the educational program.

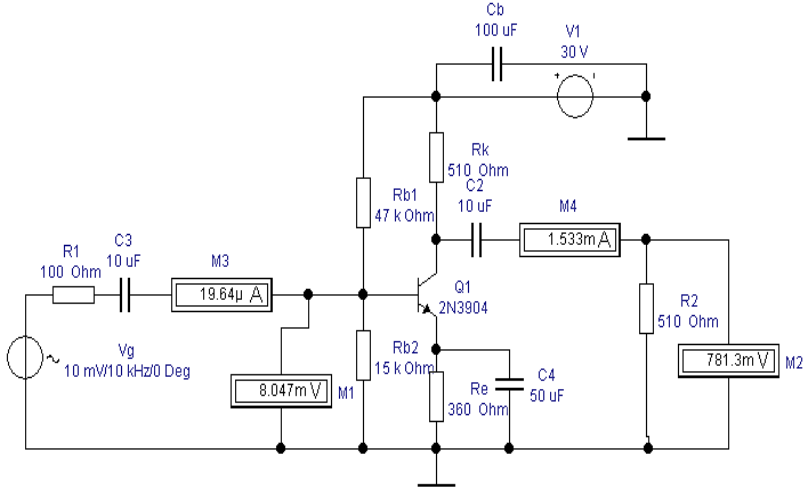
1. Description of indicators and assessment criteria at various stages of their formation, description of assessment scales

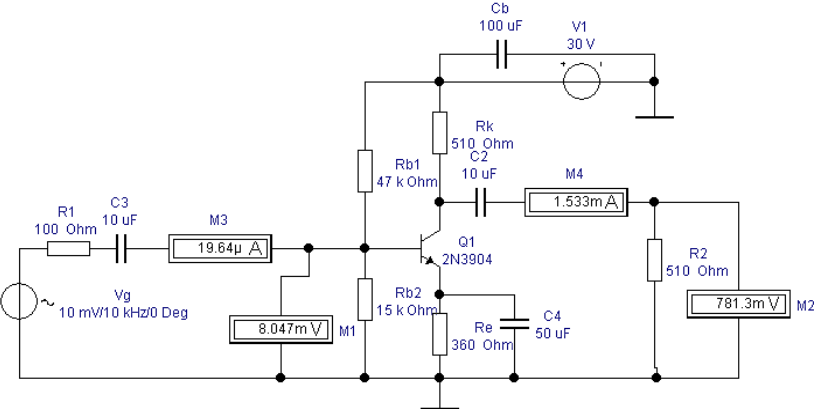
Levels of competence and indicators	Descriptors			
	The minimum level has not been reached (Unsatisfactory) 2 points	Minimum level (satisfactory) 3 points	Intermediate level (good) 4 points	High level (excellent) 5 points
Competency: OPK-1				
ID-1 OPK-1 understands the fundamental laws of nature and the basic physical mathematical laws and methods of accumulating, transmitting and processing information.	Unable to complete tasks related to this competency achievement indicator	Performs tasks at the reproductive level related to this indicator of competence achievement	Performs tasks related to this indicator of competence achievement in standard situations, making minor mistakes	Fully performs tasks related to this indicator of competence achievement, including in non-standard situations
ID-2 OPK-1 applies physical laws and mathematical methods to solve problems of a theoretical and applied nature.	Unable to complete tasks related to this competency achievement indicator	Performs tasks at the reproductive level related to this indicator of competence achievement	Performs tasks related to this indicator of competence achievement in standard situations, making minor mistakes	Fully performs tasks related to this indicator of competence achievement, including in non-standard situations
ID-3 OPK-1 uses the knowledge of physics and mathematics to solve practical problems.	Unable to complete tasks related to this competency achievement indicator	Performs tasks at the reproductive level related to this indicator of competence achievement	Performs tasks related to this indicator of competence achievement in standard situations, making minor mistakes	Fully performs tasks related to this indicator of competence achievement, including in non-standard situations
Competency: OPK-2				
ID-3 OPK-2 understands the basic methods and means of conducting experimental research, standardization and certification systems.	Unable to complete tasks related to this competency achievement indicator	Performs tasks at the reproductive level related to this indicator of competence achievement	Performs tasks related to this indicator of competence achievement in standard situations, making minor mistakes	Fully performs tasks related to this indicator of competence achievement, including in non-standard situations
ID-4 OPK-2 selects methods and means of measurement and conducts	Unable to complete tasks related to this competency	Performs tasks at the reproductive level related to this indicator of	Performs tasks related to this indicator of competence achievement in	Fully performs tasks related to this indicator of competence achievement,

experimental research.	achievement indicator	competence achievement	standard situations, making minor mistakes	including in non-standard situations
ID-5 OPK-2 is proficient in the methods of processing and presenting the data obtained and assessing the error of measurement results.	Unable to complete tasks related to this competency achievement indicator	Performs tasks at the reproductive level related to this indicator of competence achievement	Performs tasks related to this indicator of competence achievement in standard situations, making minor mistakes	Fully performs tasks related to this indicator of competence achievement, including in non-standard situations

Assessment of the level of competence in the discipline is carried out on the basis of the "Regulation on the current monitoring of progress and intermediate certification of students in educational programs of higher education - bachelor's programs, specialist programs, master's programs - in the Federal State Autonomous Educational Institution of Higher Education "North Caucasus Federal University" in the current edition.

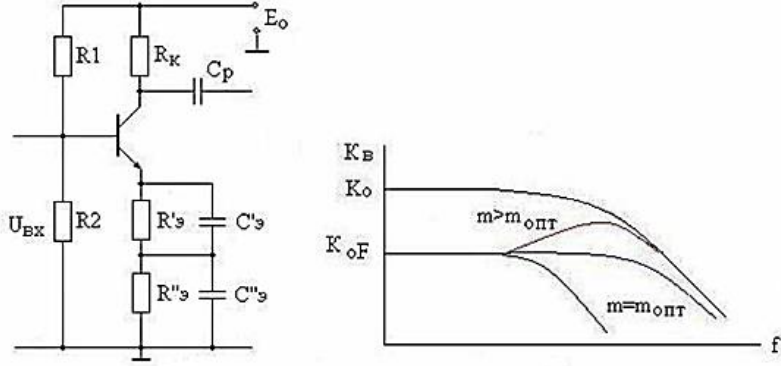
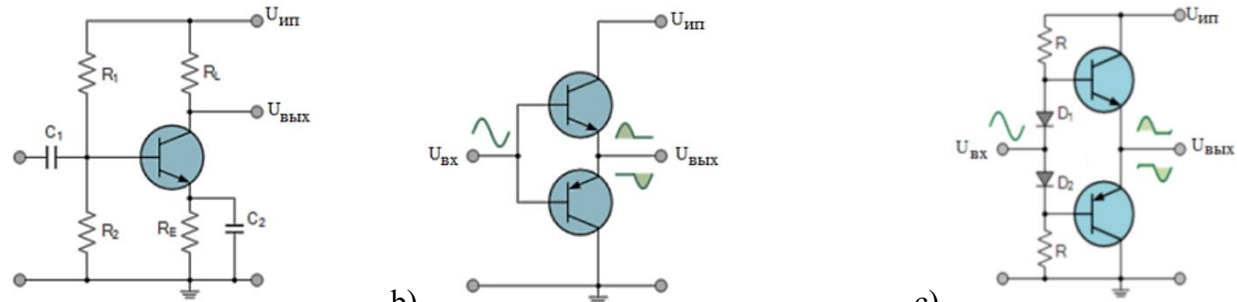
ASSESSMENT TOOLS TO CHECK THE LEVEL OF FORMATION OF COMPETENCIES

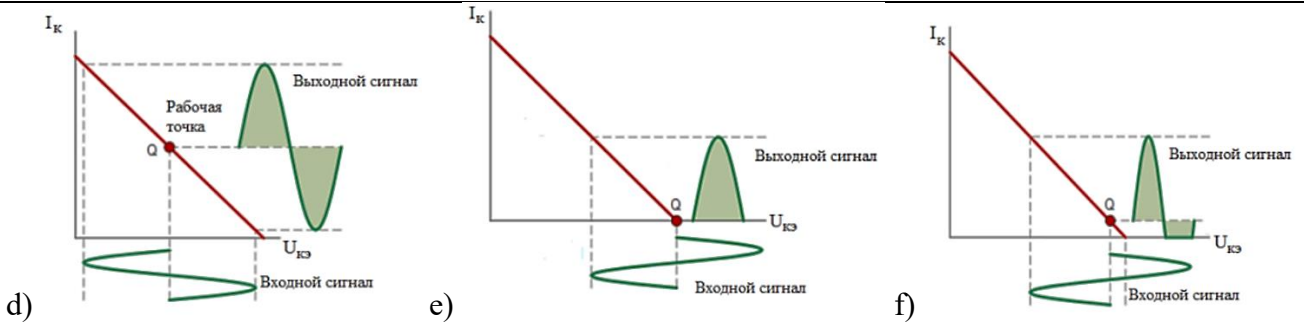
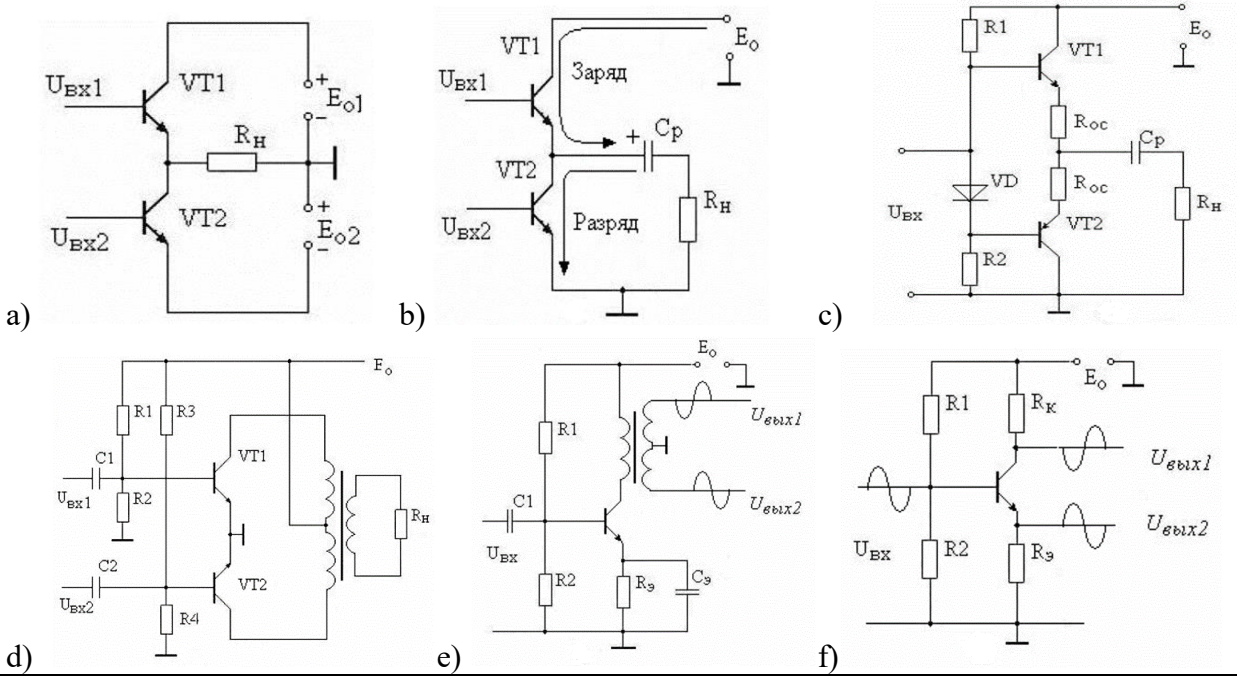
Job Number	Correct answer	Content of the question	Competence
Semester 5.			
1.	a)	The input impedance of the amplifier shown in the figure is  a) 410 ohms (b) 11.4 kΩ c) 510 ohms (d) 470 Ω	PC-3
2.	d)	The output impedance of the amplifier shown in the figure, assuming that the voltmeter M2 shows 1.5 V in the idle mode, is	PC-3

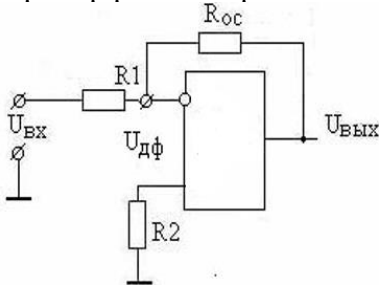
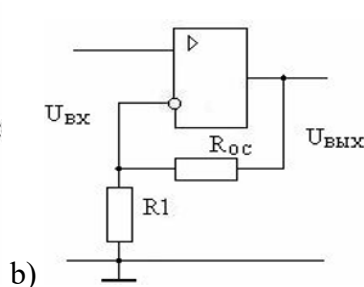
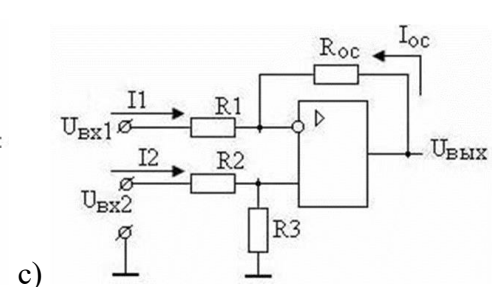
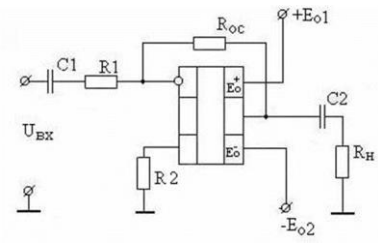
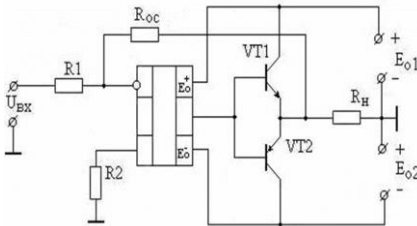
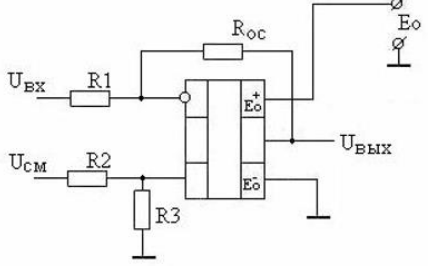
		 a) 410 ohms (b) 11.4 kΩ c) 510 ohms (d) 470 Ω	
3.	a)	The depth of feedback of the amplifier is calculated according to the formula: a) $F_{oc} = 1 + \beta K$ b) $F_{oc} = 1 - (\pm \beta K)$ c) $F_{oc} = \frac{1}{K_{oc}} - \beta$ d) $F_{oc} = \frac{K}{1 - (\pm \beta K)}$	PC-3
4.	1 – a 2 – b 3 – c 4 – d 5 – e	Establish a correspondence between the amplifier indicator and the formula for its calculation: 1) Harmonic distortion coefficient 2) Power Output 3) Efficiency 4) Dynamic Range 5) Frequency distortion coefficient $\frac{\sqrt{U_2^2 + U_3^2 + \dots + U_n^2}}{U_1}$ a) $\frac{U_{m \text{ Вых}} I_{m \text{ Вых}}}{2}$ b) $\frac{U_{m \text{ Вых}} I_{m \text{ Вых}}}{2 U_0 I_0}$ c) $\frac{U_{m \text{ Вых}} I_{m \text{ Вых}}}{2 U_0 I_0}$	PC-3

		$20 \lg \frac{U_{\text{ВХ МАКС}}}{U_{\text{ВХ МИН}}}$ d) $\frac{K_{cp}}{K_f}$	
5.	1 – a 2 – b 3 – c 4 – d 5 – e	Establish a correspondence between the parameters of the input and output circuits in the middle frequencies for the amplifier according to the OE circuit and the calculation formulas: 1) Input impedance 2) Input Circuit Transfer Ratio 3) Input Voltage 4) Nominal Gain 5) Output resistance in idle mode a) $\frac{R_{\theta} \cdot h_{11}}{R_{\theta} + h_{11}}$ $\frac{R_{ex}}{R_z + R_{ex}}$ b) $\frac{R_z + R_{ex}}{E_T \cdot K_{BX}}$ c) $E_T \cdot K_{BX}$ $S \cdot \frac{R_x \cdot R_n}{R_x + R_n}$ d) $\frac{R_K \cdot h_{22}}{R_K + h_{22}}$ e)	PC-3
6.		Determine the voltage gain of the first stage stage of a three-stage amplifier (in decibels and times) if the total gain is 80 dB, and the gain of the second stage is 6 dB more than the gain of the third stage, which is equal to 10 relative units (times).	PC-3
7.		Using the values of the measuring instruments in the diagram above, determine the gain factors for voltage, current, power and through-gain.	PC-3

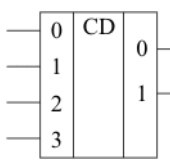
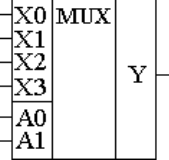
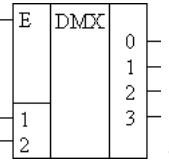
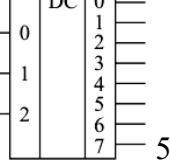
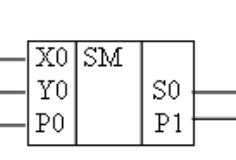
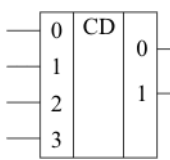
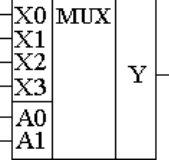
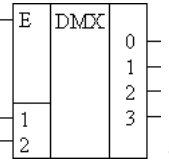
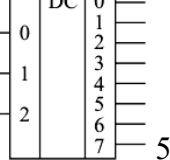
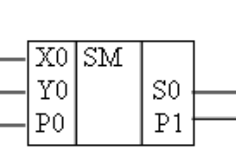
8.		Determine the gain of the op-amp shown in the figure, calculate the depth of negative feedback and the width of the gain bandwidth, provided that with broken feedback, the frequency response meter showed the following parameters: gain - 106 dB, upper cutoff frequency - 50 Hz.	PC-3
9.		Compare amplifier stages with different bipolar transistor switching circuits, while revealing their advantages and disadvantages, and indicating the field of application.	PC-3
10.		Perform a theoretical calculation of the main parameters of the amplifier stage according to the scheme with a common emitter.	PC-3
11.		Perform a theoretical calculation of the main parameters of the amplifier stage according to the scheme with a common collector.	PC-3
12.		Perform a theoretical calculation of the main parameters of the amplifier stage according to the scheme with a common base.	PC-3

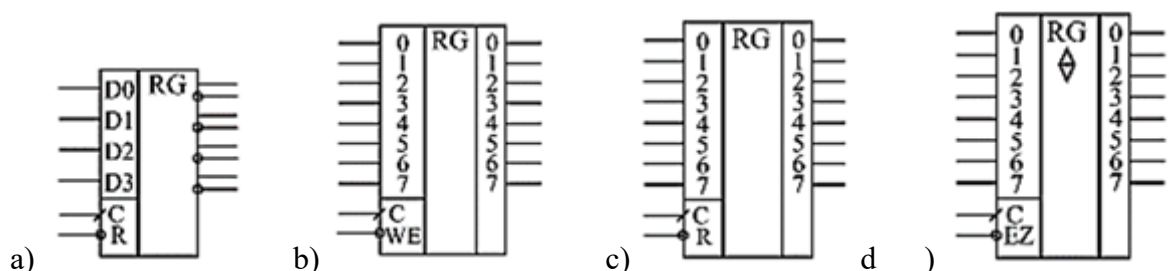
13.		Perform a theoretical calculation of the main parameters of an active second-order RC low-pass filter, convert the parameters into a high-pass filter.	PC-3
14.	a)	The diagram and graph shown in the figure describe the principles of construction and operation  a) amplifying stage according to the OE scheme with a high-frequency correction circuit of the Z-type environmental protection (b) Dynamic load OE amplification stage c) Amplification stage according to the OE scheme with a Z-type mid-frequency correction circuit (d) Load-matched AC amplification stage e) Amplification stage according to the OE circuit with a high-frequency correction circuit of the Y-type	PP-4
15.	a, d	Select drawings that are relevant to the design and operation of a Class A amplifier  a) b) c)	PP-4

		 d) e) f)	
16.	1 – a 2 – b 3 – c 4 – d	Establish a correspondence between the name of the diagram and its image: 1) Push-pull circuit of transformerless amplification power stage with two power supplies 2) Push-pull circuit of transformerless amplifying power stage with separating capacitor 3) Push-pull circuit of transformerless amplifier power stage on complementary transistors 4) Push-pull circuit of transformer amplifying power stage  a) b) c) d) e) f)	PP-4
17.	1 – a 2 – b	Establish a correspondence between the name of the diagram and its image: 1) Inverting operation of the op-amp	PP-4

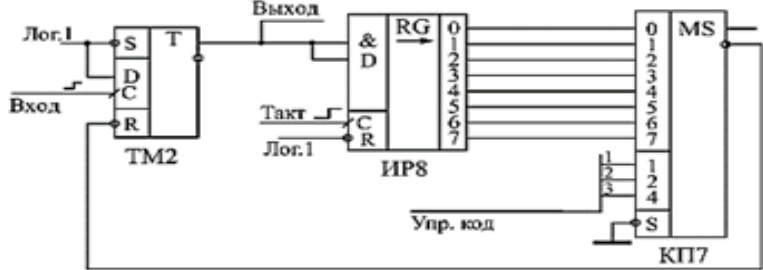
	3 – c 4 – d 5 – e 6 – f	2) Non-inverting operation of the op-amp 3) Op-Amp Differential Engagement 4) AC amplifier on op-amp 5) AC amplifier on op-amp with operating point offset 6) Op-amp power amplifier a)  b)  c)  d)  e)  f) 	
18.	1 – a 2 – b 3 – c 4 – d 5 – e 6 – f	Establish a correspondence between the name of the diagram and its image: 1) Op-amp adder 2) Op-Amp Subtractor 3) Op-amp differentiator 4) Op-Amp Integrator 5) Op-amp Comparator 6) Op-Amp Compressor	PP-4

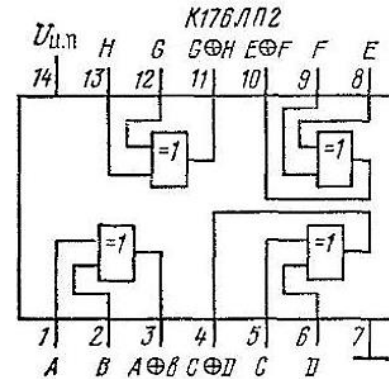
		a) Inverting amplifier with multiple inputs. b) Non-inverting amplifier. c) Integrator. d) Differentiator. e) Active second-order RC low-pass filter. f) Active second-order RC bandpass filter.	
19.		Assemble a schematic diagram of a non-inverting amplifier on an op-amp in a computer simulation software package, check its performance and set it up.	PP-4
20.		Assemble the schematic diagram of the adder (subtractor) on the op-amp in a computer simulation software package, check their operability and settings.	PP-4
21.		Assemble a circuit diagram of the differentiator (integrator) on the op-amp in a computer simulation software package, check its performance and adjust.	PP-4
22.		Assemble a schematic diagram of an active second-order RC low-pass filter in a computer simulation software package, check its performance and set it up.	PP-4
23.		To assemble in the computer simulation software package the schematic diagram of the autogenerator at the Op Object with the Wien's bridge, to check its operability and adjust.	PP-4
24.		Assemble the schematic diagram of the comparator on the op-amp in the computer simulation software package, check its operability and set it up.	PP-4
25.		Assemble a schematic diagram of a second-order RC bandpass active filter in a computer simulation software package, check its performance and set it up.	PP-4
Semester 6.			
26.	1 – a	Establish a correspondence between a digital logic device and its DSD:	PC-3

	2 – b 3 – c 4 – d 5 – e	     1)  2)  3)  4)  5)  a) 4x2 encoder b) 4x1 multiplexer c) 1x4 demultiplexer d) 3x8 decoder (e) Complete single-digit adder	
27.	1 – a 2 – b 3 – c 4 – d 5 – e	Establish a correspondence between a digital logic device and the minimum number of logic gates required to synthesize that device: 1) Single Digit Full Adder 2) 3x8 decoder 3) Dual Channel Multiplexer 4) Dual Channel Demultiplexer 5) 4x2 encoder a) 2 elements of EXCLUSIVE OR, 2 elements of AND and 1 element of OR b) 3 inverters and 16 I cells for 2 inputs c) 1 inverter, 2 AND cells for 2 inputs, 1 element OR for 2 inputs d) 1 inverter, 2 I cells for 2 inputs e) 4 inverters, 3 AND cells with 4 inputs and 2 OR cells	PC-3
28.	c)	Trigger when there are no input signals... a) is reset to 0 b) changes its status on the SI front (c) Retains its previous state (d) Set at 1	PC-3
29.	d)	The complete basis of logical operations, from which it is possible to obtain an arbitrarily complex logical expression and, consequently, a device, are a) AND, OR, NOT (b) Y-NOT (c) OR NOT (d) All of the above	PC-3
30.	1 – a 2 – b	Match the chip to the register description with its UGO 1) TM8 (4-bit data storage register containing 4 synchronous D-triggers)	PC-3

	3 – c 4 – d	2) IR27 (8-bit pulse-clocked data storage register) 3) IR35 (eight-bit edge-controlled register with parallel data input/output, with reset input) 4) IR37 (eight-bit register of information storage, clocked by pulse, with the ability to transfer outputs to a high-impedance state) 	
31.		Submit a proposal for the technical implementation of a single-digit four-channel multiplexer based on a decoder and logic gates.	PC-3
32.		Simulate the counter modulo 5 based on JK triggers and test its operation in the Multisim interactive emulator or in the Electronics Workbench schematic modeling package	PC-3
33.		Simulate a frequency divider by 8 based on JK triggers and test its operation in the interactive Multisim emulator or in the Electronics Workbench schematic modeling package	PC-3
34.		Justify the choice of the necessary microcircuits (element base) for the construction of the accumulating adder from the provided list of microcircuits: K555AP6, K555YV2, K555ID6, K555IE17, K555IM6, K555IR9, C555IR35, K555KP17, K555LR13, C555TM8	PC-3
35.		Simulate a time interval generator based on 2 four-digit counters in the Multisim interactive emulator or in the Electronics Workbench schematic modeling package.	PC-3
36.		To develop a circuit for an input signal duration meter based on synchronous counters with asynchronous transfer and a time diagram explaining its operation.	PC-3
37.		To develop a circuit for a direct input frequency meter based on synchronous counters with asynchronous transfer and a time diagram explaining its operation.	PC-3
38.	1 – a 2 – b 3 – c 4 – d	Establish a match: 1) Decoder 2) Encoder 3) Multiplexer 4) Code converter (a) Converts an n-bit binary code into 2^n an -bit unitary code containing only one logical unit or zero (b) Converts an n-bit unitary code containing only one logical unit or zero, $\lceil \log_2 n \rceil$ a -bit binary code	PP-4

		c) switches signals from its n inputs to the output of the device, the numbers of which are determined by $\lceil \log_2 n \rceil$ by the $\lceil \log_2 n \rceil$-bit address (selector) code (d) Compares two N-bit input codes and signals to the device outputs about the results of the equality or inequality of the codes e) switches the signal from the input of the device to one of its n outputs, the numbers of which are determined by $\lceil \log_2 n \rceil$ a $\lceil \log_2 n \rceil$-bit address (selector) code	
39.	1 – a 2 – b 3 – c 4 – d	Establish a match: 1) Trigger 2) Register 3) Counter 4) Read-only memory (a) A serial device with two steady states designed to record and store one bit of binary information (b) A serial or parallel device used to store n-bit binary numbers and perform transformations on them (c) A serial device whose outputs produce a binary code determined by the number of pulses received and the counting module (d) A device with random access to memory cells that are capable of storing binary data in the absence of electrical power (e) A device that stores a single bit of binary information and requires periodic rewriting to store the data	PP-4
40.	c	The figure shows the scheme a) a four-bit asynchronous binary counter b) a four-digit synchronous binary counter with asynchronous transfer (c) A four-digit synchronous binary counter (d) A four-digit right-shift register (e) A four-digit left-shift register (f) A four-digit binary counter with a variable counting module	PP-4

41.	a)	The figure shows the diagram ...  (a) Pulse conditioner with duration specified by the control code (b) A pseudo-random sequence generator (c) The Manchester Code Encoder (d) Communication communication devices (e) Controlled frequency divider on register and multiplexer (f) A time interval generator for the transmission of a controlled burst of pulses	PP-4
42.	1 – a 2 – b 3 – c	Match the title of the project document to its characteristics 1) A document that defines the complete composition of the elements and the relationships between them, giving a complete (detailed) idea of the principles of operation of the device 2) A document that reveals in detail the main (complex) components of the device, but explains the logic of the operation of the entire device as a whole 3) A document defining the main components of the device, their purpose and interconnections (a) Electrical circuit diagram (b) Functional electrical diagram (c) Electrical structural diagram (d) Electrical wiring diagram	PP-4
43.		Draw up and explain the operation of the LED indication control circuit on a logical inverter. Calculate the value of resistance limiting the current through the LED, provided that the value of the current consumption of the LED should be at least 10 mA, but not more than 100 mA, and the voltage drop on the LED is 1 V.	PP-4
44.		To present the schematic diagram of the parity control device for a 5-digit code based on the K176LP2 chip, the passport data of which are given in the figure	PP-4



45.		Use a time diagram to explain how a controlled inverter works on the "Exclusive OR" logic element	PP-4
46.		Present a graphical symbol, transition table, and time diagrams of a synchronous single-stage D trigger with dynamic write control and asynchronous preset inputs	PP-4
47.		Principles of construction and operation of an accumulator adder. To present the scheme of a 4-digit adder and time diagrams of its operation.	PP-4
48.		Synthesize the scheme of a four-bit shift register on D triggers, explain its logic of operation using a time diagram	PP-4
49.		To develop a scheme for the transmission of digital binary information in a serial code along two lines: information and synchronizing. To explain the procedure for its operation.	PP-4
50.		Develop a scheme for determining the extremal value of the input code on registers and digital comparators. Explain the procedure for its operation.	PP-4

Description of the grading scale

Within the framework of the rating system, the performance of students in each discipline is assessed during current control and intermediate certification. The rating system for assessing students' knowledge is based on the use of a set of control measures to check the material covered (control points), optimally located throughout the time interval of studying the discipline. The principles of the rating system for assessing students' knowledge are based on the requirements described in the Regulation on the organization of the educational process based on the rating system for assessing students' knowledge at NCFU.

Criteria for assessing competencies

An "excellent" grade is given to a student if he/she fully and accurately performs the tasks of assessment tools in the discipline related to this competence (indicators of competence achievement), while demonstrating at a high level the ability to solve standard and non-standard applied practical problems of circuitry of telecommunication devices.

A grade of "good" is given to a student if he/she, making minor mistakes, performs the tasks of assessment tools in the discipline related to this competence (indicators of competence achievement), while demonstrating at an average level the ability to solve only standard applied practical problems of circuitry of telecommunication devices.

A "satisfactory" grade is given to a student if he/she performs the tasks of assessment tools in the discipline related to this competence (indicators of competence achievement), while demonstrating at a minimum level the ability to solve standard applied practical problems of circuitry of telecommunication devices.

An "unsatisfactory" grade is given to a student if he/she, performing the tasks of assessment tools in the discipline, does not reach the minimum level of competence formation ((indicators of competence achievement), while not demonstrating the ability to solve standard applied practical problems of circuitry of telecommunication devices, makes gross mistakes that he cannot correct even with the help of leading questions from the teacher.