MINISTRY SCIENCES AND HIGHER EDUCATION RUSSIAN FEDERATION FEDERAL STATE AUTONOMOUS EDUCATIONAL INSTITUTION OF HIGHER EDUCATION "NORTH CAUCASIAN FEDERAL UNIVERSITY"

METHODOLOGICAL INSTRUCTIONS

By completion of Practical Classes

By discipline

Analog Electronic Technology

for students in the field of study

11.03.02 Infocommunication technologies And systems connections

Stavropol 2026

CONTENT

1 Study parameters And characteristics amplifying devices on based on his circuit model for the variable component of the signal.
2 Study amplifiers voltage on bipolar transistors.
3 Study influences negative reverse connections on characteristics of amplifying devices.
4 Study aperiodic amplifying stages.
5 Study amplifiers power.
6 Study operating amplifiers.
7 Study functional schemes at the base operational amplifiers.
8 Study active filters on operating amplifiers.
9 Research of autogenerators.

PRACTICAL WORK No. 1

Subject: **STUDY PARAMETERS AND CHARACTERISTICS OF THE AMPLIFIER DEVICE BASED ON ITS CIRCUIT TECHNICAL MODELS FOR AC COMPONENT OF THE SIGNAL**

Time – 4 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of amplifying devices V mode small signal With using universal packages applied computer programs;

– to conduct a study of the main parameters and characteristics of the amplifying device based on its circuit model in the form of a hybrid U-shaped equivalent circuit ;

– collection and analysis of information to generate initial data for the design of electronic amplifying devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program schematic editor Electronics Workbench (EWB) simulation , version 5.12 or later, or NI Multisim Education version;

– application for mathematical and engineering calculations Mathcad Professional version not lower than 15.0;

– electronic methodological development By laboratory work.

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Development And analysis circuit design models amplifying devices V view hybrid U-shaped schemes substitutions.	30 min
2. Study parameters And characteristics amplifying devices on base his schematic model.	25 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study parameters And characteristics amplifying devices on base his schematic model.	55 min
Final Part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF THE WORK

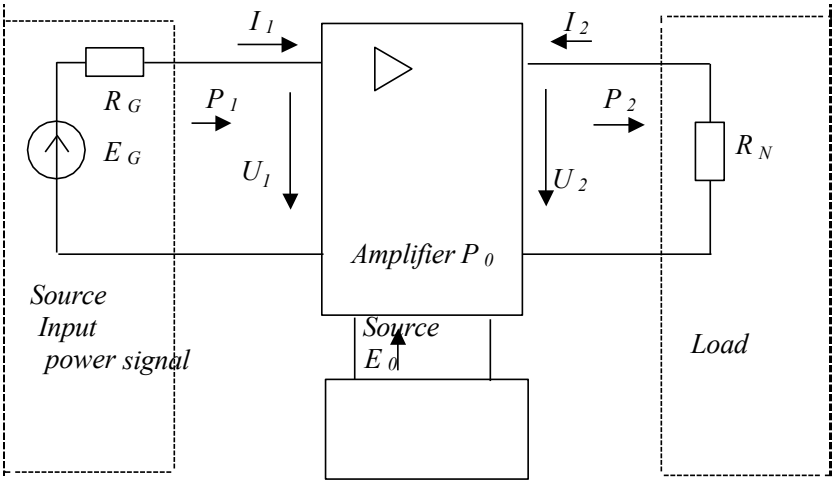
Brief theoretical or reference and information materials

1. General Provisions

An electronic amplifier is a device that converts low-power electrical signal on at the entrance V signal greater power on exit With minimal distortions forms. These amplifiers are called electronic, So How principle actions used in them amplifying elements (transistors, (electronic tubes, integrated circuits , thyristors and other devices) is based on electronic processes occurring in a semiconductor or vacuum.

The signal power is amplified by the amplifier consuming energy from an additional source called a power supply. Consequently, an amplifier is a device whose input signal controls the conversion of the power supply energy into the energy of the output signal. This conversion is carried out With help active elements amplifier (amplifiers) elements). The amplifier's output electrical signal is fed to a device called a load. The relationship between the amplifier, the input signal source, the load, and the power supply is shown in Figure 1.

IN quality source input signal can perform various sensors, microphone , photocell, thermocouple And etc., A Also preceding amplifier, because strengthening , given one amplifying element, For practical goals often turns out insufficient. Then V amplifier use some amplifying elements, included in such in this way, What reinforced first element signals are served on entrance second, amplified by the second - to the input of the third, etc. In this case, one amplifying element and the coupling elements assigned to it are called a cascade. Most amplifiers are multi-cascade .

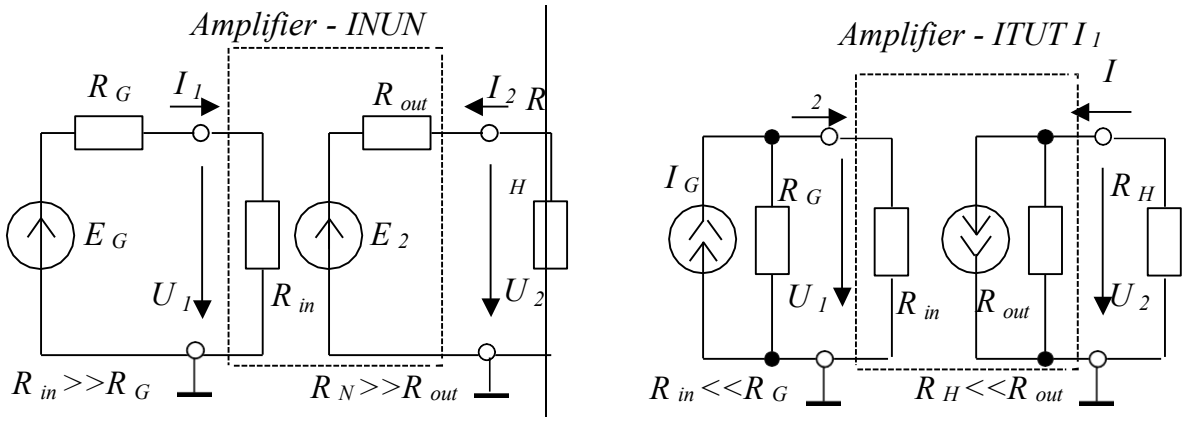


Rice. 1 Generalized scheme amplifying device

IN quality loads can perform telephone, speaker, various systems oscilloscope , relay, electric motor, communication channel, etc., as well as a subsequent amplifier.

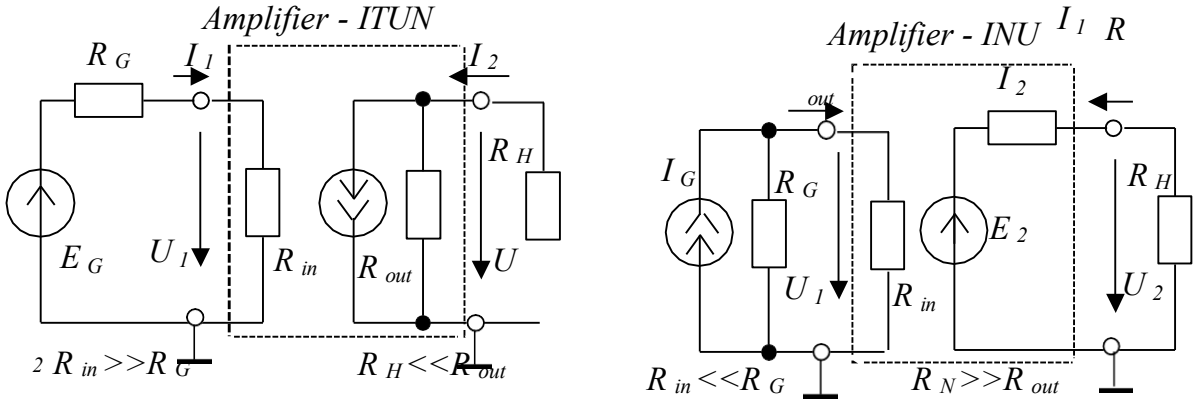
Because sources input signals And loads significantly differ By a couple of meters, That ***at analysis amplifiers follows consider*** ratios, With one sides, between source resistance signal R_G And input resistance amplifier R_{in} And, With another sides, between resistance loads R_H And weekend resistance amplifier R_{out}. IN dependencies from these ratios ***amplifier Maybe be managed*** or voltage (at $R_G << R_{in}$) or electric shock (at $R_G >> R_{in}$) And Maybe ***be For loads source*** current (at $R_H << R_{out}$) or source voltage (at $R_H >> R_{out}$).

Types of equivalent circuits of amplifiers with different ratios of the specified resistances given on rice. 2, Where INUN - This source voltage, voltage controlled, ITUT - source current, controlled electric shock, ITUN – source current, voltage- controlled , ICU – current-controlled voltage source.



A b

Rice. 2 - Varieties equivalent schemes amplifiers



V G

Rice. 2 - Varieties equivalent schemes amplifiers

Requirements To quantities input R_{in} ***And weekend*** R_{out} ***resistances amplifier are being produced, based on from analysis conditions transmissions maximum power V load*** . For example, For INUN (amplifier voltage) power V load $P_H = \frac{U^2_2}{R_H}$. So

How $U_2 = \frac{E_2 R_H}{R + R}$, A $E = K_U U$, K_U - coefficient gains amplifier By tension,
2 1
Whe
re

That $P_H = \frac{K^2 U^2 \cdot R_H}{(R + R_N)}$ $\frac{U_1}{R_2}$ $\frac{E_N R}{R_{in} + R}$. But since $U = \frac{K_G^2 \cdot (E \cdot R)^2 \cdot R}{(R_\Gamma + R)^2 \cdot (R_{вых} + R_N)}$, That $P_H = \frac{U_G}{R}$. From ana-
out vh in 2 1 in G

Lisa this expressions follows, What power V load will have maximum meaning only, If $R_G << R_{in}$ (V limit $R_{in} \to \infty$) And $R_{out} << R_H$ (in limit $R_{out} \to 0$). Then $P_{H\max} = \frac{K_U^2 \cdot E_G^2}{R_H}$.

Like this in this way, ***any amplifier must contain*** :

- ***an input device*** for undistorted, lossless transmission of energy from a signal source in entrance chain first amplifying cascade. Input device Maybe And be absent , If acceptable direct connection source signal To entrance first cascade. IN in particular, For the case under consideration INUN V as the first cascade Can

use cascade With common collector on bipolar transistors or With common stock on field-effect transistors, at which R_{in} great and can be provided $R_{in} >> R_G$;

- ***weekend device*** For undistorted without losses transmissions reinforced signal from the amplifier output circuit to the load. The output device may be absent if the direct connection loads To exit terminal cascade. IN in particular, for under consideration case INUN V quality terminal cascade Can use cas cad With common collector on bipolar transistors or With common stock on composite on the left transistor;

- ***The amplifier itself*** , which typically contains a series connection of simple amplification stages. These could be, for example, common-emitter stages on bipolar transistors or integrated gain stages implemented on integrated operational amplifier microcircuits. It should be noted that when constructing an amplifier that should not invert phase, an even number of such stages must be used on common-emitter stages;

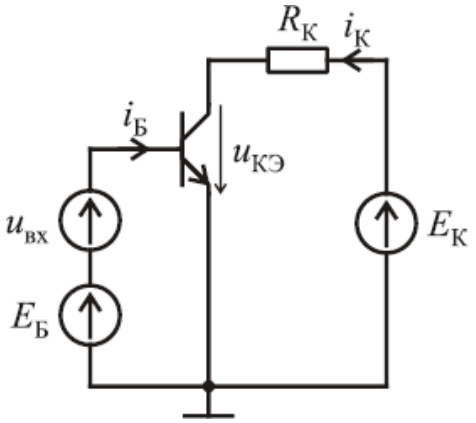
- ***Elements (circuits) of the connection*** between the signal source, amplifier, load, and between amplifier stages. These may include direct couplings, *RC* couplings, transformers, optocouplers, etc.

2. Models bipolar transistors For regime small signal

In amplifier circuits, currents and voltages contain both DC and AC components. The DC components are necessary to provide the required bias. transistor. Variables components contain useful information. These the components must be amplified and transmitted without distortion.

To simplify the analysis, the superposition method is used, i.e. the circuit is calculated - separately for the variable and constant components. The variable (signal) components have significantly smaller size, than a constant. Therefore, the calculation is based on the variable component they call *analysis V mode small signal* . Models transistor For small signal mode contains only linear elements.

For Togo to get model bipolar transistor For regime small signal, let's look at the diagram in Fig. 3.



Rice. 3 – Circuit diagram for connecting a bipolar transistor using a common emitter

IN chain base-emitter included source permanent voltage $E_б$, providing forward bias of the emitter junction, and the input signal source u_{in} .

Current collector at inclusion transistor By scheme with common emitter equal

$$i_К = \alpha I_{э0} e^{(E_б + u_{вх})/Vt} = \alpha I_{э0} e^{E_б/Vt} \cdot e^{u_{вх}/Vt} = I_К e^{u_{вх}/Vt}, \quad (1)$$

where I_{e0} – reverse current of the emitter junction, $I_к = \alpha I_{э0} e^{E_б/Vt}$ - constant component of the collector current, α is the emitter current transfer coefficient, ***Vt*** is the temperature potential, which is directly proportional to the absolute temperature and at 27 °C is equal to approximately 26 mV.

Let's break it down exponent V expression (1) V row Taylor. If variable the component of the input voltage is small, i.e. $u_{in} < Vt$, then in the expansion we can limit ourselves to the first two terms:

$$i_к \approx I_к \left(1 + \frac{u_{вх}}{Vt}\right).$$

Then variable current component collector is equal

$$i_к = \frac{I_к}{Vt} u_{вх} = g_m u_{вх}. \quad (2)$$

Coefficient proportionality $g_m = I_{to}/Vt$ - they call ***steepness or transfer conductivity*** of a bipolar transistor.

How follows from (2), steepness proportional constant component current collector I_{to} and back proportional constant ***Vt*** . For example, If I_{to} =10 mA, then at room-room temperature g_m = 400 mA/V. Like this in this way, V mode small signal bipolar The transistor can be considered as a current source controlled by voltage u_{in} .

Let's define Now variable component current bases. Full current bases equal

$$i_б = i'_б + i''_б = \frac{i_к}{\beta} = \frac{I_к}{\beta} + \frac{1}{\beta}\frac{I_к}{Vt} u_{вх},$$

Where **β** - transmission coefficient current bases.

Variable the base current component is equal to

$$i''_б = \frac{1}{\beta}\frac{I_к}{Vt} u_{вх}.$$

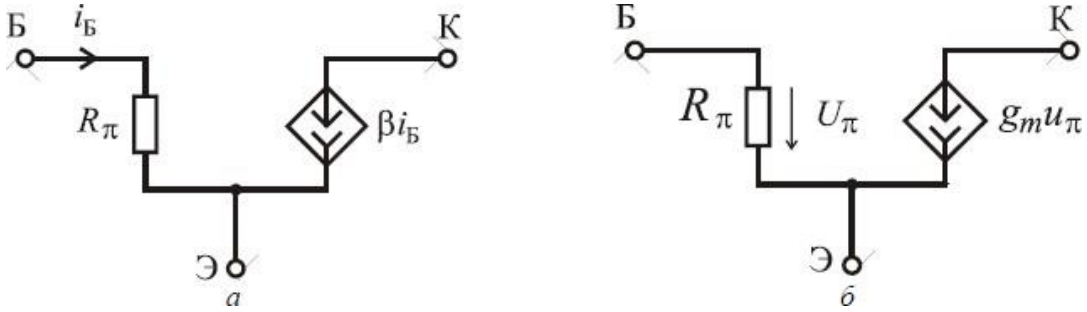
Considering, What $g_m = I_{to}/Vt$, we get

$$i_б = \frac{g_m}{\beta} u_{вх}.$$

Input resistance For variable component with sides bases equals

$$r_\pi = \frac{u_{вх}}{i_б} = \frac{\beta}{g_m}. \quad (3)$$

Received equalities (2) And (3) correspond low-signal models on rice. 4 *A, b* . Dependence (2) models controlled source current, A linear connection between i_b And u_{vkh} represented by a resistor connected between the base and the emitter.



Rice. 4 - Equivalent schemes substitutions bipolar transistor

According to (3), the resistance of the resistor r_π is directly proportional to β and inversely proportional to the DC component of the collector current. Since $g_m = I_k/Vt$, and the base current $I_b = I_k/\beta$, then another expression for r_π can be obtained :

$$r_\pi = \frac{Vt}{I_б}.$$

IN last expression I_b - constant component base current .

The equivalent circuits in Fig. 4, *a, b* are called ***hybrid U-shaped models of a bipolar transistor*** . Thus, at low alternating voltages not exceeding ***Vt*** , a bipolar transistor is equivalent to a current source controlled by voltage u b_e or current $i_б$.

Models transistor For regime small signal contain only linear elements .

The analysis of circuits with bipolar transistors in small signal mode is performed in the following order .

1) collector current *I* k and voltage *U* ke . The circuit for determining the operating point is obtained by replacing the inductive elements short short circuit, A capacitive - breaks. Sources variable signals are excluded from the circuit, leaving only sources of constant voltages and currents.

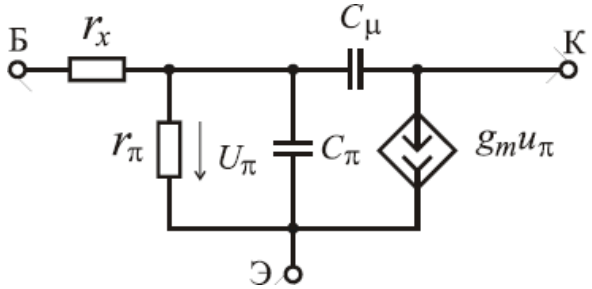
2) By results calculations, completed on first step, are calculated model parameters for small signal mode:

$$g_m = I_к/Vt\ ,\ r_\pi = \beta/g_m\ ,\ r_э = Vt/I_э\ .$$

3) A design scheme for small-signal mode is developed. The transistor is replaced with one of the small-signal mode models (Fig. 4). DC voltage and current sources are excluded.

4) In progress analysis calculated schemes, received on previous step.

The bipolar transistor models shown in Fig. 4, *a, b* , ***are used for analysis in the mid-frequency range*** , where it is possible not to Consider the frequency dependence of transistor parameters. To account for effects that become significant at high frequencies, additional elements are included in the equivalent circuit (Fig. 5).



Rice. 5 - Equivalent schemes substitutions bipolar transistor on high often-tah

Resistor r_x takes into account resistance basic layer. Size this resistance depends on the type of transistor and the position of the operating point and can vary from units to several tens of ohms. Capacitor C_μ takes into account the capacitance of the reverse-biased collector junction. Capacitor C_π takes into account the capacity associated with the accumulation of non-essential carriers V base, And capacity, conditioned spatial charge V emitter region transition. IN most cases C_π makes up from units picofarad to several tens of nanofarads. Capacitance C_μ does not exceed a few picofarads.

Let's consider an amplifier in which the transistor is connected according to the circuit With common emitter, and negative feedback is used to stabilize the operating point By current (Fig. 6).

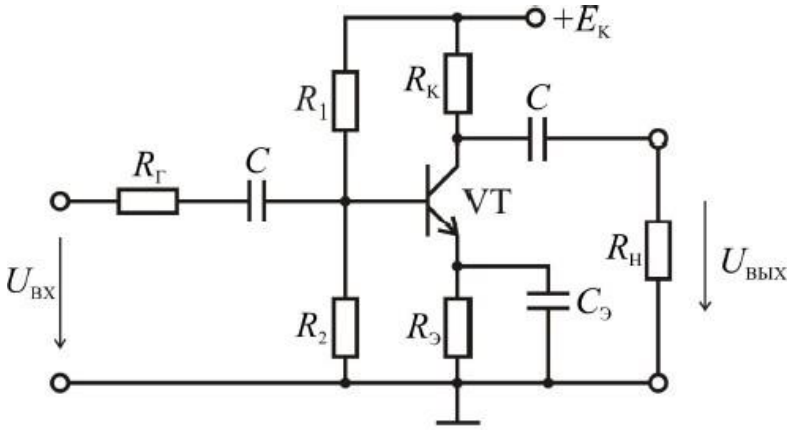


Fig. 6 – Typical amplifier stage with a common emitter Capacitors *From* 1 And *From* 2 are dividing: *From* 1 hinders connections By constant-current of the input signal source and the amplifier, and *C* 2 serves to separate the direct current of the collector circuit and the load.

Capacitances *C* 1 and *C* 2 are selected such that at the frequency of the alternating component their resistance Can was neglect. Resistor *R* g takes into account internal resistance signal source. Resistors R1 *and* R2 *form* a voltage divider that determines the position of the operating point of the emitter junction.

Resistor V chains collector transforms change current collector V weekend voltage . On exit chains included resistor loads *R* n , With whom is being removed reinforced signal .

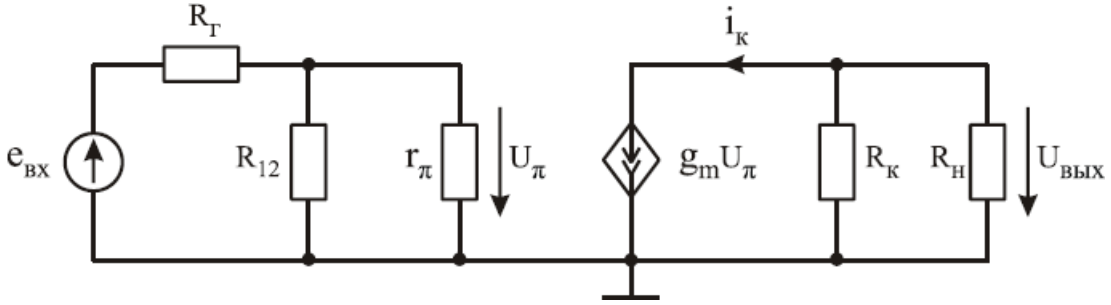
Resistor *Rэ* is a negative feedback circuit. Capacitor *Cэ* in the emitter circuit shunts resistor *Rэ* . The capacitance of this capacitor is chosen such that at the signal frequency

$$X_э = \frac{1}{\omega C_э} << R_э .$$

For check this increases coefficient gains variable component.

Since the circuit contains AC (input signal source) and DC sources voltage, For calculation we use method overlays. Let's analyze chain separately for the variable components. Recall that this analysis is called small-signal mode analysis.

Analysis of the AC component . Let's eliminate the DC voltage source from the circuit. ***Ek*** , replacing his short short circuit. Upper clamps resistors ***R1*** And ***Rk*** will be grounded, so ***R1*** and ***R2*** , ***Rк*** and ***Rн*** are connected in parallel. Capacitances of capacitors choose such, to their resistance on frequency variable component was small compared to the resistances of the resistors. Therefore, the capacitor terminals were short-circuited. Replacing transistor low-signal model, we will receive equivalent diagram amplifier for small signal mode (Fig. 7).



Rice. 7 - Equivalent scheme substitutions amplifier By scheme With common emitter For small signal mode

On equivalent resistance circuit

$$R_{12} = \frac{R_1 R_2}{R_1 + R_2}.$$

Resistor $R_э$ in the emitter circuit it is shunted by a small resistance of the capacitor $C_э$, therefore there is no negative feedback on the variable component.

The input impedance of the circuit is equal to the resistance of the parallel connection of two resistors.

$$R_{вх} = r_\pi \| R_{12}.$$

Typically, the input resistance of a common emitter circuit is low and does not exceed a few kOhms.

Let's define the output equivalent voltage schemes amplifier. Resistors $R_г$, $R12$ And r_π form divider voltage, That's why

$$u_\pi = \frac{r_\pi \| R_{12}}{R_г + r_\pi \| R_{12}} e_{вх}.$$

Weekend voltage schemes on Fig. 5 is determined by the expression

$$u_{вых} = -g_m R_к \| R_н u_\pi = -\frac{g_m R_{вх}}{R_г + R_{вх}} R_к \| R_н e_{вх}. \quad (4)$$

If resistance source signal not big, That voltage $u_\pi \approx e_g$, And formula (45) can be simplified:

$$u_{вых} = -g_m R_к \| R_н e_{вх}.$$

Coefficient gains variable component voltage is equal

$$K_U = \frac{u_{вых}}{e_{вх}} = -g_m R_к \| R_н. \quad (5)$$

Sign minus V last expression indicates on That, What input And day off the signals are out of phase.

Let's define coefficient gains current schemes With common emitter. When $R_н << R_к$ the output current

$$i_{вых} = -i_к = -g_m R_{12} \| r_\pi i_{вх}$$

Coefficient gains variable component current

$$K_i = \frac{i_{вых}}{i_{вх}} = -g_m R_{12} \| r_\pi \approx -g_m r_\pi = -\beta.$$

This is the maximum current gain that can be obtained in the short-circuit mode of the output terminals, at $R_н = 0$.

In most cases $|K_i| < \beta$, due to the fact that part of the output current is closed through the resistor $R_э$.

So, the common emitter circuit provides both voltage and current gain. She has not high input (hundreds om - tens kOhm) And relatively big output resistance (units to tens of kiloohms). In multi-stage amplifiers, a common emitter circuit is used to achieve the required voltage gain.

IN mode small signal transistor amplifier represents by yourself ***linear Active four-terminal device*** . When the transistor stage operates in small-signal mode, the greatest gain of the input signal is achieved with minimal distortion. A characteristic feature of this mode is that the transistor's operating point remains in the linear region for all possible input signal values.

3. Transistor noise

The main components of transistors' own noise are thermal and shot noise.

Thermal noise is caused by the chaotic thermal motion of charge carriers within a semiconductor or conductor. As a result, a random fluctuation EMF acts at the ends of a conductor with a certain resistance, which is called EMF thermal noise E $_{pcs}$. Thermal noises have uniform frequency spectrum (white noise) and are estimated by the root-mean-square EMF of the noise:

$$E_{шm}^{2} = 4kTR_{ш}П_{ш},$$

Where k = 1.37-10 $^{-23}$ J/K — constant Boltzmann; T — absolute temperature; R_{sh} — equivalent "noise" resistance; P_{sh} — the frequency band in which the noise EMF is calculated.

In transistors, thermal noise is mainly determined by the bulk resistance of the base, since the bulk resistance of the emitter and collector is small due to the high concentration of carriers in them.

Root Mean Square Thermal EMF noise transistor

$$E_{pcs}^{2} = 4kTr_{b}P_{sh},$$

Where r_b — volumetric base resistance .

Shotguns noises are determined unevenness in time density flow charge carriers of the collector, emitter, and base currents. The shot noise EMF consists of the noise introduced by the emitter-base and collector-base junctions:

$$E_{she}^{2} = 2q r_{e}^{2}(I_{E} + I_{EB0})P_{sh},$$

Where q — charge electron, r_e — differential resistance emitter transition; I_E — emitter current; I_{EB0} — reverse emitter current.

On collector transition EDS shotgun noises V basically depends from reverse collector current $I_{КБ0}$

$$E_{shk}^{2} = 2q r_{to}^{2} I_{KB0} P_{sh},$$

Where r_K — differential resistance collector junction.

The noise properties of a transistor, as an active element of an amplifier, are generally characterized by the noise factor.

The noise figure F determines the increase in noise referred to the transistor input compared to the noise generated by the internal resistance of the signal source. The formula for the noise figure is determined as follows:

$$F = \frac{E_{shg}^{2} + E_{shtr}^{2}}{E_{shg}^{2}} = 1 + \frac{E_{pcs}^{2}}{E_{shg}^{2}}. \quad (6)$$

Coefficient noise shows, as far as increases noise on exit transistor.
His usually express V decibels at given resistance source signal R_G.

$$NF(\text{дБ}) = 20\lg(F). \quad (7)$$

If we compare the parameters of a field-effect transistor and a bipolar transistor in the audio frequency range By coefficient noise, That field transistor will lose because of influences resistance of the signal source R_G.

Contents of the practical work performed students V in the course classes

Description laboratory equipment:

- PC for each student;
- program editor schematic modeling Electronics Workbench" (EWB) version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher.

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) In case of emergency situations, it is necessary to immediately disconnect the equipment from the power supply, inform the teacher about this and act according to his instructions .

6) If equipment catches fire, it must be immediately de-energized, the teacher must be informed, measures must be taken to eliminate the fire, and the teacher must act as instructed.

7) By ending work With laboratory equipment (computers) his must be switched off in the established order.

Initial data for modeling and research

Options for tasks for individual modeling and research by students are presented in Table 1.

Table 1 - Options tasks For modeling and research.

Option	**f,** MHz	**Uh,** In	**Rvykh** , mW	β	**Hey** , pF	**Where** , pF
0	1	10	5	100	100	10
1	0.5	11	6	95	150	20
2	1.5	12	7	90	140	19
3	2	13	8	80	130	18
4	2,5	14	9	75	120	17
5	3	15	10	70	110	16
6	3,5	10	11	65	100	15
7	4	11	12	60	90	14
8	4,5	12	13	105	80	13
9	5	13	14	110	75	12
10	5,5	14	15	115	70	11
11	6	15	14	120	65	10
12	6,5	10	13	100	60	9
13	7	11	12	95	55	8
Variant	**f,** MHz	**Uh,** In	**Rvykh** , mW	β	**Hey** , pF	**Where** , pF
14	7.5	12	11	90	50	7
15	8	13	10	85	45	6
16	8,5	14	9	80	45	5
17	9	15	8	75	40	5
18	9,5	12	7	70	35	4
19	10	14	6	65	30	4
20	1	16	10	60	100	12

Tasks, performed V in the course l work

Tasks basic level:

1) Develop in a computer modeling software package circuit model of the amplifying device in the form of a hybrid U-shaped equivalent circuit.

2) Conduct analysis developed circuit design models amplifying device-state.

Tasks increased level:

3) Study frequency properties amplifier (amplitude-frequency And phase-frequency characteristics, the range of amplified frequencies) and the resulting frequency distortions .

4) Study amplitude characteristics amplifier, his sensitivity, dynamic range and the resulting nonlinear distortions.

Order execution work

Exercise 1. Develop V software package computer modeling technical diagram model amplifying devices V view hybrid U-shaped schemes for replacements.

Task And original simulation data . Simulate in program EWB A schematic model of the amplifier device in the form of an equivalent circuit. The model should contain equivalent circuits for the signal source, the amplifier itself based on a voltage-controlled current source (VCCS), and the load. The circuit simulation should be performed using functional blocks and base elements radio engineering available in the Electronics Workbench program.

For constructions schemes substitutions source signal follows use theorem about the equivalent source, according to which any scheme, no matter how complex, can always be introduce V view source voltage (generator EMF ***Ug***) And included in series with it a resistor ***Rg*** corresponding to the output resistance. In this case, the equivalent circuit of the signal source should contain a noise generator ***Vn1*** simulating the voltage noise, created external Wednesday, or voltage own noise active element (transistor) of the previous stage. An FM signal generator should be used as a noise generator, setting its modulating frequency to be comparable to the carrier frequency of the signal and a very large (on the order of several thousand) modulation index. In this case, a noise-like signal close to natural noise is produced.

The basis schematic models directly himself amplifier performs, the equivalent circuit shown in Fig. 7 amplifier according to the diagram with a common emitter for small signal mode. To take into account the physical effects that occur in amplifiers at high frequencies, scheme substitutions should be supplemented, How shown on rice. 5 capacitors simulating the capacitances of the collector junction ***Ck*** , as well as the base and emitter ***Cbe*** .

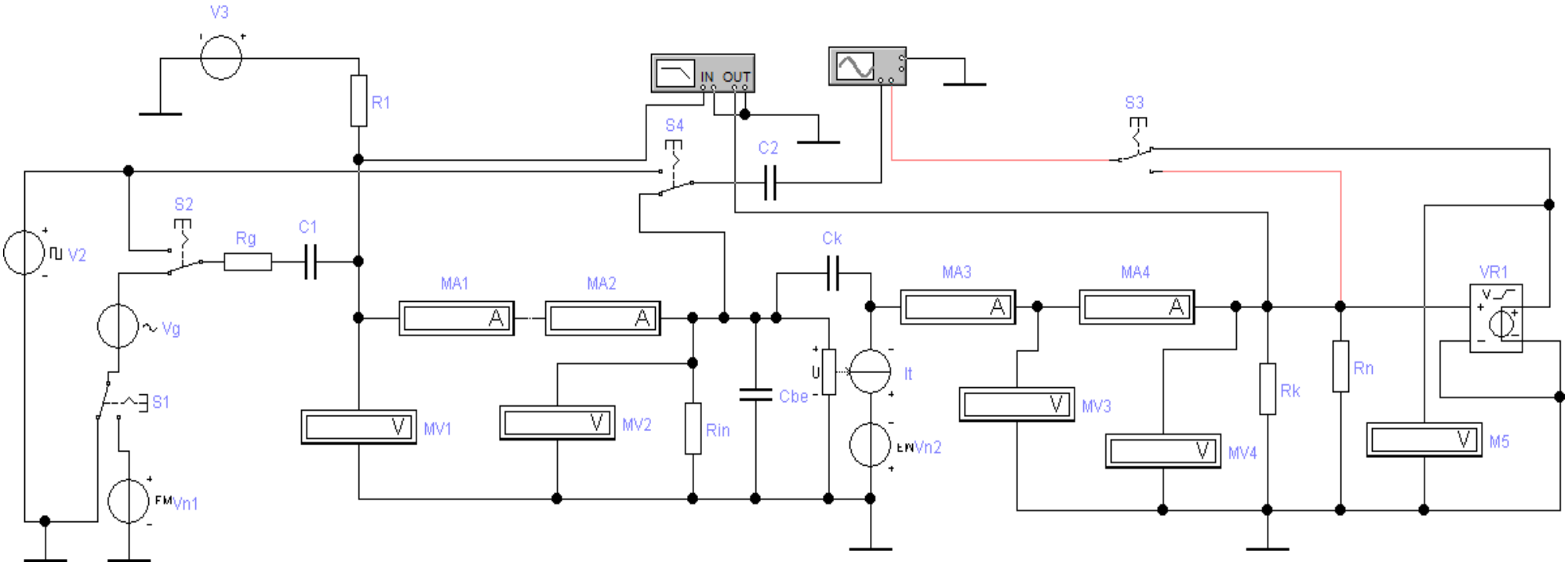
In addition, to simulate the nonlinear properties of the amplifier in large signal mode scheme substitutions should contain limiter voltage ***VR1*** . A For introduction In the model of the constant current component that determines the operating point, the equivalent circuit must contain a constant voltage source ***V3*** and a resistance ***R1*** that simulates the resistance in the base circuit.

The output of the amplifier equivalent circuit must be connected to the load resistance ***Rn*** (the input resistance of the next stage).

For metrological provision conducting research scheme substitutions must contain:

- ammeter ***MA1*** for measurements of constant current on at the entrance amplifier;
- ammeter ***MA2*** for variable measurements current on at the entrance amplifier;
- voltmeter ***MV1*** for measurements of constant voltage on at the entrance amplifier;
- voltmeter ***MV2*** for variable measurements voltage at the entrance amplifier;
- ammeter ***MA3*** for measurement permanent current on exit amplifier;

– ammeter ***MA4*** for measurement alternating current at the amplifier output ;
– voltmeter ***MV3*** for measurements of constant voltage on exit amplifier;
– voltmeter ***MV4*** for variable measurements voltage on exit amplifier;
– voltmeter ***M5*** for measuring variable voltage in load amplifier;
– ***S4*** and ***S3*** connected to its inputs for switching various points of the circuit to the oscilloscope inputs;
– Bode plotter for obtaining amplitude-frequency and phase-frequency characteristics (AFC and PFC).



Rice. 8 - Example circuit design models amplifying devices V view hybrid U-shaped schemes substitutions

Order circuit simulation.

1) In the Mathcad Professional application for mathematical and engineering calculations, perform calculation parameters elements schemes substitutions. For this execute the following actions:

1.1) IN open window programs enter By given option original data:

- power supply voltage $U_п$;
- given day off power amplifier R_{out};
- statistical coefficient transmissions By current β;
- temperature potential, equal Vt = 25.6 mV.

1.2) Enter formulas And calculate next parameters:

- permanent voltage on collector relatively general points (emitter)

$$Uкэо := \frac{Uп}{2};$$

- constant component current collector (elementary collector current)

$$Iко := \frac{Pвых}{Uкэо};$$

- steepness or transmission conductivity transistor

$$g := \frac{Iко}{Vt};$$

- resistance V chains collector

$$Rк := \frac{Uп}{2 \cdot Iко};$$

- constant component current bases (elementary current bases)

$$Iбо := \frac{Iко}{\beta};$$

- permanent voltage on base relatively general points (emitter)

$$Uбэо := \frac{Iко}{g};$$

- input resistance amplifier

$$Rвх := \frac{Vt}{Iбо};$$

- resistance V base chains

$$Rб := \frac{Uп - Iбо \cdot Rвх}{Iбо}.$$

1.3) Include in the lab report a listing of the program typed in Mathcad with the calculation results.

2) Collect V program EWB electrical diagram substitutions amplifier. Example schematic - model of an amplifying device in the form of a hybrid U-shaped equivalent circuit presented on rice. 8. Connect To scheme measuring devices: oscilloscope, graph plotter, ammeters and voltmeters.

3) In the assembled circuit model, check the correctness of the assembly, paying attention, first of all, to the correct connection of the circuit elements to each other, as well as the connection of measuring instruments and switching keys, paying special attention to the connection of the power source and grounding.

The procedure for setting up, debugging and checking the performance of the simulated equivalent circuit.

1) Enter V collected diagram given or calculated parameters elements:

– the frequency in the signal source (EMF generator ***Ug***) according to the specified option, and the voltage equal to 5 mV;

– internal resistance ***Rg*** source signal (generator EMF ***Ug***) initially set to 1 Ohm;

– dividing capacitor ***C1*** install equal 10 μF;

– in the noise generator ***Vn1*** , simulating the noise voltage created by the external environment, set the carrier amplitude to 0.02 mV, the carrier frequency to 5 MHz, the modulation index to 5000, and the modulating frequency to 4.9 MHz;

– in the noise generator ***Vn2*** , simulating the amplifier's own noise voltage, set amplitude load-bearing 1 mV, load-bearing frequency 5.1 MHz, index modulations 5000, modulating - frequency of 4.9 MHz;

– set the voltage in the power source ***V3*** , as well as the capacitances in the capacitors ***Ck*** and ***Cbe, according to the specified option;***

– install V in accordance With received calculated values quantities input resistance R_{in} , resistances in the base circuit R_b and collector R_k ;

– ***It*** in accordance with the calculated value obtained ;

– size resistance loads R_n initially install equal resistance in the collector circuit R_k ;

– V limiter voltage ***VR1*** install lower limit (VL) equal minus by the half supply voltage, and the upper limit (VU) is equal to 0 V;

– install V source (generator) rectangular impulses ***V2*** frequency, V ten times less than the specified frequency, and the pulse amplitude equal to 10 mV.

2) Tune means measurements, For this execute next operations:

– ammeters **MA1, MA3** switch to DC current measurement mode, and ammeters **MA2** , **MA4** switch to AC current measurement mode;

– voltmeters **MV1** and **MV3** are switched to the DC voltage measurement mode, and voltmeters **MV2** , **MV4** and **MV5** are switched to the AC current measurement mode;

– DC voltage measurement mode **DC** So, to By first channel (A) was observed weak input signal, For this set the vertical sweep to 50 mV/div, and on the second channel (B) – the amplified output signal, For this install vertical development - 2 In/case, at this horizontal Time base should be between 0.50 and 0.10 μs/div;

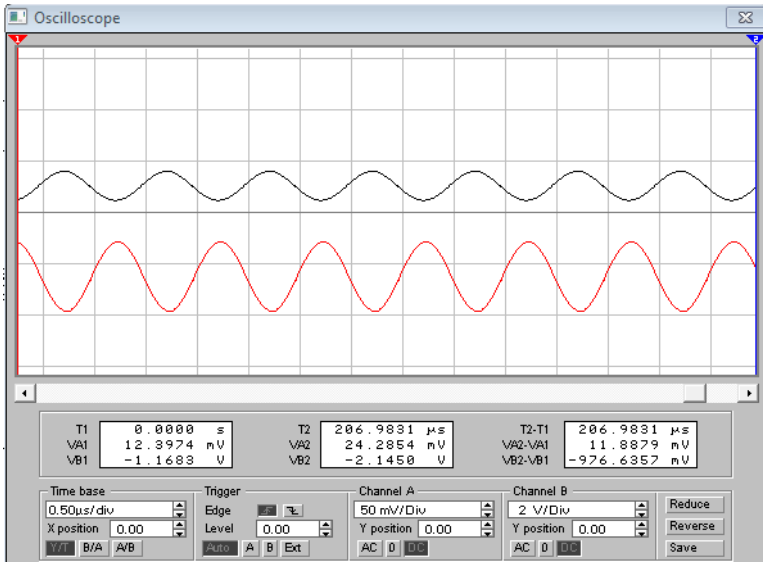
– Set up a graph plotter (Bode plotter) to measure the frequency response; to do this, set the vertical sweep from I = 20 dB to F = 60 dB, and the horizontal sweep from I, equal to a frequency half the frequency of the input signal, to F, equal to a frequency one hundred times greater than the input signal.

3) Conduct check performance circuit design models, For this perform the following operations:

– set the switching keys ***S1*** and ***S2*** to the left and lower positions , respectively, thereby connecting only the signal source (EMF generator ***Ug***) to the amplifier input without the external noise source ***Vn1*** ;

– set the switching keys ***S3*** and ***S4*** to the upper and lower positions, respectively, connecting the input signal to the first channel of the oscilloscope and the signal from the amplifier output to the second channel;

– run the EWB simulator, set up the oscilloscope sweep on the first channel for measurements input signal, A By to the second channel For weekend signal. Having received oscillograms input And weekend reinforced signal, make sure V volume, What They similar on about exemplary oscillograms, given on rice. 9. Bring in received oscillogram V laboratory work report.



Rice. 9 - Exemplary oscillograms, demonstrating right work developed amplifier equivalent circuit

If the oscilloscope does not show the output signal, then find errors in the circuit assembly or in the switching of measuring instruments, then eliminate them, achieving correct operation of the circuit.

4) Include a screenshot of the developed and working amplifier circuit model in your report. Draw conclusions based on the work completed in the assignment.

Task 2. Conduct an analysis of the developed circuit model of the amplifying device.

Statement of the problem and analysis methods . The task of analyzing the developed circuit design models amplifying the device consists of V receipt most complete information about its properties, identifying the relationships between input and output parameters necessary for the effective practical use of the device. In addition, the task of analysis includes assessment adequacy developed models amplifier, definition By this model of given functions and parameters, construction of frequency, time and other characteristics .

Methodology analysis consists of V definition reaction (response) developed equivalent circuits amplifier on a priori famous impacts, called measuring signals when changing the internal parameters of the circuit or external parameters that affect the operation of the electronic circuit.

As part of this task, the input and output resistances of the amplifier are calculated. devices, grade his transmission (amplifying) properties, definition its output power, as well as a study of their dependence on external and internal parameters .

Order execution tasks.

1) Define For given internal parameter amplifier (steepness transistor g) transfer (amplification) indicators of the circuit substitutions amplifier. For this take measurements, calculate and enter into table 2:

– coefficients transmissions (reinforcements) By constant and variable currents $K_I = I_k / I_b = I_{out} / I_{vh}$ and $K_{and} = and_k / and_b = and_{exit} / i_{vh}$,

Where $I_{in} = I_b$ - permanent meaning current bases, measured ammeter ***MA1*** , A $I_{'m\ leaving} = I_k$ - permanent meaning current collector, measured ammeter ***MA3*** ; Where $i_{in} = i_b$ - dey-existing meaning current bases, measured ammeter ***MA2*** , A $and_{out} = i_k$ - current collector current value measured by ammeter ***MA4*** ;

– coefficients transmissions (reinforcements) at a constant rate And variable voltages

$$FATE = U_{ke} / They_{are} = U_{exit} / U_{vh} \text{ and } Fate = u_{k}\, e\, / u_{be} = u_{output} / u_{vh},$$

Where $U_{in} = U_{be}$ - permanent voltage on base relatively emitter, measured voltmeter *MV1*, A $U_{out} = U_{ke}$ - voltage on collector relatively emitter, measured ammeter *MV3*; Where $u_{vkh} = u_{be}$ - current voltage on base relatively emitter, measured ammeter *MV2*, A $u_{out} = u_{ke}$ - current voltage on collector fromrelative emitter, measured ammeter *MV4*;

– coefficients transmissions (reinforcements) By constant And variable capacities

$$K_P = K_U \cdot I \text{ and } K_p = You \cdot You;$$

– express calculated coefficients gains V view coefficients gains by power in decibels:

$$K_I[dB] = 20 \cdot \lg(I_{out} / I_{in}) \text{ And } K_i[dB] = 20 \cdot \lg(i_{out} / i_{in}),$$

$$K_U[dB] = 20 \cdot \lg(U_{out} / In_{the\ entrance}) \text{ and } To[dB] = 20 \cdot \lg(u_{out} / in_{the\ entrance}),$$

$$K_P[dB] = 10 \cdot \lg(K_U \cdot K_I) \text{ and } K_p[dB] = 10 \cdot \lg(K_u \cdot K_i);$$

Table 2 – Results of calculations and measurements.

g, A/B	K_I	K_I [дБ	] K_i	K_i [дБ	] K_U	K_U [дБ	] K_u	K_u [дБ	] K_P	K_P [дБ	] K_p	K_p[дБ
0,5g												
g												
2g												

2) Change the internal parameters of the amplifier by setting the transistor slope in series ***g***, equal ***0.5g***, ***2g***. For data values produce measurements And calculation everyone gain coefficients. The obtained results are entered into Table 2.

3) Draw conclusions based on the results of the conducted research, including how the internal transistor slope parameter affects the studied amplifier parameters.

4) Determine the amplifier's input and output impedances for a given external amplifier parameter (***Rg = 1 Ohm). To do this, take measurements, calculate, and enter the results in Table 3:***

– input resistance By direct current

$$R_{in\,0} = (U_{in\,0} / I_{in\,0}) \text{ at } R_n = const,$$

where $U_{in\,0}$ - permanent input voltage, measured voltmeter *MV1*, the input $I_{input\,0}$ - constant-current measured by the ammeter *MA1*.

– input resistance By alternating current

$$R_{input\sim} = (u_{in} / and_{in}) \text{ at } R_n = const,$$

Where u_{vkh} - variable input voltage, measured voltmeter *MV2*, i_{in} - variable input current, measured ammeter *MA2*.

– weekend DC resistance current

$$R_{out\,0} = U_{out.xx} / I_{output.kz},$$

Where $U_{out.xx}$ - voltage single move on exit amplifier (at R_n =1000 Mohm ≈ ∞), measured voltmeter *MV3*; $I_{output.kz}$ – current short short circuits (at R_n = 0.1 Ohm ≈ 0), measured ammeter *MA3*.

– weekend resistance By variable current

$$R_{out\sim} = u_{out.xx} / i_{out.kz},$$

Where $u_{out.xx}$ – variable voltage single move on exit amplifier (at R_n =1000 Mohm ≈ ∞), measured voltmeter *MV4* ; $i_{out.kz}$ - variable current short short circuits (at R_n = 0.1 Ohm ≈ 0), measured ammeter *MA4* .

Bring in results measurements V table 3. Compare quantities measured resistances with those previously calculated.

Table 3 - Calculation results And measurements.

resistance Rg	R_{vx0}, Om		$R_{vh\sim}$, Om	P_{vx0}, μW	$P_{vx\sim}$, μW
	Calculate.	Measured.			
Rg = 1 Ω					
Rg = 100 Ω					
Rg = ***Rin***					
Rg = 10 kOhm					
resistance Rн	R_{out0}, Ohm		$R_{out\sim}$, Ohm	P_{out0}, μW	$P_{out\sim}$, μW
	Calculate.	Measured.			
Rn = 100 Ohm					
Rn = ***Rк***					
Rg = 10 kOhm					

5) Define For given external parameter amplifier (***Rн*** = ***Rк***) quantities input and output powers of the amplifier for direct and alternating current. For this purpose, take measurements, calculate and enter into Table 3:

– entrance power By direct current

$$P_{in0} = U_{in0} \cdot I_{in0},$$

where U_{in0} - permanent input voltage, measured voltmeter *MV1* , the input I_{in0} - constant-current measured by the ammeter *MA1* .

– entrance power By alternating current

$$P_{in\sim} = u_{in} \cdot and_{in},$$

Where u_{vkh} - variable input voltage, measured voltmeter *MV2* , i_{in} - variable input current, measured ammeter *MA2* .

– day off power By direct current

$$P_{out0} = U_{out0} \cdot I_{out0},$$

Where U_{out0} - permanent voltage on exit amplifier, measured voltmeter *MV3* ; I_{out0} - constant current on exit amplifier, measured ammeter *MA3* .

– day off power By alternating current

$$P_{out\sim} = u_{out} \cdot and_{out},$$

Where u_{out} - variable voltage on exit amplifier, measured voltmeter *MV4* ; ***and*** – variable current on exit amplifier, measured ammeter *MA4* .

out 6) Change external parameters amplifier, having installed sequentially resistance generator ***Rg*** , equal 100 Ohm, 10 kOhm And calculated entrance resistance. For take measurements from these values and Calculate input resistances and input powers. Enter the results into Table 3.

7) Change external parameters amplifier, having installed sequentially load resistance ***Rн*** , equal to 100 Ohm, 10 kOhm. For these values, take measurements and calculate the output resistances And weekend capacities. Received results bring in V Table 3.

8) Draw conclusions based on the results of the studies, including how they influence external parameters resistance generator And loads on researched amplifier indicators .

9) Do generalized conclusions By results analysis, completed V task 2.

Task 3. Study of the frequency properties of the amplifier (amplitude-frequency and phase-frequency characteristics, range reinforced frequencies) And emerging frequency distortion .

Statement of the problem and research methodology . The objective of the study of the developed circuit model of the amplifying device is to obtain the most complete information about his frequency properties, V establishment reasons, contributing the occurrence of frequency distortions.

The research methodology consists of determining the reaction (response) of the developed scheme substitutions amplifier on a priori famous impacts, called measuring signals, when changing the internal parameters of the circuit or external parameters that affect on work electronic schemes. IN quality measuring signal is used subsequence rectangular impulses, having endlessly big quantity harmonics. As part of this task, the frequency response and phase response of the amplifier equivalent circuit are measured , range reinforced frequencies (stripes transmission), A Also is being carried out studies of how these characteristics affect the frequency distortion that occurs in the amplifier.

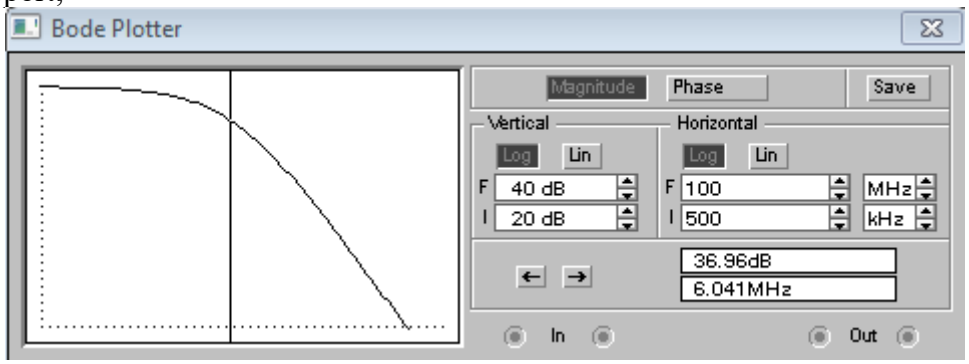
Order execution tasks.

1) Conduct measurements frequency response And phase response schemes substitutions amplifier. For this perform the following operations:

– install switching keys V next provisions: ***S1*** - V left, ***S2*** - V bottom, and resistance ***Rg*** = 1 Ohm;

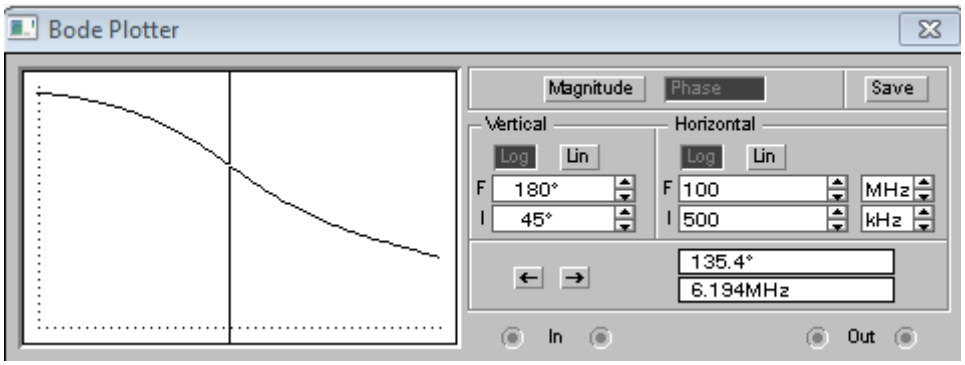
– run the EWB simulator, open the Bode plotter, which should be configured to obtain a frequency response of approximately the same type as shown in Fig. 10;

– measure range reinforced frequencies (strip transmission amplifier) With using the obtained frequency response, to do this, use the cursor located on the left side of the plotter screen to move on such frequency, at which maximum values coefficient gains will decrease by 3 dB. Enter the obtained frequency response with the results of frequency range measurement into the laboratory report;



Rice. 10 - Example of setup graph plotter For frequency response measurements

– switch plotter For measurements phase response, by clicking Phase button, And adjust it in such a way as to obtain a phase response of approximately the type shown in Fig. 11;



Rice. 11 - Example of setup graph plotter For phase response measurements

– measure range reinforced frequencies (strip transmission amplifier) With using the obtained phase frequency response, to do this, move the cursor located on the left side of the plotter screen to a frequency at which the maximum phase value decreases by 45 degrees. Bring in V report By laboratory work received phase response With results measurements frequency range ;

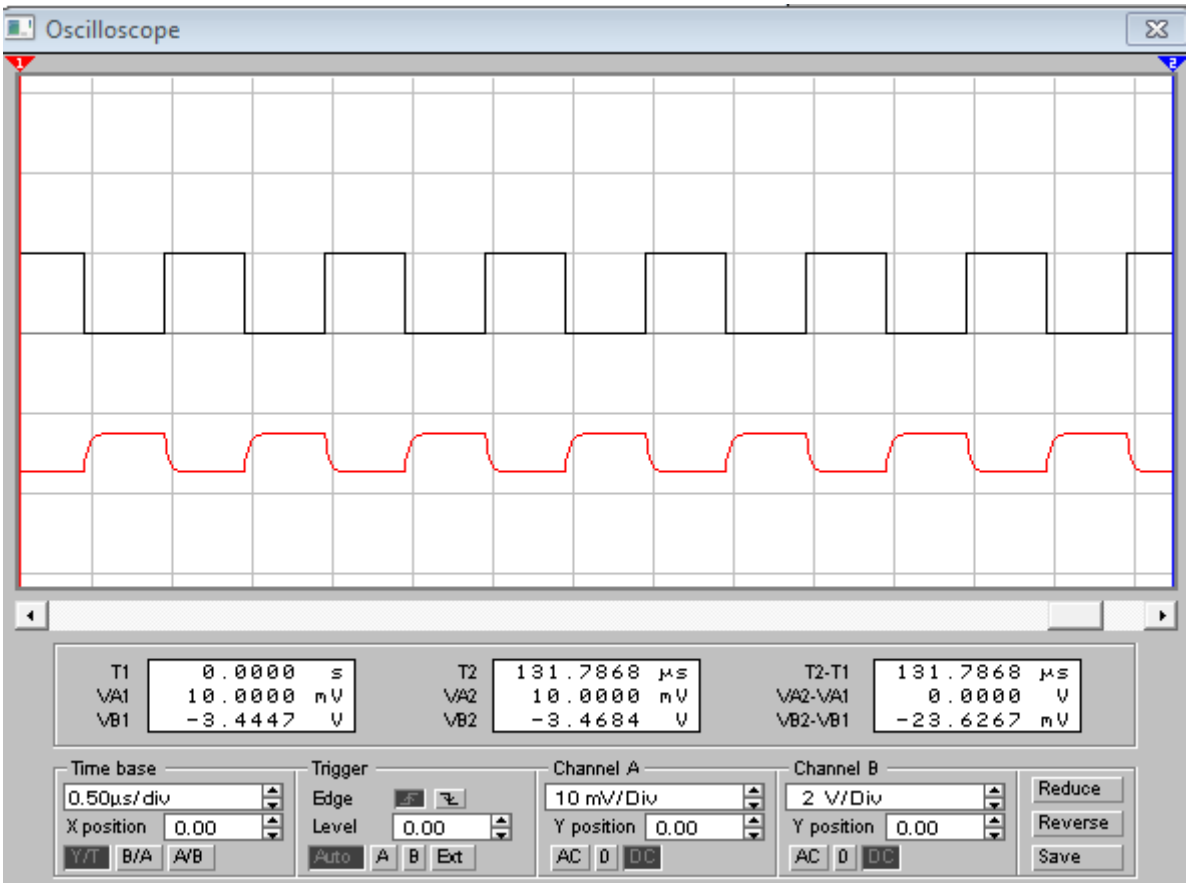
– Having analyzed the obtained frequency response and phase response, formulate a conclusion about what type of filter, in terms of bandwidth, this amplifier belongs to.

2) Simulate frequency distortions, emerging on exit amplifier. For To do this, perform the following operations:

– install switching keys V next provisions: ***S2*** - V top, ***S4*** - V top;

– install frequency fluctuations rectangular impulses V generator ***V2*** , equal frequency harmonic signal V generator ***V1*** ;

– run the EWB simulator, open the oscilloscope, and configure it as follows , to get oscillogram, approximately such species, How shown on rice. 12, at In this case, the first channel displays an input measuring signal in the form of a sequence of rectangular pulses, and the second channel displays a distorted signal at the amplifier output. Add the resulting oscillogram to the report;



Rice. 12 - Example settings oscilloscope

– qualitatively assess what frequency distortions led to, how the input signal was distorted.

3) Determine the frequency distortion coefficients of the first 5 odd harmonics of rectangular pulses using a graph plotter. To do this, perform the following operations:

– switch switching key ***S2*** V lower position,

– Run the EWB simulator, open the Bode plotter by moving the cursor on required frequencies, produce measurements coefficients gains on them And enter them into table 4;

Table 4 - Calculation results And measurements.

Harmonic frequency	f_{g1} =	f_{g3} =	f_{g5} =	f_{g7} =	f_{g9} =
Coefficient usileniya, To_{Gi}, dB					
Coefficient distortions of M_{Gi}, dB					

– calculate coefficients distortions V decibels For these harmonics By formula

$$M_{Gi} = K_{Gi} - K_{\max};$$

– quantitatively evaluate existing distortions, do conclusions.

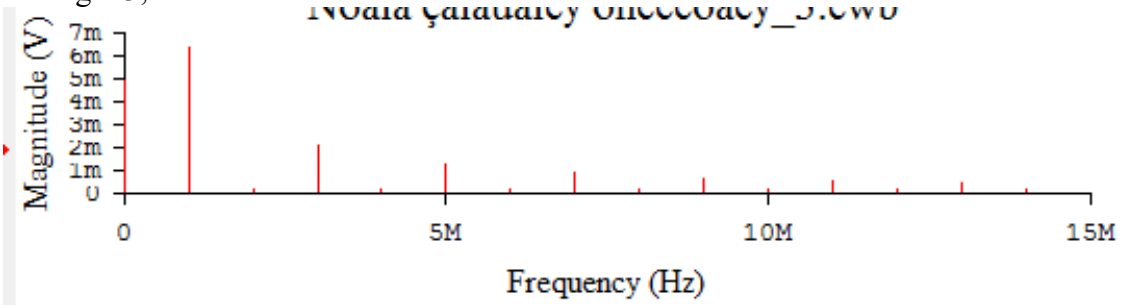
4) Determine the frequency distortion coefficients of the first 5 odd harmonics of rectangular pulses using a Fourier analyzer. To do this, perform the following steps:

– switch switching key ***S2*** V upper position;

– modify the circuit by connecting a 10 µF capacitor between the amplifier output (output of limiter ***VR1***) and switch ***S3 for ease of measurement;***

– install information nodes in the amplifier equivalent circuit being studied; to do this, in the “Circuit” tab, select “Schematic options” and in the dialog box that opens, set the “Show nodes” option;

– Launch the Fourier analyzer via the Analysis menu, in which you set the following options: output node – the node number corresponding to the amplifier input or the output of the ***V2*** generator , the fundamental frequency – 25 kHz, the number of harmonics – 600. The Fourier analyzer will start window, V which will be displayed spectrum input signal, For example, How shown in Fig. 13;



Rice. 13 – Spectrum example input measuring signal

– With help cursors Fourier analyzer produce measurement amplitudes first 5 odd harmonics of the input signal, enter the results in table 5;

Table 5 - Calculation results And measurements.

Harmonic frequency	f_{g1} =	f_{g3} =	f_{g5} =	f_{g7} =	f_{g9} =
Amplitudes harmonics of the input signal, ***Svkh*** $_{Gi}$, mV					
Amplitudes harmonics ideal output signal, ***Свых*** $_{Гi}$, mV					
Amplitudes harmonics distorted output signal, ***S*outh*** $_{Gi}$, mV					
Coefficient distortions ***of M*** $_{Gi}$					

– calculate and enter into table 5 the amplitudes of the harmonics of the output signal for an ideal amplifier without distortion by multiplying the amplitudes of the harmonics of the input signal by the maximum voltage gain of the alternating component, i.e.

$$S_{out\,Gi} = S_{in.Gi} \cdot K_u ;$$

– Using the Fourier analyzer cursors, measure the amplitudes of the first 5 odd harmonics of the distorted output signal ***S*output*** $_{Gi}$, for this in the Fourier analyzer window necessary indicate number weekend node, corresponding exit capacitor inserted into the circuit at the amplifier output. Enter the obtained results into Table 5;

– calculate and enter into table 5 the values of the distortion coefficients of the first 5 odd harmonics of the output signal using the formula

$$M_{Gi} = \frac{S^*_{out\,Gi}}{S_{out.Gi}} ;$$

– quantitatively evaluate existing distortions, compare these results With result-
there, received With help graph plotter, do conclusions.

5) Conduct study frequency properties schemes substitutions amplifier from internal - parameters of the transistor. To do this, perform the following operations:

– return diagram research V original state, having installed switching key ***S4*** to the upper position;

– install capacity collector junction ***Ck*** , V 5 once less than specified;

– set the switching key ***S2*** to the lower position, use the graph plotter to obtain the frequency response of the amplifier and determine the range of amplified frequencies, enter the results into the laboratory report;

– install switching key ***S2*** V upper position, having connected To entrance amplifier source of rectangular pulses, using an oscilloscope obtain oscillograms of the input and output signals, qualitatively evaluate the frequency distortions in the amplifier, and record the results in the laboratory report;

– install capacity collector transition ***Ck*** , V 5 times greater than the specified one;

– set the switching key ***S2*** to the lower position, use the graph plotter to obtain the frequency response of the amplifier and determine the range of amplified frequencies, enter the results into the laboratory report;

– install switching key ***S2*** V upper position, having connected To entrance amplifier source of rectangular pulses, using an oscilloscope obtain oscillograms of the input and output signals, qualitatively evaluate the frequency distortions in the amplifier, and record the results in the laboratory report;

– draw a conclusion about how the frequency properties of the amplifier are affected by the capacitance of the collector junction.

6) Do generalized conclusions By results research, conducted V task 3.

Exercise 4. Study amplitude characteristics amplifier, his sensitive ity, dynamic range And emerging nonlinear distortions.

Statement of the problem and research methodology . The objective of the study of the developed circuit model of the amplifying device is to obtain the most complete information about its amplitude characteristic and the parameters arising from it: sensitivity And dynamic range, V establishment reasons, contributing the occurrence of frequency distortions.

The research methodology consists of determining the reaction (response) of the developed amplifier equivalent circuit to a priori known effects, in the form of a harmonic signal at a fixed frequency, with constant values of the internal parameters of the circuit and changes amplitudes input signal With taking into account availability external And own noises the force of the litel.

As part of this task, the amplitude characteristic of the circuit is measured. substitutions amplifier, definitions threshold sensitivity And dynamic range , and research is also being conducted on how this characteristic affects the nonlinear distortions that occur in the amplifier.

Order execution tasks.

1) Define nominal sensitivity schemes substitutions amplifier. For To do this, perform the following operations:

– modify the circuit by connecting 10 μF capacitors to both inputs of the oscilloscope for ease of measurement;

– set the switching key ***S1*** to the right position, connecting the external noise source ***Vn1*** ;

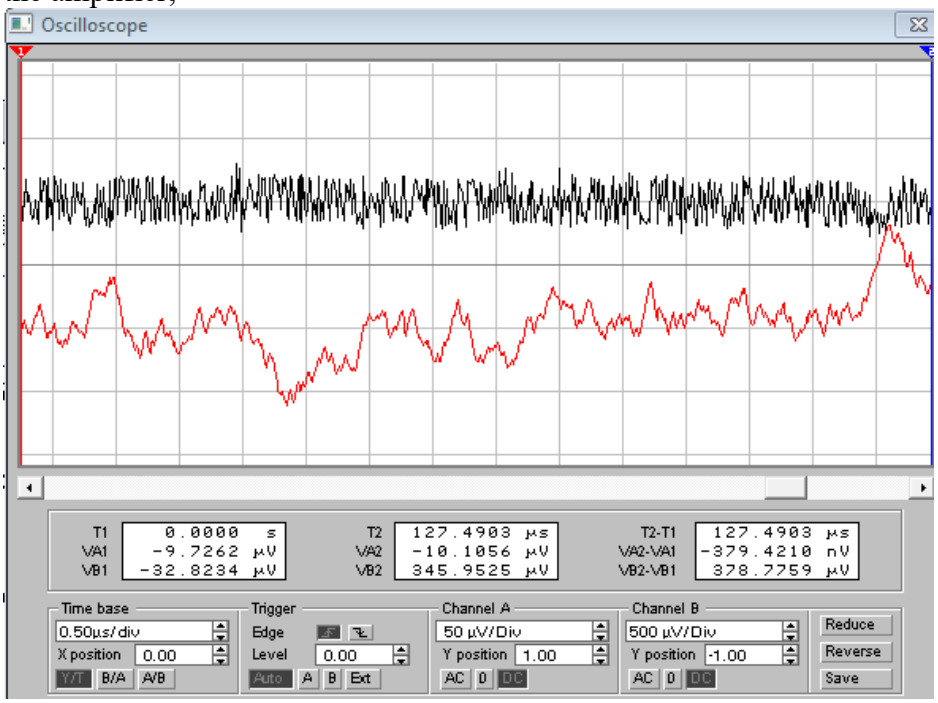
– install V source (generator) signals minimally possible effective voltage equal to 1 μV;

– launch simulator EWB, open oscilloscope And get By Channel One an oscillogram of the additive mixture of signal and noise at the amplifier input, and the resulting output signal on the second channel. Example of an oscillogram shown in Fig. 14. The obtained oscillograms should be included in the report;

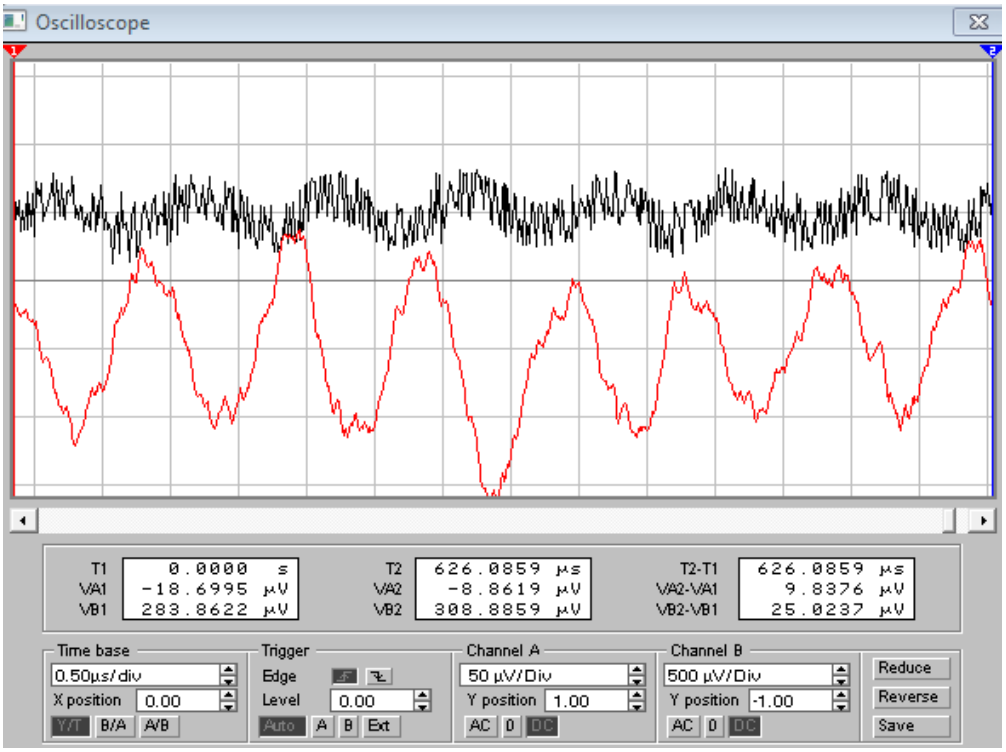
– get With help Fourier analyzer spectrum input And weekend signals, to include them in the report;

– conducted analysis oscillograms And spectra, How input, So And weekend The signal - must show that the signal is not distinguishable from the background noise;

– By increasing the source's effective voltage in 2 μV increments, use an oscilloscope and a Fourier analyzer to accurately detect the signal against the background noise. Threshold sensitivity is defined as the minimum input signal at which the output signal is clearly defined above the noise level, with the input signal and noise levels being equal. An example of threshold sensitivity is shown in the oscillogram. given on rice. 15. Having reached such ratios input signal And noise, as shown on rice. 15, fix V report size current voltage input signal corresponding to the threshold sensitivity of the amplifier;



Rice. 14 - Example oscillograms input And weekend signals, When small input the signal is suppressed (not distinguishable) against the background noise

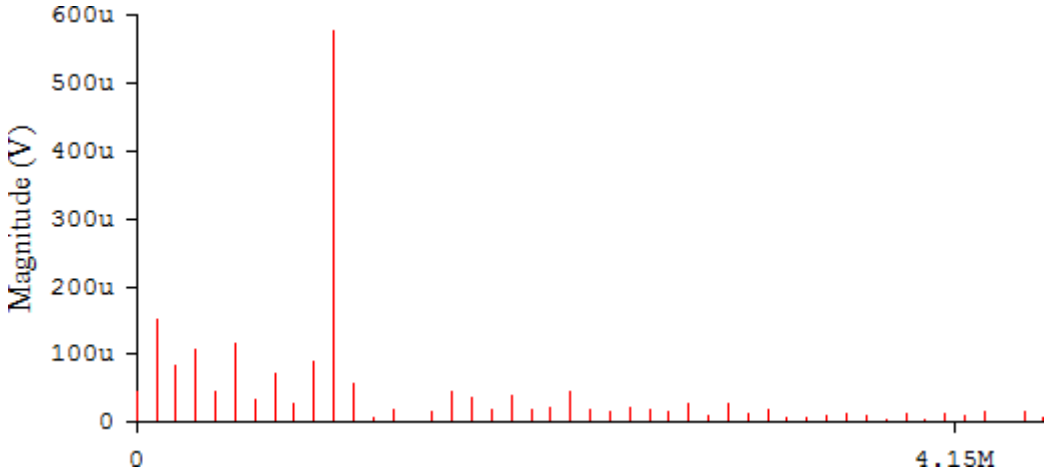


Rice. 15 - Example oscillograms input And weekend signals, When small input the signal is determined at the noise level

– to carry out a quantitative assessment of the possibility of recognizing a signal against a background of noise using the coefficient of harmonic distortion (CHD), determined by the formula

$$K_{\Gamma} = \frac{\sqrt{U_2^2 + U_3^2 + U_4^2 + \ldots + U_n^2 + \ldots}}{U_1},$$

To do this, select 4-5 of the highest amplitude noise harmonics and calculate the THD. Example spectrum weekend signal on background noise, given on rice. 15 shown on rice.
16. For this case KGI approximately equals 0.45;



Rice. 16 - Example spectrum weekend signals on level threshold sensitivity nost

For a qualitative assessment of nonlinear distortions, the following typical values in percentage for THD should be used as a guide: 0% - the signal shape is an ideal sinusoid; up to 3% - the signal shape differs from sinusoidal, but the distortions are not noticeable to the eye; up to 5% - deviation of the signal shape from sinusoidal is noticeable to the eye on the oscillogram; up to 10% - standard (acceptable) level of distortion, noticeable to the ear; approximately 50% - threshold sensitivity of the signal.

– draw a conclusion about the magnitude of the threshold sensitivity of the developed - amplifier replacement circuit.

2) Define And build schedule amplitude characteristics schemes substitutions the force of the litel. For this, sequentially installing current voltage input signal in generator ***Vg*** V view quantities equal threshold sensitivity, then 50 μV, 200 μV, 500 μV, 2 mV, 10 mV, 20 mV, 30 mV, 40 mV perform the following operations:

– for each set input voltage, measure the output voltage using an ***MV5 voltmeter*** and enter it into a spreadsheet;

– build schedule dependencies weekend voltage U_{out} from input voltage U_{in};

– With help graphics define size dynamic range amplifier By given formulas And bring in received results V report

$$D = U_{out.max} / U_{out.min} \quad \text{And} \quad D\,[\,dB\,] = 20 \cdot \lg(U_{out.max} / U_{out.min}),$$

Where $U_{out.max}$ - maximum meaning weekend voltage on linear plot OH,

$U_{out.min}$ - minimum meaning weekend voltage on linear plot OH;

– do conclusions about amplitude characteristics amplifier.

3) Model the nonlinear distortions that occur at the amplifier output and determine their KGI. For this, sequentially installing current voltage input signal in the ***Vg generator*** in the form of values equal to 20 mV, 25 mV, 30 mV, 40 mV, perform the following operations:

– display day off signal on oscilloscope, For Togo, to make sure V volume, that the output signal will begin to be limited in amplitude due to the nonlinearity of the current-voltage characteristic of the transistor,

– using a Fourier analyzer, obtain the spectrum of the output signal, measure the amplitudes of its harmonics and determine the THD;

– do conclusion about that when arise nonlinear distortions.

4) Do generalized conclusions By results research, conducted V task 4.

Exercise 5. (For independent work) Design results research V view report By laboratory work And protect his.

1) Display in the report :

– topic and target work, tasks For research And brief order their execution;

– simulated principled electric scheme replacement of the amplifying device in the form of a U-shaped hybrid circuit;

– results research V view tables With measurements And calculations, graphs;

– oscillograms And spectrograms studied signals;

– conclusions By results execution tasks And V in general By done work.

2) Protect report By done laboratory work, having completed individual for the assignment specified by the teacher, within the framework of the research conducted.

PRACTICAL WORK No. 2

Subject: **STUDY AMPLIFIERS VOLTAGES**

Time – 4 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of amplifiers with various schemes inclusions active element (transistor) With using universal packages of applied computer programs;

– conduct study main parameters And characteristics amplifiers With common emitter (CE), common base (CB) and common collector (CC);

– collection and analysis of information to generate initial data for the design of electronic amplifying devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

During independent work hours in preparation for the PR

1. Theoretical calculation main parameters amplifiers By schemes With about-shimm emitter (OE), general base (ABOUT) And common collector (OK).	**90 min**
Lesson No. 1	**90 min**
Introductory part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
2. Assembly circuit design models amplifiers By schemes With OE, ABOUT And OK.	30 min
3. Study main parameters And characteristics amplifiers By sche-mom with OE, ABOUT And OK.	45 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
3. Study main parameters And amplifier characteristics according to the scheme-mom with OE, ABOUT And OK.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENT

Brief theoretical or reference and information materials

Theoretical knowledge required for practical work information is available: in lectures materials (lecture No. 4); in appendix to this laboratory work; in recommended literature on the academic discipline.

Exercise For preparation To laboratory work:

1. To study the rules and circuit design for constructing amplifiers using circuits with a common emitter , common base and common collector;

2. Analyze fundamental peculiarities And characteristics schemes amplifiers with common emitter, common base and common collector.

3. Master the rules for calculating the main parameters of amplifier circuits with a common emitter , common base and common collector.

4. Perform theoretical calculations in advance during independent work hours amplifiers By schemes With common emitter, base And collector. For this calculate the parameters given in tables 3 and 4 of the practical lesson using the methodology given in the Appendix.

Contents of the practical work performed students V in the course classes

Description laboratory equipment:

– PC for each student;

– program editor schematic modeling Electronics Workbench" (EWB) version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher.

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) At occurrence emergency situations necessary immediately turn off equipment from the power supply networks, report about this to the teacher And act according to him instructions.

6) At fire equipment his necessary immediately de-energize, report about this to the teacher, accept measures By elimination fires And act By instructions pre teacher.

7) Upon completion of work with laboratory equipment (computers) it must be turned off in the established order.

Initial data For modeling and research

Options for tasks for individual modeling and research by students are presented in Table A.

Table A - Options tasks for modeling And research.

Option number	Rb1, kOhm	Rb2, kOhm	Option number	Rb1, kOhm	Rb2, kOhm
1.	101	15	2.	68	22
3.	91	18	4.	68	27
5.	91	22	6.	56	18
7.	82	15	8.	56	24
9.	82	18	10.	51	18
11.	75	15	12.	51	24
13.	75	22	14.	51	30

15.	75	24	16.	47	15
17.	75	27	18.	47	20
19.	68	15	20.	47	33

Tasks to be completed during practical work

Tasks basic level:

1) Execute theoretical calculation main parameters amplifier By scheme With common emitter (during independent work hours).

2) Assemble a circuit model of an amplifier using a common emitter circuit in a computer simulation software package.

3) Conduct study main parameters And characteristics amplifier By scheme with a common emitter.

4) Execute theoretical calculation main parameters amplifier By scheme With general collector (during independent work hours).

5) Assemble a circuit model of an amplifier using a common collector circuit in a computer simulation software package.

6) Conduct study main parameters And characteristics amplifier By scheme with a common collector.

Tasks increased level:

7) Execute theoretical calculation main parameters amplifier By scheme With common base (during independent work hours).

8) Assemble a circuit model of an amplifier using a common base circuit in a computer simulation software package.

9) Conduct study main parameters And characteristics amplifier By scheme with a common base.

Order execution work

Task 3. Study of the main parameters and characteristics of an amplifier using a common emitter circuit

Statement of the research problem : In this task, research is carried out on two modes work preliminary amplifier: without load (idle) and with load ($R_н$ = 360 Ohm). At this To amplifier connects or ideal source signal, whose internal resistance is 0, or a real current source with a resistance of 1 kOhm. The amplifier must provide an output voltage equal to U_{OUTPUT} = 300 mV.

IN task necessary on average frequency f_{cf} = 10 kHz execute next actions:

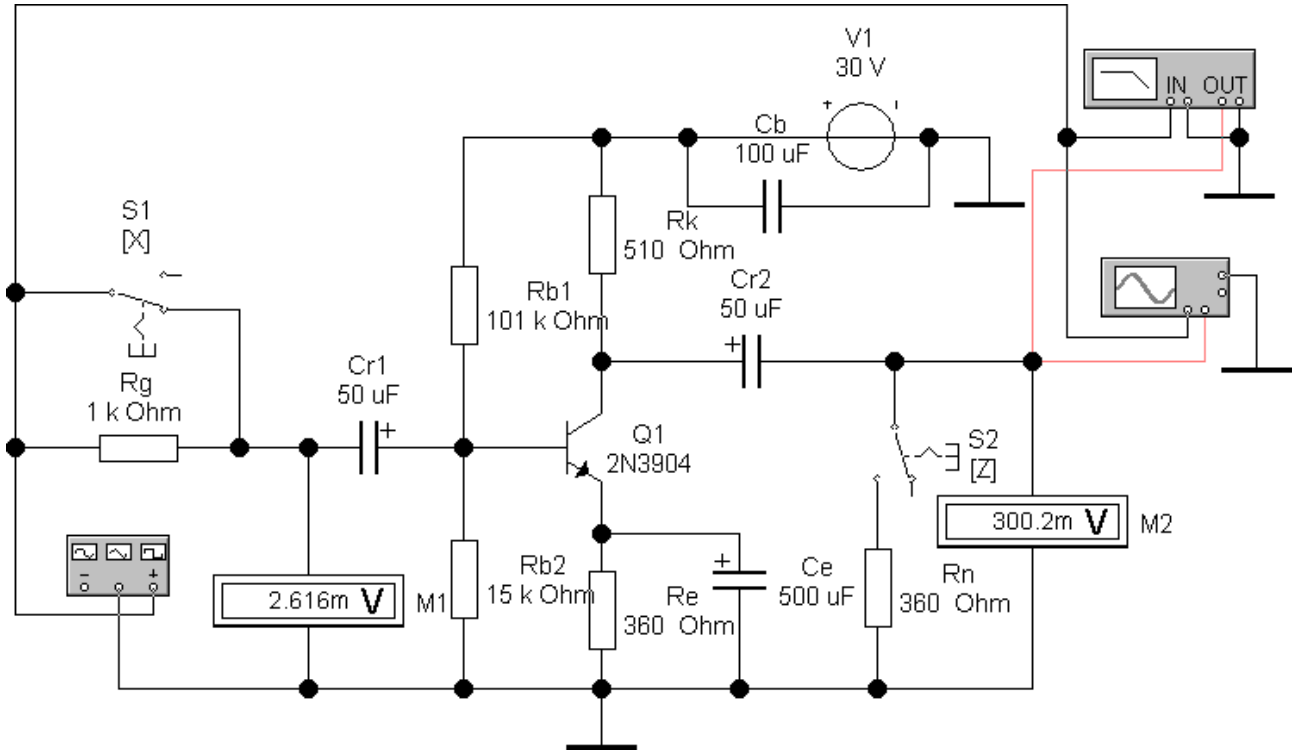
– take off oscillograms input And weekend signal, define introduced they have a phase shift in the output signal,

– remove the amplitude-frequency response (AFR) and phase-frequency response (PFR) of the amplifier, determine the band of amplified frequencies;

– define primary And secondary amplifier parameters ;

– evaluate transmission (amplifying) properties By tension, By current And By power-nost.

For execution tasks 3 necessary ***execute exercise 2*** , those. V software pa-kete computer modeling assemble circuit design model amplifier by scheme with the OE shown in Fig. 1.



Rice. 1 – Schematic diagram amplifier with common emitter

Recommendations By execution tasks:

1) Set the values of the elements in the assembled circuit as shown in Fig. 1, with the exception of the voltage divider resistances ***Rb1*** and ***Rb2*** , the values of which are set according to the specified option. In the function generator, set the input frequency signal 10 kHz, A amplitude ***Eg*** =10 mV. Keys ***S1*** And ***S2*** install V provisions, as shown in Fig. 1.

2) Check performance schemes. For this activate work schemes button located in the upper right corner of the screen. When the circuit is working correctly, the variable voltmeters ***M1*** And ***M2*** they will show respectively values input voltage U_{in} And output voltage U_{out} .

3) To obtain oscillograms, adjust the oscilloscope so that 3–4 oscillation periods are displayed on its screen, and the amplitudes of the input and output signals are approximately equal. Enter the resulting oscillograms into the PZ report. Use the oscillograms to determine the phase shift between the input and output signals.

4) Order actions at removal frequency response And Phase response:

– launch double click left button mice Bode plotter;

– In the dialog box that opens, select the Magnitude operating mode, this means that the Bode plotter will operate in the frequency response meter mode;

– V frame Vertical choose linear scale By axes amplitudes, And install upper and lower threshold values ***F*** = 100 or 500, ***I*** = 0.

– In the Horizontal frame, select the logarithmic scale along the frequency axis, and set the upper and lower threshold values to ***F*** = 10 GHz, ***I*** = 1 Hz.

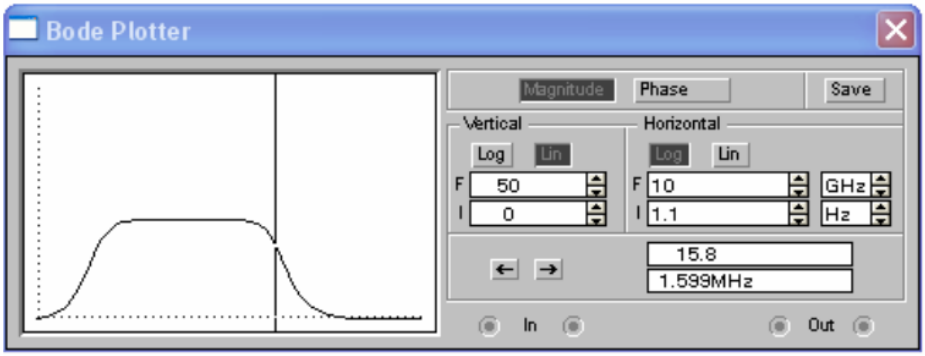
– activate work schemes button, located V right top corner screen; Bode plotter will show the frequency response of the amplifier on its screen (example in Fig. 2);

– bring in received frequency response V report according to PZ ;

– install V Bode plotter operating mode Phase, translating it V in the frequency response meter mode ;

– V frame Vertical For linear scale By axes amplitudes install values the top and bottom thresholds F= -90 degrees, I= -270 degrees;

– bring in received phase response V report according to PZ .



Rice. 2 - Example settings Bode plotter

5) Define strip reinforced frequencies (strip transmission) amplifier. For To do this, perform the following operations:

– In Magnitude mode, set the Bode plotter cursor to the average (working) frequency amplifier, equal 10 kHz, define size coefficient gains By voltage K_{SR} in times;

– Move the Bode plotter cursor to the left to find the lower gain cutoff frequency f_{GPH}, on which coefficient gains To_{SR} decrease on size $\sqrt{2}$ (those. will make up 0.707 from K_{SR});

– by moving the Bode plotter cursor to the right, find the upper limit frequency of the gain f_{GDV}, on which coefficient strengthening $of\ K_{SR}$ decrease on the value of $\sqrt{2}$ (i.e. will make up 0.707 from K_{SR});

– received results bring in V Table 1 report according to PZ ;

– in the Phase operating mode, set the Bode plotter cursor to the amplifier's average (operating) frequency, equal to 10 kHz, and determine the phase shift value φ_{CP} in degrees;

– promoting cursor Bode plotter V left find lower border frequency gains f_{UAH}, on which phase shift φ_{SR} change on size +45 degrees;

– moving the cursor Bode plotter V right find top border frequency gains f_{GRV}, on which phase shift φ_{SR} change on size -45 degrees;

– received results bring in V table 1 report according to PZ.

Table 1 – Results of the frequency response and phase response studies.

Type cascade	Parameter	f_{UAH}, Hz	f_{SR}, kHz	f_{GRV}, MHz
OE	K		10	
	K / K_{SR}	0.707	1	0.707
	φ			
OK	K		10	
	K / K_{SR}	0.707	1	0.707
	φ			
OB	K		10	
	K / K_{SR}	0.707	1	0.707
	φ			

6) Order actions at conducting measurements primary parameters amplifier:

6.1) Close key "X" So, to short-circuit internally resistance generator Rg, thereby having done its equal to zero, as in ideal source of EMF (see Fig. 1).

6.2) Open the key “Z”, disconnecting the load, thereby establishing the idle mode, when $R\ n = \infty$ (see Fig. 1).

6.3) Run the circuit, select the amplitude of the signal voltage E_G in a functional generator, at which the voltage at the output of the amplifier stage will be U_{OUTPUT} = 300 mV.

6.4) Results of measurements of E_G, U_{BX} and U_{EXIT} for this case, the ideal EMF source (Rg = 0) and the disconnected load are entered into table 2.

6.5) the voltage gain ***K , the through gain*** amplification K_E . Received results bring in V table 2. For this take advantage of formulas:

$$K = \frac{U_{out}}{U_{in}},\ K_E = \frac{U_{out}}{E_G}.$$

Table 2 - Results measurements And experimental calculations.

Scheme	**OE without load**		**OE with load**		**OK without load**		**OK with load**		**ABOUT without load**		**ABOUT with load**	
Parameter	Rg=0	Rg= 1 kOhm	Rg=0	Rg= 1 kOhm	Rg=0	Rg= 1 kOhm	Rg=0	Rg= 1 kOhm	Rg=0	Rg = 10 Ohm	Rg=0	Rg = 10 Ohm
E_g, mV												
U_{in}, mV												
U_{out}, mV												
K												
K_E												

6.6) Repeat the measurements with the ***X key open*** , thereby connecting the internal - resistance of the generator Rg = 1.0 kOhm; determine the value of *Eg* at which the output voltage of the amplifier will be U_{OUTPUT} = 300 mV.

6.7) Repeat All measurements for both cases (Rg = 1.0 kOhm and Rg = 0) With connected load R_H = 360 Ohm; For this need to close key ***Z*** by way pressing on the keyboard key of the same name.

6.8) Results measurements E_G , U_{VH} And U_{EXIT} For cases With connected And with the load disconnected R_n enter into table 2.

7) The procedure for carrying out experimental calculations of the primary and secondary - parameters of the amplifier:

7.1) Calculate experimental values input And weekend currents I_{in} And $I_{'m\ out}$, coefficients gains current And power To_I And To_R For situations With real source signal (Rg = 1.0 kOhm) of the connected and disconnected load, investigated in the previous paragraph 6).

For this V package For mathematical And engineering calculations ***In Mathcad Professional*** , enter the initial data for calculations and write down the formulas for calculation:

$$I_{in} = \frac{E_g - U_{in}}{R_g},\ I_{'m\ leaving} = \frac{U_{out}}{R'_n},$$

Where

$$R'_n = \begin{cases} \dfrac{R_{to} R_n}{R_{to} + R_n}, & \text{if } R_n = 360 \text{ Ohm} \\ R_{to}, & \text{if } R_n = \infty \end{cases},$$

$$K_I = \frac{I_{'m\ leaving}}{I_{in}},\ K_P = K \cdot K_I.$$

Received results bring in V Table 3.

Table 3 – Results experimental calculations.

Para meter	Scheme					
	OE without load	**OE with load**	**OK without load**	**OK with load**	**ABOUT without load**	**ABOUT with load**
***I* in**, mA						
***I* outp ut**, mA						
To I						
***K* P**						

7.2) Connect With help keys ***X*** And ***Z*** ko entrance amplifier real source signal With internal resistance ***Rg*** , A to the exit – load, having active resistance ***R* n** .

7.3) Calculate the experimental values of secondary parameters for the established operating mode. parameters R_{in} , R_{out} , h_{11} And Y_{22} amplifier, taking advantage of data from tables 2 And 3. For this V package for mathematical And engineering ***Mathcad*** calculations ***Professional*** enter the initial data for calculations and write down the formulas for calculations:

– input And output resistances

$$R_{\text{in}} = \frac{U_{\text{in}}}{I_{\text{in}}}, \quad R_{\text{out}} = R_{\text{Ohm}}\Big|_{n=360} \left(\frac{U_{\text{out}\,R_H=\infty}}{U_{\text{out}\,R_H=360}} - 1 \right);$$

– own input resistance amplifying element

$$h_{11} = \frac{R_{\text{in}} R_{\text{b}}}{R_{\text{b}} - R_{\text{in}}}, \text{ where } R_{\text{б}} = \frac{Rb1 \cdot Rb2}{Rb1 + Rb2};$$

– day off conductivity amplifying element (transistor)

$$Y_{22} = \frac{R_{\text{to}} - R_{\text{out}}}{R_{\text{out}} R_{\text{to}}}.$$

Received results bring in V table 4.

Table 4 - Results experimental calculations.

Para meter	Scheme					
	OE without load	**OE with load**	**OK without load**	**OK with load**	**ABOUT without load**	**ABOUT with load**
R_{in}, Ohm						
R_{out}, Ohm						
h_{11}, Ohm						
Y_{22}, 1/Ohm						

8) Conduct an analysis of the transfer (amplification) properties of the amplifier stage for the case of connecting to the input of a real generator. To do this, enter the previously obtained - coefficients transmissions V table 5. Compare their quantities For various modes work And for various connection schemes, formulate conclusions.

Table 5 - Comparative analysis transmission properties amplifying stages.

Para meter	**Scheme**					
	OE without load	**OE with load**	**OK without load**	**OK with load**	**ABOUT without load**	**ABOUT with load**
K						
K_E						
K_I						
K_P						

9) Do conclusions By results conducted research.

Task 6. Study of the main parameters and characteristics of an amplifier using a common collector circuit.

Statement of the research problem : In this task, research is carried out on two modes work coordinating amplifier: without loads (on single on the move) And With load ($R_н$ = 360 Ohm). In this case, either an ideal signal source with an internal resistance of 0, or a real current source with a resistance of 1 kOhm is connected to the amplifier. The amplifier must provide an output voltage equal to U_{OUTPUT} = 300 mV.

IN task necessary on average frequency f_{cf} = 10 kHz execute next actions:

– take off oscillograms input And weekend signal, define introduced they have a phase shift in the output signal,

– remove the amplitude-frequency response (AFR) and phase-frequency response (PFR) of the amplifier, determine the band of amplified frequencies;

– define primary And secondary amplifier parameters ;

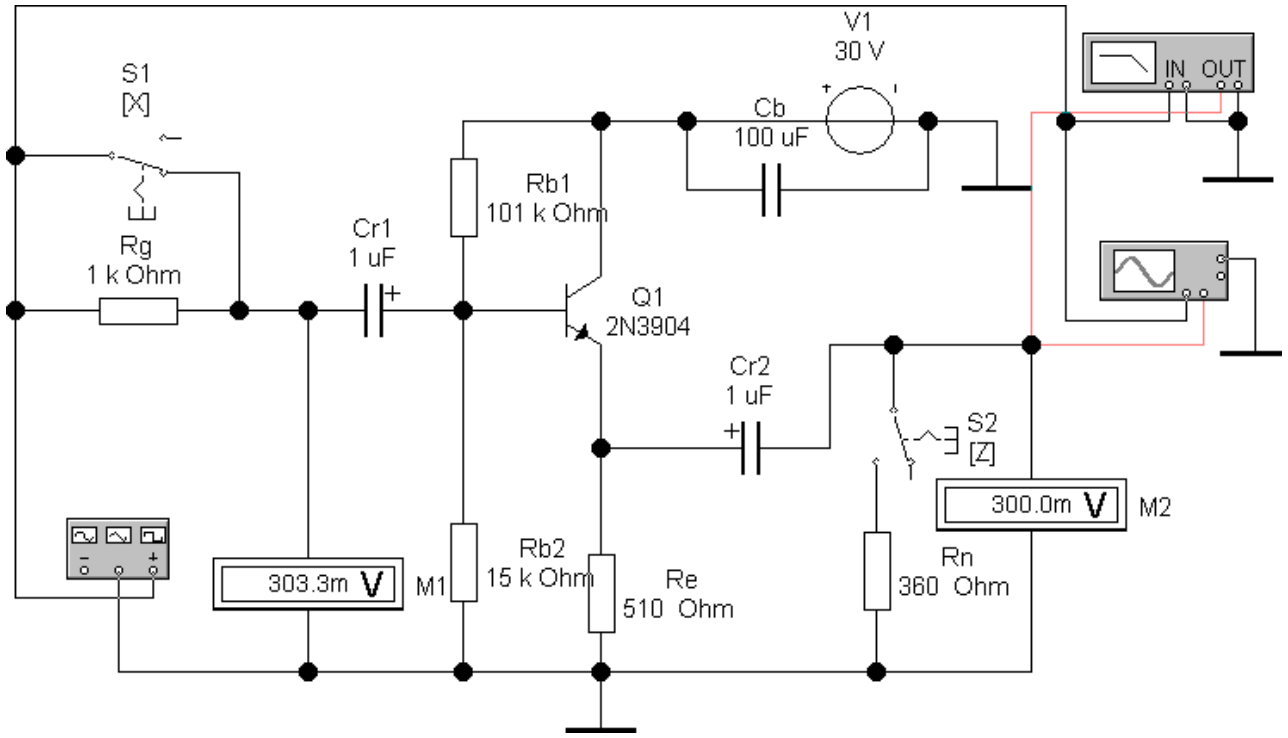
– evaluate transmission (amplifying) properties By tension, By current And By power-nost.

For execution tasks 6 necessary ***execute exercise 5*** , those. V software pa-kete computer modeling assemble circuit design model amplifier by scheme with OK, shown in Fig. 3.

Recommendations By execution tasks:

1) Set the values of the elements in the assembled circuit as shown in Fig. 1, with the exception of the voltage divider resistors ***Rb1*** and ***Rb2*** , the values of which are set according to the specified option. In the function generator, set the input signal frequency to 10 kHz and the amplitude ***Eg*** = 450 mV. Set the switches ***S1*** and ***S2*** to the positions shown in Fig. 3.

2) Check performance schemes. For this activate work schemes button located in the upper right corner of the screen. When the circuit is working correctly, the variable voltmeters ***M1*** And ***M2*** they will show respectively values input voltage U_{in} And output voltage U_{out} .



Rice. 3 – Schematic diagram amplifier with common collector

3) To obtain oscillograms, adjust the oscilloscope so that 3–4 oscillation periods are displayed on its screen, and the amplitudes of the input and output signals are approximately equal. Enter the resulting oscillograms into the PZ report. Use the oscillograms to determine the phase shift between the input and output signals.

4) Order actions at removal frequency response And Phase response:

– launch double click left button mice Bode plotter;

– In the dialog box that opens, select the Magnitude operating mode, this means that the Bode plotter will operate in the frequency response meter mode;

– V frame Vertical choose linear scale By axes amplitudes, And install values of the upper and lower thresholds ***F*** =1, ***I*** =0.

– In the Horizontal frame, select the logarithmic scale along the frequency axis, and set the upper and lower threshold values to ***F*** = 900 GHz, ***I*** = 1 Hz.

– activate work schemes button, located V right top corner screen; Bode plotter on in his own screen will show frequency response amplifier; bring in received frequency response V report according to PZ;

– install V Bode plotter operating mode Phase, translating it V in the frequency response meter mode ;

– V frame Vertical For linear scale By axes amplitudes install values the upper and lower thresholds F= 90 degrees, I= -90 degrees;

– bring in received phase response V report according to PZ .

5) Define strip reinforced frequencies (strip transmission) amplifier. For To do this, perform the following operations:

– In Magnitude mode, set the Bode plotter cursor to the average (working) frequency amplifier, equal 10 kHz, define size coefficient gains By voltage ***K*** **SR** in times;

– Move the Bode plotter cursor to the left to find the lower gain cutoff frequency ***f*** **ГРН** , on which coefficient gains ***To*** **SR** decrease on size $\sqrt{2}$ (those. will make up 0.707 from ***K*** **SR**);

– by moving the Bode plotter cursor to the right, find the upper limit frequency of the gain f_{GDV}, on which coefficient strengthening *of* K_{SR} decrease on the value of $\sqrt{2}$ (i.e. will make up 0.707 from K_{SR});

– received results bring in V Table 1 report according to PZ ;

– in the Phase operating mode, set the Bode plotter cursor to the amplifier's average (operating) frequency, equal to 10 kHz, and determine the phase shift value φ_{CP} in degrees;

– promoting cursor Bode plotter V left find lower border frequency gains f_{UAH}, on which phase shift φ_{SR} change on size +45 degrees;

– moving the cursor Bode plotter V right find top border frequency gains f_{GRV}, on which phase shift φ_{SR} change on size -45 degrees;

– received results bring in V Table 1 report according to PZ .

6) Order actions at conducting measurements primary parameters amplifier:

6.1) Close key "X" So, to short-circuit internally resistance generator Rg, thereby making its equal to zero, as V ideal source EMF (see fig. 3).

6.2) Open the key “Z”, disconnecting the load, thereby setting the idle mode, when $R_{\text{n}} = \infty$ (see Fig. 3).

6.3) Run the circuit, select the amplitude of the signal voltage E_G in a functional generator, at which the voltage at the output of the amplifier stage will be U_{OUTPUT} = 300 mV.

6.4) Results of measurements of E_G, U_{BX} and U_{EXIT} for this case the ideal source EMF (Rg = 0) and disconnected load are entered into table 2.

6.5) the voltage gain ***K , the through gain*** amplification K_E . Received results bring in V table 2. For this take advantage of formulas:

$$K = \frac{U_{\text{out}}}{U_{\text{in}}},\ K_{\text{E}} = \frac{U_{\text{out}}}{E_{\text{G}}}.$$

6.6) Repeat the measurements with the ***X key open*** , thereby connecting the internal - resistance of the generator Rg = 1.0 kOhm; determine the value of *Eg* at which the output voltage of the amplifier will be U_{OUTPUT} = 300 mV.

6.7) Repeat All measurements for both cases (Rg = 1.0 kOhm and Rg = 0) With connected load R_H = 360 Ohm; For this need to close key Z by way pressing on the keyboard key of the same name.

6.8) Results measurements E_G, U_{VH} And U_{EXIT} For cases With connected And with the load disconnected R_{n} enter into table 2.

7) The procedure for carrying out experimental calculations of the primary and secondary - parameters of the amplifier:

7.1) Calculate experimental values input And weekend currents I_{in} And $I'_{m\ out}$, current and power gain factors K_I and K_R for all four situations examined in the previous paragraph 6).

the Mathcad Professional package for mathematical and engineering calculations and write down the formulas for the calculation:

$$I_{\text{in}} = \frac{E_{\text{g}} - U_{\text{in}}}{R_{\text{g}}},\ I'_{\text{m leaving}} = \frac{U_{\text{out}}}{R'_{\text{n}}},$$

Where

$$R'_{\text{n}} = \begin{cases} \dfrac{R_{\text{e}} R_{\text{H}}}{R_{\text{e}} + R_{\text{H}}}, & \text{if } R_{\text{n}} = 360\ \text{Ohm} \\ R_{\text{e}}, & \text{if } R_{\text{n}} = \infty \end{cases},$$

$$K_I = \frac{I'_{\text{m leaving}}}{I_{\text{in}}},\ K_{\text{P}} = K \cdot K_I.$$

Received results bring in V table 3.

7.2) Connect With help keys ***X*** And ***Z*** ko entrance amplifier source signal With internal - resistance ***Rg ,*** and to the output – a load with active resistance ***Rn .***

7.3) Calculate the experimental values of secondary parameters for the established operating mode. parameters R_{in}, R_{out}, h_{11} And Y_{22} amplifier, taking advantage of data from tables 2 And 3. For this V package for mathematical And engineering ***Mathcad*** calculations ***Professional*** enter the initial data for calculations and write down the formulas for calculations:

– input And output resistances

$$R_{in} = \frac{U_{in}}{I_{in}}, \quad R_{out} = R_{Ohm}\Big|_{h=360}\left(\frac{U_{out\,R_H=\infty}}{U_{out\,R_H=360}} - 1\right);$$

– own input resistance amplifying element

$$h_{11} = \frac{R_{in} R_b}{R_b - R_{in}}, \quad \text{where} \quad R_б = \frac{Rb1 \cdot Rb2}{Rb1 + Rb2};$$

– day off conductivity amplifying element (transistor)

$$Y_{22} = \frac{R_e - R_{out}}{R_{out} R_e}.$$

Received results bring in V table 4.

8) Conduct an analysis of the transfer (amplification) properties of the amplifier stage for the case of connecting to the input of a real generator. To do this, enter the previously obtained - coefficients transmissions V table 5. Compare their quantities For various modes work And for various connection schemes, formulate conclusions.

9) Do conclusions By results conducted research.

Task 9. Study of the main parameters and characteristics of an amplifier using a common base circuit.

Statement of the research problem : In this task, research is carried out on two modes work coordinating amplifier: without loads (on single on the move) And With load (***Rн*** = 360 Ohm). In this case, either an ideal signal source or an internal one is connected to the amplifier. resistance whom equals 0, or real source voltage With resistance of 10 ohms. The amplifier must provide an output voltage equal to U_{OUTPUT} = 300 mV.

IN task necessary on average frequency f_{cf} = 10 kHz execute next actions:

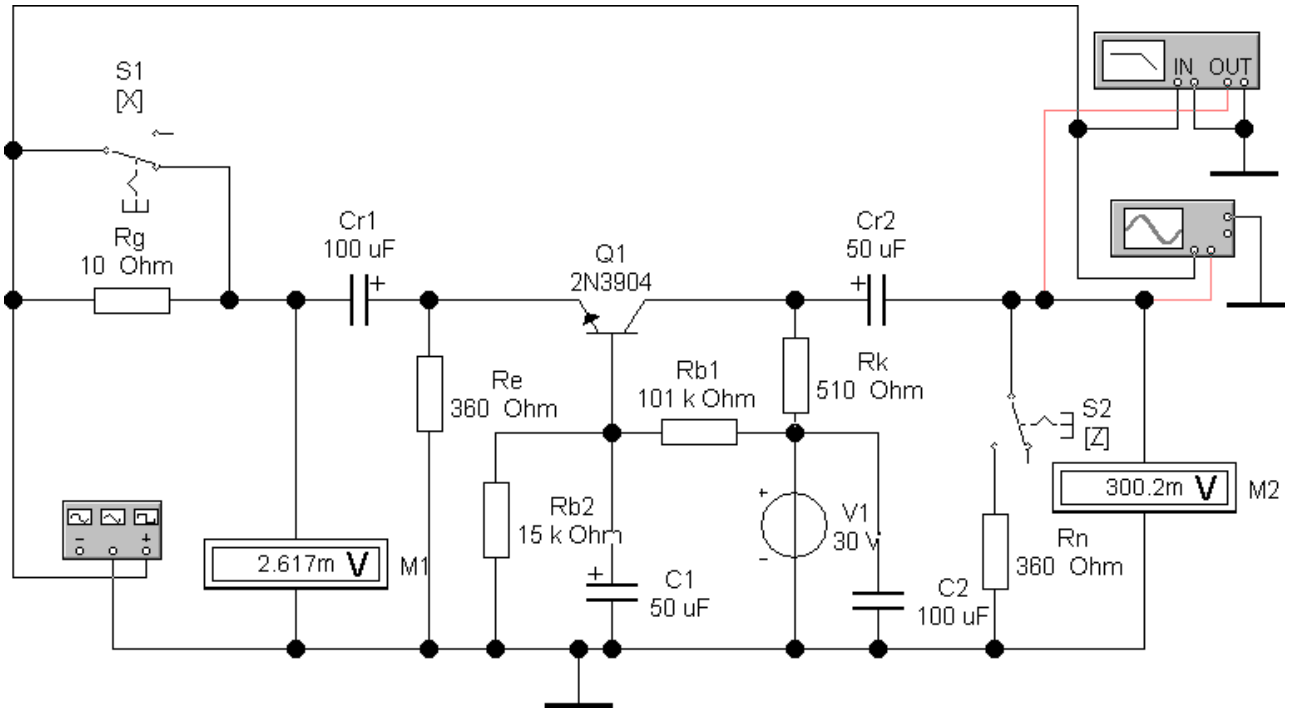
– take off oscillograms input And weekend signal, define introduced they have a phase shift in the output signal,

– remove the amplitude-frequency response (AFR) and phase-frequency response (PFR) of the amplifier, determine the band of amplified frequencies;

– define primary And secondary amplifier parameters ;

– evaluate transmission (amplifying) properties By tension, By current And By power- nost.

For execution tasks 9 necessary ***execute exercise 8*** , those. V software pa- kete computer modeling assemble circuit design model amplifier by scheme with the OB shown in Fig. 4.



Rice. 4 – Schematic diagram amplifier with common base

Recommendations By execution tasks:

1) Set the values of the elements in the assembled circuit as shown in Fig. 1, with the exception of the voltage divider resistances ***Rb1*** and ***Rb2*** , the values of which are set according to the specified option. Note that the internal resistance of the generator has changed and is now equal to 10 ohms. In the function generator, set the frequency input signal 10 kHz, A amplitude ***Eg*** =450 mV. Keys ***S1*** And ***S2*** install V positions as shown in Fig. 4.

2) Check performance schemes. For this activate work schemes button located in the upper right corner of the screen. When the circuit is working correctly, the variable voltmeters ***M1*** And ***M2*** they will show respectively values input voltage U_{in} And output voltage U_{out} .

3) To obtain oscillograms, adjust the oscilloscope so that 3–4 oscillation periods are displayed on its screen, and the amplitudes of the input and output signals are approximately equal. Enter the resulting oscillograms into the PZ report. Use the oscillograms to determine the phase shift between the input and output signals.

4) Order actions at removal frequency response And Phase response:

– launch double click left button mice Bode plotter;

– In the dialog box that opens, select the Magnitude operating mode, this means that the Bode plotter will operate in the frequency response meter mode;

– V frame Vertical choose linear scale By axes amplitudes, And install upper and lower threshold values ***F*** = 100 or 500, ***I*** = 0.

– In the Horizontal frame, select the logarithmic scale along the frequency axis, and set the upper and lower threshold values to ***F*** = 10 GHz, ***I*** = 1 Hz.

– activate work schemes button, located V right top corner screen; Bode plotter on in his own screen will show frequency response amplifier; bring in received frequency response V report according to PZ;

– install V Bode plotter operating mode Phase, translating it V in the frequency response meter mode ;

– V frame Vertical For linear scale By axes amplitudes install values the upper and lower thresholds F= 90 degrees, I= -180 degrees;

– bring in received phase response V report according to PZ .

5) Define strip reinforced frequencies (strip transmission) amplifier. For To do this, perform the following operations:

– In Magnitude mode, set the Bode plotter cursor to the average (working) frequency amplifier, equal 10 kHz, define size coefficient gains By voltage K_{SR} in times;

– Move the Bode plotter cursor to the left to find the lower gain cutoff frequency $f_{ГРН}$, on which coefficient gains To_{SR} decrease on size $\sqrt{2}$ (those. will make up 0.707 from K_{SR});

– by moving the Bode plotter cursor to the right, find the upper limit frequency of the gain f_{GDV}, on which coefficient strengthening $of\ K_{SR}$ decrease on the value of $\sqrt{2}$ (i.e. will make up 0.707 from K_{SR});

– received results bring in V Table 1 report according to PZ ;

– in the Phase operating mode, set the Bode plotter cursor to the amplifier's average (operating) frequency, equal to 10 kHz, and determine the phase shift value φ_{CP} in degrees;

– promoting cursor Bode plotter V left find lower border frequency gains f_{UAH}, on which phase shift φ_{SR} change on size +45 degrees;

– moving the cursor Bode plotter V right find top border frequency gains f_{GRV}, on which phase shift φ_{SR} change on size -45 degrees;

– received results bring in V Table 1 report according to PZ .

6) Order actions at conducting measurements primary parameters amplifier:

6.1) Close key "X" So, to short-circuit internally resistance generator Rg, thereby making its equal to zero, as V ideal source EMF (see Fig. 3).

6.2) Open the key “Z”, disconnecting the load, thereby setting the idle mode, when $R_{\text{n}} = \infty$ (see Fig. 3).

6.3) Run the circuit, select the amplitude of the signal voltage E_G in a functional generator, at which the voltage at the output of the amplifier stage will be U_{OUTPUT} = 300 mV.

6.4) Results of measurements of E_G, U_{BX} and U_{EXIT} for this case the ideal source EMF (Rg = 0) and disconnected load are entered into table 2.

6.5) the voltage gain ***K , the through gain*** amplification K_E. Received results bring in V table 2. For this take advantage of formulas:

$$K = \frac{U_{\text{out}}}{U_{\text{in}}},\ K_{\text{E}} = \frac{U_{\text{out}}}{E_{\text{G}}}.$$

6.6) Repeat the measurements with the ***X key open*** , thereby connecting the internal - resistance of the generator Rg = 10 Ohm; determine the value of *Eg* at which the output voltage of the amplifier will be U_{OUTPUT} = 300 mV.

6.7) Repeat All measurements For both cases (Rg = 10 Ohm And Rg = 0) With connected load $Rн$ = 360 Ohm; to do this, close the key Z by pressing the keyboard key of the same name.

6.8) Results measurements E_G, U_{VH} And U_{EXIT} For cases With connected And with the load disconnected R_{n} enter into table 2.

7) The procedure for carrying out experimental calculations of the primary and secondary - parameters of the amplifier:

7.1) Calculate experimental values input And weekend currents I_{in} And $I_{'m\ out}$, current and power gain factors K_I and K_R for all four situations examined in the previous paragraph 6).

the Mathcad Professional package for mathematical and engineering calculations and write down the formulas for the calculation:

$$I_{\text{in}} = \frac{E_{\text{g}} - U_{\text{in}}}{R_{\text{g}}}, \quad I_{\text{'m leaving}} = \frac{U_{\text{out}}}{R'_{\text{n}}},$$

Where

$$R'_{\text{n}} = \begin{cases} \dfrac{R_{\text{to}} R_{\text{n}}}{R_{\text{to}} + R_{\text{n}}}, & \text{if } R_{\text{n}} = 360 \text{ Ohm} \\ R_{\text{to}}, & \text{if } R_{\text{n}} = \infty \end{cases},$$

$$K_I = \frac{I_{\text{'m out}}}{I_{\text{'m leaving}} + I_{\text{in}}}, \quad K_{\text{P}} = K \cdot K_I.$$

Received results bring in V Table 3.

7.2) Connect With help keys ***X*** And ***Z*** ko entrance amplifier source signal With internal - resistance ***Rg ,*** and to the output – a load with active resistance ***Rn .***

7.3) Calculate the experimental values of secondary parameters for the established operating mode. parameters R_{in}, R_{out}, h_{11} And Y_{22} amplifier, taking advantage of data from tables 2 And 3. For this V package for mathematical And engineering ***Mathcad*** calculations ***Professional*** enter the initial data for calculations and write down the formulas for calculations:

– input And output resistances

$$R_{\text{in}} = \frac{U_{\text{in}}}{I_{\text{in}}}, \quad R_{\text{out}} = R_{\text{h}} \Big|_{h = 360 \text{ Ohm}} \left(\frac{U_{\text{out}\,R_{\text{H}} = \infty}}{U_{\text{out}\,R_{\text{H}} = 360}} - 1 \right);$$

– own input resistance amplifying element

$$h_{11} = \frac{R_{\text{in}} R_{\text{e}}}{R_{\text{e}} - R_{\text{in}}};$$

– day off conductivity amplifying element (transistor)

$$Y_{22} = \frac{R_{\text{to}} - R_{\text{out}}}{R_{\text{out}} R_{\text{to}}}.$$

Received results bring in V table 4.

8) Conduct analysis transmission (amplifying) properties amplifying cascade. For this contribute received previously coefficients transmissions V table 5. Compare their quantities for different operating modes and for different connection schemes, formulate conclusions.

9) Do conclusions By results conducted research.

<u>Task 10. (for independent work)</u> Present the research results in the form of a laboratory report and defend it.

1) IN display the report :

– topic and target work, tasks For research And brief order their execution;

– simulated V editor schematic modeling basic electrical circuit diagrams of amplifiers with OE, OK and OB;

– oscillograms input and weekend signals;

– graphs frequency response And phase response With results measurements border frequencies stripes gains;

– research results in the form of tables with measurements and calculations of the specified primary and secondary parameters of the amplifiers;

– conclusions By results execution tasks And V in general By work done .

2) Protect report By done laboratory work, having completed individual for the assignment specified by the teacher, within the framework of the research conducted.

Control questions For preparation To protection:

1. Please explain, What means term "general" on specific methods inclusions UE: OE, OB, OK.
2. Draw the circuit diagrams of the amplifier stages on the UE connected with the EO, OB, and OK. Explain the purpose of the circuit elements.
3. Provide a general description of the three main switching methods. Compare the following parameters: K, Ke, Ki, Kp, Rin, Rout, fgr.lower, fgr.upper.
4. Please explain, Why at inclusion UE By schemes ABOUT And OK Not is happening inverting the input signal.
5. Please explain, Why at inclusion UE By scheme OE observed inverting the input signal.
6. Give a definition of the lower and upper cutoff frequencies of the amplifier stage $f_{gr.lower}$, $f_{gr.upper}$. How are they determined in the amplifier stage?
7. Please explain, Why UE at inclusion With ABOUT Not Maybe strengthen current signal?
8. Please explain, Why UE at inclusion With OK Not Maybe strengthen voltage signal?
9. Please explain, Why at inclusion UE By scheme With OE has place gain How both current and signal voltage?
10. Which of the three connection schemes The UE allows to obtain the highest gain power?
11. Which elements V scheme resistor cascade limit size input resistance ? Explain the difference between Rвх and h11.
12. Please explain difference between Rout And Y22.
13. Tell me about the methodology measurements of Rвх and Rout.
14. Tell me about the methodology frequency response removal cascade.

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 3

Subject: **STUDY INFLUENCES NEGATIVE FEEDBACK CONNECTIONS ON CHARACTERISTICS REINFORCEMENT DEVICES**

Time – 4 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of amplifiers with various types of negative feedback (NFB) using universal software packages;

– conduct study influences various species OOS on main characteristics and parameters of a common emitter (CE) amplifier;

– collection and analysis of information to generate initial data for the design of electronic amplifying devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Assembly circuit design models amplifier By scheme With OE With various species OOS.	25 min
2. Study useful properties OOS.	50 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	90 min
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
3. Study influences OOS on amplifying properties And frequency Ha-characteristics amplifier.	25 min
4. Study influences OOS on input And weekend resistance usi-litel.	20 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

Feedback is the connection between circuits in an amplifying device in which signal energy is transferred in the direction opposite to the normal, i.e. from the output to the input.

IN amplifying devices wide applies negative OOS With the purpose of: a) reducing nonlinear distortions and interference;

b) reduction of linear (otherwise - frequency And transient) distortions;

V) increase stability parameters at impact on amplifier destabilizing factors (changes in ambient temperature, supply voltage, etc.), d) change in the desired direction of the input or output resistance of the amplifier calf.

OOS gives so big positive effect, What her apply, despite on That, What at this is decreasing coefficient gain.

The amplifier and the feedback circuit form a closed structure called a feedback loop .

The signal transmission coefficient along the feedback loop is called **the loop gain T (or return ratio)** . To determine the loop gain, the feedback loop in an arbitrary place (more often on at the entrance amplifier) tear apart, on exit open loops The resistance ***Rвx*** , which was connected to the break points before the loop opening operation, is included, and the voltage or current transfer coefficient is found for the resulting circuit. This will be the gain $T = \beta \cdot K$.

Under returnable difference (or depth OS) understood magnitude

$$F = 1 - T .$$

This indicator shows, How are changing many indicators amplifying devices from the introduction of OS (Ke, q, Kg, etc.).

Depending on the sign of the real part of ***T*** at the operating frequencies, a distinction is made between ***positive and negative feedback*** . With positive feedback, the real part ***of T*** is positive. With negative feedback, the return voltage ***Uos*** is out of phase with ***Uin*** , and the signals from the signal source and from the feedback circuit at the amplifier input are subtracted. This is what determines the name negative feedback. If in the operating range frequencies ***T*** Not depends from frequencies, That OOS it's called ***frequency-independent*** . IN Otherwise , the OOS is ***frequency-dependent .***

IN dependencies from devices formations OOS on exit amplifier distinguish the following types of feedback: current, voltage and combined output.

With current-biased feedback, the feedback voltage is proportional to the output current. Current-biased feedback is typically achieved by connecting a resistor in series with the load in the amplifier's output current circuit .

At OOS By voltage voltage OS proportionally weekend voltage. To obtain such feedback, you can use a resistor divider, transformer, or autotransformer.

At combined By exit OOS voltage OS contains two components. One of them proportional to the output current, and other - weekend tension.

Figure 1 of the laboratory work shows all three schemes for generating feedback at the amplifier output:

– OOS By voltage - voltage OS, proportional weekend voltage is removed from the resistor (load) R_{to} and through a 1.9 kOhm resistor is fed to the amplifier input using switch “D” - the switch is closed;

– frequency-independent feedback for current - the feedback voltage is taken from the resistor R_e , connected in series with the load R_k (switches “A”, “B”, “C” and “D” are open);

– frequency-dependent OOS By current - voltage OS is being removed With resistor R_e, connected in series with the load R_k (switch "D" is open, and one of the switches "B" or "C" is closed;

– combined output of the OOS - they work simultaneously both schemes for the formation - of environmental protection systems.

IN dependencies from devices input OS distinguish next types OS: serial , parallel and combined by input.

With serial feedback, the feedback voltage is applied to the amplifier input in series with the signal.

With parallel feedback, the feedback voltage is supplied to the amplifier input in parallel with the signal.

With combined feedback at the input, the communication signal contains two components, one of which is which is introduced on entrance amplifier sequentially With source signal, A other - in parallel.

Figure 1 of the laboratory work shows all three circuits for generating feedback at the amplifier input:

– parallel feedback – the feedback voltage is fed through a 1.9 kOhm resistor to the amplifier input (using switch “D” – the switch is closed) in parallel with the signal;

– series feedback – the feedback voltage taken from the resistor $R_э$ is fed to the amplifier input in series with the signal (capacitor “C” is disconnected);

– - combined By entrance OOS - they work simultaneously both For a

complete characteristic of an amplifier with negative feedback, it is necessary

to specify:

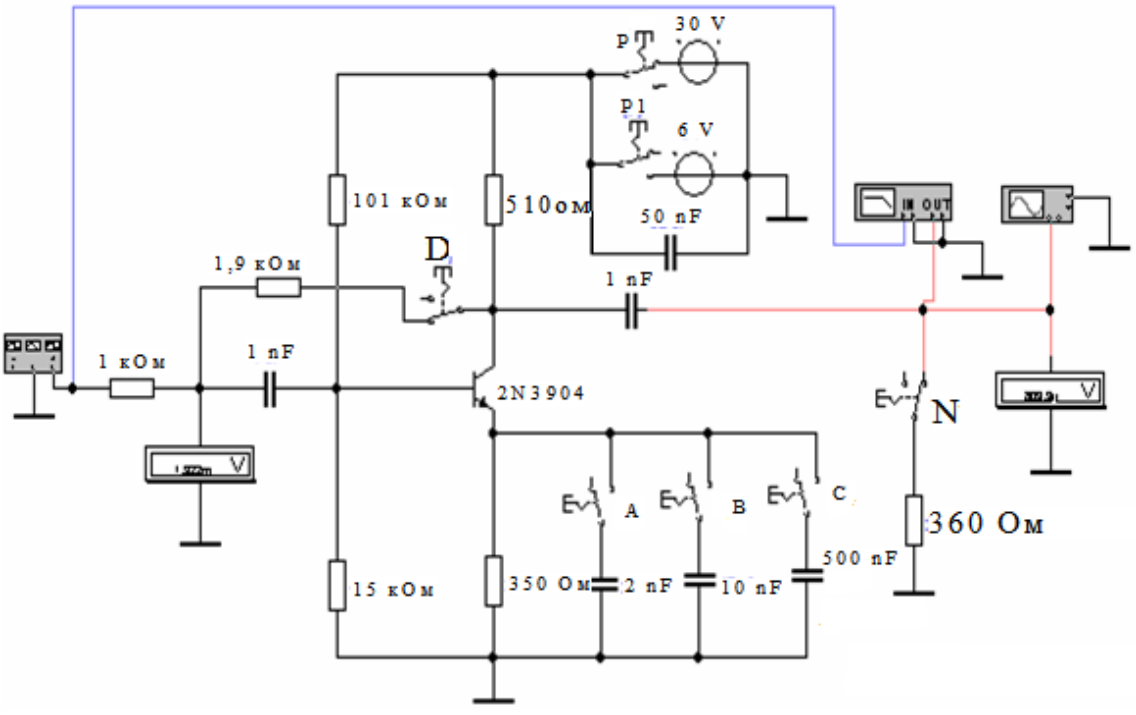
1) way introduction of OS voltage at its entrance;

2) sign ;

3) way receipt voltage OS on exit amplifier.

IN scheme drawing 1 laboratory work, like this in this way, given three schemes OS:

- parallel OOS By tension;
- consistent OOS by current;
- combined By entrance of the OOS, combined by exit.



Drawing 1- Fundamental scheme amplifying devices

Influence OS on coefficients gains Not depends from method receipt signal OS, and is determined only by the method of introducing the OS signal to the amplifier input.

With series feedback , the input circuit current, and therefore ***the current gain*** **, does not** ***change*** ; voltages are added together. If the feedback is negative, the feedback signal is subtracted from the signal source voltage, and ***the voltage gain decreases*** . With positive feedback, on the contrary, the voltage gain increases.

At parallel OS voltage on at the entrance amplifier, A Means And ***coefficient amplification amplifier By voltage Not are changing*** . It's changing coefficient gains By current. If the feedback is negative, the feedback current is subtracted from the current from the signal source, and ***the current gain decreases*** . With positive feedback, on the contrary, the current gain increases.

With a combined feedback at the input, the serial feedback component only affects on coefficient gains By tension, A component parallel OS — only on the current gain.

At OOS All coefficients gains are decreasing , A at POS - are increasing.

Through coefficient gains at any method introduction OS is changing the same thing **.** The formula used for calculation is

$$Keoc = \frac{Ke}{F}, \quad (1)$$

Where - ***Keos*** through coefficient gains With taking into account OS; ***Ke*** through coefficient gain before the introduction of OS, ***F*** is the depth of OS.

Important useful property OOS - decrease instability parameters strengthening **,** and in first queue instability through coefficient gains, at exposure to destabilizing factors.

Relative instability through coefficient gains Can calculate based on two values of this indicator obtained under different conditions, using the formula

$$q = \frac{\Delta Ke}{Ke} = \frac{Ke1 - Ke2}{Ke1}, \quad (2)$$

Where ***Ke1*** And ***Ke2*** - through coefficients gains, For example, at change supply voltage.

From introduction OOS instability gains changes according to the formula

$$q_{eoc} = \frac{q_e}{F}. \quad (3)$$

With negative feedback, $F > 1$, instability decreases. Physically, this is explained by the fact that, for example, when the gain increases under the influence of any destabilizing factors, the signal on exit amplifier increases. This leads To increase signal OS. At this from signal from source subtracted more signal OS, signal on at the entrance amplifying parts of the circuit decreases, What leads To reduction weekend signal. At POS vice versa, the gain instability increases.

Second useful property OOS - decrease nonlinear distortions And interference **.**
Voltage harmonics or interference V amplifier with feedback can be calculated according to the formula

$$Unoc = \frac{Un}{F}, \quad (4)$$

Where ***Up*** - voltage harmonics and interference before the introduction of the OS, ***F*** - depth OS.

When the feedback factor $F > 1$, the harmonic or interference voltage decreases. Physically, this is explained by the fact that the harmonic or interference voltage returns to its point of origin along the feedback loop with the opposite polarity and is subtracted from the original interference voltage .

Third useful property OOS - decrease linear distortions **.** For In amplifiers of harmonic signals, linear distortions should be considered as frequency distortions.

For simple amplifiers from introduction OS border frequencies are changing By formulas

$$f_{нгрос} = \frac{f_{нгр}}{F} \qquad f_{вгрос} = f_{вгр} \cdot F \,, \tag{5}$$

Where $f_{нгр}$ And $f_{вгр}$- lower And top border frequencies to introduction OOS

At OOS $F > 1$ ***fнгрос*** - decreases, A ***fvgros*** - increases, those. at OOS the length of the frequency range is greater, where the frequency response is uniform (and therefore there is no linear distortion).

The physical explanation of this phenomenon coincides with the explanation of the stabilization of the coefficient gain. Chain OOS reacts on change input signal equally, regardless of physical reasons, provocative This change. At POS gain is increasing, But the length of the frequency range with a uniform frequency response is reduced.

The introduction of feedback will change the input impedance of the amplifier . This change does not depend on from method receipt signal OS on exit amplifier, A is determined way introduction signal OS in entrance chain amplifier. Influence OS on input resistance is described by the Blackman formula:

$$R_{вхос} = R_{вх} \cdot \frac{F_{ос}}{F_{\infty ос}} \,, \tag{6}$$

where ***Rinput*** is the input resistance taking into account the feedback; ***Rinput*** *is* the input resistance before introducing the feedback; ***Fog*** *is* the feedback depth at zero internal resistance of the signal source;$F_{\infty ос}$ - the depth of the feedback loop with an infinitely large internal resistance of the signal source.

Size *Fog* is determined component consistent OS; at parallel OS $F_{ос} = 1$.

At consistent OOS

$$R_{вхос} = R_{вх} \bullet F_{ос} \,. \tag{7}$$

If the feedback is negative, ***then the input resistance increases*** , since $F_{ос} > 1$. Physically This is explained those, What at OOS voltage connections subtracted from signal from To restore the same voltage at the amplifier input as before the introduction of feedback, it is necessary to increase the voltage taken from the signal source. With positive feedback, on the contrary, the input impedance decreases.

At parallel OOS

$$R_{вхос} = \frac{R_{вх}}{F_{\infty ос}} \,. \tag{8}$$

If OS negative, That $\boldsymbol{F \infty g} > 1$ And input resistance decreases. Physically, this is explained by the fact that with negative feedback the coupling current is subtracted from the signal from the signal source, and for recovery Togo same current on at the entrance amplifier, which was to introduction OS, necessary increase the current taken from the signal source. With positive feedback, the input resistance increases .

At combined By entrance OS two components signal OS are in effect regardless Friend from friend. IN in accordance With formula Blackman They are changing input resistance V opposite directions. Meaning input resistance after introduction The feedback depends on the ratio of components in the combined feedback signal.

With negative feedback, the input resistance increases if the series feedback prevails. OS And decreases, If prevails parallel OS. For practical For purposes of this study, the case where the serial OS and parallel OS balance each other is useful.

At this from the introduction of the OS And changes its depths R_{in} not changes.

Such property healthy, When source signal is long line, V To eliminate reflected waves, it is necessary to maintain matching mode. This is achieved by maintaining a constant input impedance of the amplifier.

The introduction of feedback also changes the amplifier's output impedance . The output impedance of an amplifier is understood to be the internal resistance of the equivalent generator , which, relative to the load, can replace the amplifier's output circuit.

Change weekend resistance from introduction OS Not depends from method input signal OS on entrance amplifier, A is determined only way receipt signal OS on amplifier output. The effect of feedback on output impedance is determined by the Blackman formula

$$Rвыхос = Rвых \cdot \frac{Fон}{F\infty н} \quad (9)$$

where ***Rout is*** the output resistance taking into account feedback; ***Rout*** is the output resistance before introducing feedback; ***Fon*** is the feedback depth at zero load resistance; ***Fн*** ∞ is the feedback depth at infinite load resistance.

The value of ***F*** is determined component OS by current, at OS voltage ***Background*** = 1. Size *Fн* ∞ is determined component OS By tension, at OS By current ***Fн***∞ = 1.

At OS By current , Thus

$$Rвыхос = Rвых \cdot Fон \quad (10)$$

If OS negative, That *Background* >1, And ***weekend resistance increases*** . Physically , this is explained by the fact that the current feedback stabilizes the output current. The property of constancy weekend current possesses source given current With endlessly big Internal resistance. Current feedback brings the amplifier's output circuit closer to a source of a given current in its properties. With positive feedback, the output resistance, on the contrary, decreases.

At OS by voltage

$$Rвыхос = \frac{Rвых}{F\infty н} \quad (11)$$

If the feedback is negative, ***the output resistance decreases*** . Physically, this is explained by the fact that the voltage feedback stabilizes the output voltage. A source of emf with zero internal resistance has the property of maintaining a constant output voltage . OOS By voltage brings closer day off chain By your own properties To source of emf. With positive feedback, the output resistance, on the contrary, increases.

With a combined output feedback, the two components of the feedback signal act independently of each other. According to Blackman's formula, they change the output impedance. V different directions. Meaning weekend resistance after introduction The combined output feedback depends on the ratio of the current and voltage feedback components in the overall feedback signal. With negative feedback, the output impedance will increase if the current feedback predominates, and decrease if the voltage feedback predominates. For practical purposes, it is useful happening, When OS By current And By voltage balance Friend friend. At this from the introduction of the OS and the change in its depth R_{out} does not change. This property is useful when the amplifier's load is a long line, in which the matching mode must be maintained to eliminate reflected waves. This is achieved by maintaining the amplifier's output impedance constant.

IN amplifiers systems multichannel connections wide application finds OOS With great - depth. An amplifier with deep negative feedback has a fundamentally important property: the coefficient gains amplifier With deep OOS Not depends from coefficient gains amplifying parts schemes, A depends only from coefficient transmissions chains OS. This property you follow from the equation

$$Keoc = \frac{Ke}{F} = \frac{Ke}{1 + \beta \cdot Ke} \approx \frac{1}{\beta} \quad (12)$$

An important rule of thumb follows from this property: if you need to change the coefficient gains amplifier With deep OOS, That regulating element must be included in the feedback circuit and regulate the value of β. The property of an amplifier with deep feedback is the dependence of the coefficient gains from coefficient transmissions chains OOS - practically applies V

amplifiers multichannel connections And For corrections amplitude-frequency distortions signal in communication lines. The signal is distorted when propagating along the communication line, since the attenuation of the line connections is growing With increase frequencies signal. For achievements such properties V The amplifiers use frequency-dependent feedback.

Contents of the practical work performed students V in the course classes

Description laboratory equipment:

– PC for each student;

– program editor schematic modeling Electronics Workbench" (EWB) version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher.

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) At occurrence emergency situations necessary immediately turn off equipment from feeding networks, report about this to the teacher And act according to him instructions.

6) At fire equipment his necessary immediately de-energize, report about this to the teacher, accept measures By elimination fires And act By instructions pre teacher.

7) Upon completion of work with laboratory equipment (computers) it must be turned off in the established order.

Initial data for modeling and research

Options for tasks for individual modeling and research by students are presented in Table A.

Table A - Options tasks for modeling And research.

Option number	Rb1, kOhm	Rb2, kOhm	Option number	Rb1, kOhm	Rb2, kOhm
1.	101	33	2.	101	27
3.	101	24	4.	101	22
5.	101	18	6.	101	15
7.	91	15	8.	91	18
9.	91	22	10.	91	24
11.	91	27	12.	91	33
13.	82	15	14.	82	18
15.	82	22	16.	82	24
17.	82	27	18.	82	33
19.	75	33	20.	75	24

Tasks to be completed during practical work

Tasks basic level:

1) Assemble a basic electrical circuit diagram of a common emitter amplifier with various types of negative feedback using a computer simulation software package.

2) Conduct study useful properties negative reverse connections.

3) Conduct study influences OOS on amplifying properties And frequency amplifier characteristics .

Tasks increased level:

4) Conduct study influences OOS on input And weekend resistance amplification calf.

Order execution work

<u>Exercise 1.</u> Collect V software package computer modeling The basic electrical circuit diagram of an amplifier with a common emitter and with different types of negative feedback.

statement :

Simulate an electrical circuit in the EWB computer simulation software package principled amplifying devices With common emitter without feedback and with the ability to connect various types of negative feedback, namely:

- parallel OOS by voltage;
- consistent frequency-independent OOS by current;
- consistent frequency-dependent OOS By current;
- combined By entrance And exit OOS.

Use a function generator with internal resistance as the signal source. Use a connected active resistor as the load.

For conducting research scheme should have measuring instruments :

– ammeters for measurements input And weekend currents V amplifier;

– voltmeters For measurements input And weekend stresses in the amplifier;

– oscilloscope For analysis forms input And weekend signals And measurements their a couple - of meters;

– frequency response plotter (Bode plotter) for plotting amplitude-frequency and phase-frequency characteristics (AFC and PFC).

Example principled schemes amplifier given on rice. 2.

Order execution tasks

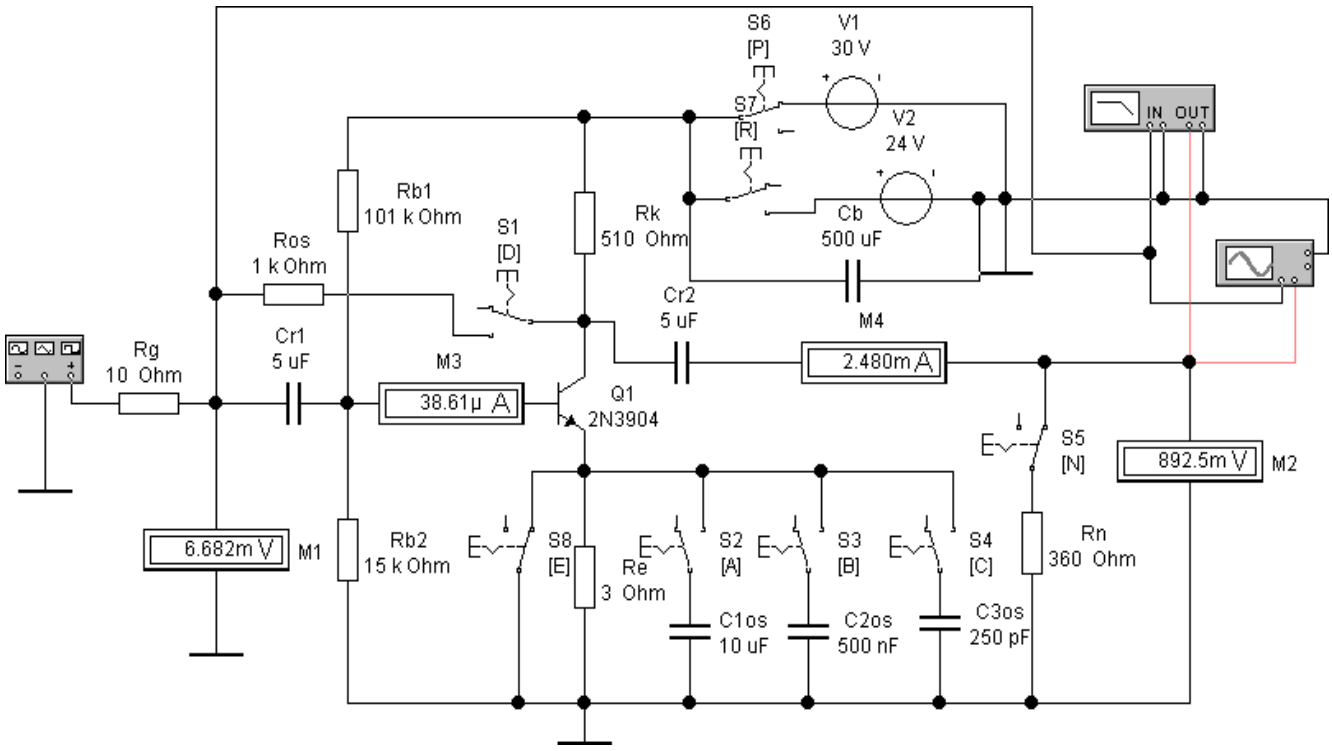
1) Assemble the basic electrical circuit of the amplifier with the given types of feedback in the EWB program and connect the required measuring instruments.

2) Install V collected scheme quantities parameters elements, How shown on Fig. 2, with the exception of the voltage divider resistances ***Rb1*** and ***Rb2*** , the values of which are set according to given option. IN functional generator install the frequency of the input harmonic signal equal to 3 kHz, and the amplitude initially – ***Eg*** = 10 mV.

3) Disable All types OOS, For this install switching keys as follows :

– open keys ***S1*** (button D), ***S2*** (button A), ***S3*** (button B), ***S4*** (button C), disconnecting the resistance and all capacitances in the feedback circuits;

– close key ***S8*** (button E), short-circuiting (disconnecting) the emitter resistance, which also acts as a resistance in the feedback circuit.



Rice. 2 - Fundamental scheme amplifying devices By scheme With common emitter with various types of negative feedback

4) Connect the load by closing the key ***S5*** (button N), apply the supply voltage from 30 volt source, For this close key ***S6*** (button P), A open key ***S7*** (R button).

5) Check right assemblies schemes. For this, before in total, check correctness connections elements schemes Friend To to a friend, A Also connection measuring devices and switching keys, paying particular attention to connecting the power source and grounding.

6) Check the circuit's functionality. To do this, activate the EWB program using the switch located in the upper right corner of the program's working window. If it is correct, work schemes variables voltmeters And ammeters they will show respectively values of input and output currents and voltages that are not equal to 0, while the output values will be significantly greater than the input ones.

7) Tune means measurements:

– ammeters And voltmeters must measure variables ;

– set the horizontal and vertical sweeps on the oscilloscope so that 3–4 oscillation periods are displayed on its screen, and the amplitudes of the input and output signals are approximately the same. Enter the obtained oscillograms into the PZ report ;

– set the graph plotter (Bode plotter) to the frequency response meter mode, to do this, turn - on Magnitude button, in select Vertical frame linear scale along the amplitude axis, and set the upper and lower threshold values F=100 or 500, I=0, in the Horizontal frame select the logarithmic scale along the frequency axis, and set the upper and lower threshold values F=10 GHz, I=1 Hz.

8) Check right settings schemes. For this With help oscilloscope Analyze the input and output signal shapes. In a common-emitter amplifier, they should be out of phase. If the output signal is subject to nonlinear distortion, in which case its shape will differ from the harmonic signal. Eliminate the distortion by reducing the amplitude of the ***Eg generator*** to 1–5 mV.

9) If the oscilloscope or ammeter and voltmeter do not show the presence of an output signal, then find errors in the circuit assembly or in the switching of measuring instruments, then eliminate them, achieving correct operation of the circuit.

10) Include a screenshot of the assembled and working amplifier circuit in your lab report. Draw conclusions based on the work completed in the assignment.

Exercise 2. Conduct study useful properties negative reverse connections.

statement :

IN This task requires confirm expediency introduction OOS V amplifier-devices. To do this, it is necessary to qualitatively evaluate how negative feedback improves the amplifier's key performance indicators or imparts new specific properties to them.

WITH this purpose V task is being carried out study following useful properties OOS: a) reduction of nonlinear distortions;

b) decrease linear (otherwise - frequency And transitional) distortions;

V) increase stability parameters at impact on amplifier destabilizing factor in the form of a change in supply voltage.

Use the amplifier assembled in the previous task as a model for the study. By scheme With common emitter, having opportunity connect various types of environmental protection.

Order execution tasks

1) ***Conduct a study of the beneficial property of feedback—reducing nonlinear distortions*** . To do this, perform the following procedures:

1.1) Install amplifier V original state With open chain OOS:

– close key ***S8*** (button E), short-circuiting (disconnecting) the emitter resistance, which acts as a resistance in the feedback circuit.

– open the switches ***S1*** (button D), ***S2*** (button A), ***S3*** (button B), ***S4*** (button C), - disconnecting the resistance and all capacitors in the feedback circuits.

1.2) Set the harmonic signal voltage in the function generator to 5–10 times greater than the original voltage, equal to 10 mV.

1.3) Launched EWB, With help oscilloscope analyze form weekend signal , making sure that nonlinear distortions occur. Add the resulting oscillogram to the PZ report.

1.4) To determine the harmonic distortion coefficient, perform the following operations:

– install V scheme amplifier informational nodes, For this in tab Select "Circuit" Schematic options», V opened dialogic window install option "Show nodes»;

– Using the Analysis menu, launch the Fourier analyzer, in which you set the following options: output node – the node number corresponding to the amplifier output, fundamental - frequency – 3 kHz, number of harmonics – 10. The Fourier analyzer will launch a window in which the spectrum of the output signal will be displayed;

– With help cursors Fourier analyzer produce measurement amplitudes first 5 harmonics of the output signal, enter the results into table 2;

– calculate And bring in V table 2 coefficient harmonic distortions ($K_Г$), determined by the formula

$$K_{\Gamma} = \frac{\sqrt{U_2^2 + U_3^2 + U_4^2 + \ldots + U_n^2 + \ldots}}{U_1} \quad . \qquad (13)$$

Table 2 – Calculation results And measurements.

View OOS in the amplifier	***Amplitude harmonics***				
	U_{g1} =	U_{g2} =	U_{g3} =	U_{g4} =	U_{g5} =
Open OOS chain					
	K_G =				
Parallel OOS By voltage					
	To_G =				
Consistent frequency-independent current feedback					
	To_G =				

1.5) Connect V amplifier parallel OOS By tension, having closed key ***S1*** (button D).

1.6) Launched EWB, With help oscilloscope analyze form weekend signal , ensuring that nonlinear distortions are reduced. Add the resulting oscillogram to the PZ report.

1.7) Determine the harmonic distortion coefficient in the presence of parallel feedback by voltage. To do this, launch the Fourier analyzer, use its cursors to measure the amplitudes of the first 5 harmonics of the output signal, results enter into table 2, calculate and enter into table 2 the coefficient of harmonic distortion (K_G), determined by formula (13).

1.8) Connect the serial frequency-independent current feedback to the amplifier by opening switches ***S1*** (button D) and ***S8*** (button E).

1.9) Launched EWB, With help oscilloscope analyze form weekend signal , ensuring that nonlinear distortions are reduced. Add the resulting oscillogram to the PZ report.

1.10) Define coefficient harmonic distortions at availability sequential current feedback. To do this, launch the Fourier analyzer (Fourier), use its cursors to perform measurement amplitudes first 5th harmonics weekend signal, results enter into table 2, calculate and enter into table 2 the coefficient of harmonic distortion (K_G), determined by formula (13).

1.11) Draw conclusions based on the results of the conducted research on how negative feedback affects nonlinear distortion in an amplifier.

2) ***Conduct a study of the beneficial property of negative feedback – reduction of linear (- frequency and transient) distortion*** . To do this, perform the following procedures:

2.1) Install amplifier V original state with weak frequency-dependent OOS:

– open key ***S8*** (button E), having connected resistance emitter, acting as a resistance in the feedback circuit.

– open keys ***S1*** (button D), ***S3*** (button B), ***S4*** (button C), having closed key ***S2*** (button A), having connected capacity 10 μF V chain reverse connections.

2.2) Set up a pulse signal in the function generator with a voltage amplitude of 10 mV and a duty cycle of 50%.

2.3) Launched EWB, With help oscilloscope analyze form weekend pulse signal, making sure that linear (transient) distortions occur. Add the resulting oscillogram to the PZ report.

2.4) Determine the frequency distortion coefficients of the first 5 odd harmonics of a pulse signal using a graph plotter. To do this, perform the following operations :

– Run the EWB simulator, open the Bode plotter by moving the cursor on required frequencies, produce measurements coefficients gains on these often takh and enter them into table 3;

Table 3 – Calculation results And measurements.

View OOS	Frequency harmonics, kHz	f_{g1} =3	f_{g3} =9	f_{g5} =15	f_{g7} = 21	f_{g9} =27
weak frequency-dependent feedback (at *With* os = 10 (μF)	Coefficient amplification , K_{Gi} , dB					
	Coefficient distortions of M_{Gi} , dB					
strong consistent - frequency-dependent OOS by current (at *With* os = 250 pF)	Coefficient strengthened nia, To_{Gi} , dB					
	Coefficient distortions of M_{Gi} , dB					
parallel OOS by voltage	Coefficient amplification , K_{Gi} , dB					
	Coefficient search-zheniya M_{Gi} , dB					
combined at the entrance and exit OOS	Coefficient amplification , K_{Gi} , dB					
	Coefficient distortions of M_{Gi} , dB					

– using a graph plotter (Bode plotter) determine the maximum coefficient gains To_{max} at availability weak consistent frequency-dependent OOS By current;

– calculate And bring in V table 3 coefficients frequency (transitional) distortion in decibels for these harmonics according to the formula

$$M_{\text{Gi}} = K_{\text{Gi}} - K_{\max}; \quad (14)$$

– qualitatively evaluate existing distortions, do conclusions.

2.5) Connect V amplifier strong consistent frequency-dependent OOS by current, by opening switch ***S2*** (button A), closing button ***S4*** (button C), connecting a 250 pF capacitor to the feedback circuit.

2.6) Launched EWB, With help oscilloscope analyze form weekend signal , making sure that the linear (transient) distortions change. Add the resulting oscillogram to the PZ report.

2.7) Determine the frequency distortion coefficients of the first 5 odd harmonics of a pulse signal using a graph plotter. To do this, perform the following operations :

– Run the EWB simulator, open the Bode plotter by moving the cursor on required frequencies, produce measurements coefficients gains on these often takh and enter them into table 4;

– using a graph plotter (Bode plotter) determine the maximum gain coefficient K_{max} in the presence of strong consistent frequency-dependent negative feedback on current;

– calculate And bring in V table 3 coefficients frequency (transitional) distortion in decibels for these harmonics according to formula (14);

– qualitatively evaluate existing distortions, do conclusions.

2.8) Connect a frequency-independent parallel voltage feedback in the amplifier by closing - switches ***S1*** (button D) and ***S2*** (button A), opening button ***S4*** (button C), and connecting a 1 kOhm resistance to the feedback circuit.

2.9) Launched EWB, With help oscilloscope analyze form weekend signal , making sure that the linear (transient) distortions change. Add the resulting oscillogram to the PZ report.

2.10) Define coefficients frequency distortions first 5th odd harmonics of a pulse signal using a graph plotter. To do this, perform the following operations :

– Run the EWB simulator, open the Bode plotter by moving the cursor on required frequencies, produce measurements coefficients gains on these often takh and enter them into table 4;

– using a graph plotter (Bode plotter) determine the maximum gain coefficient K_{max} in the presence of parallel voltage feedback;

– calculate And bring in V table 3 coefficients frequency (transitional) distortion in decibels for these harmonics according to formula (14);

– qualitatively evaluate existing distortions, do conclusions.

2.11) Connect the combined input and output feedback to the amplifier by closing the switches ***S1*** (button D) and ***S4*** (button C), and opening the button ***S2*** (button A).

2.12) After running EWB, use an oscilloscope to analyze the shape of the output signal, having made sure V change linear (transitional) distortions. Received Enter the oscillogram into the PZ report.

2.13) Define coefficients frequency distortions first 5th odd harmonics of a pulse signal using a graph plotter. To do this, perform the following operations :

– Run the EWB simulator, open the Bode plotter by moving the cursor on required frequencies, produce measurements coefficients gains on these often takh and enter them into table 3;

– using a graph plotter (Bode plotter) determine the maximum gain coefficient K_{max} in the presence of a combined environmental protection system;

– calculate And bring in V table 3 coefficients frequency (transitional) distortion in decibels for these harmonics according to formula (14);

– qualitatively evaluate existing distortions, do conclusions.

2.14) Draw conclusions based on the results of the conducted research on how negative feedback affects linear (frequency and transient) distortion in an amplifier.

3) ***Conduct study useful properties OOS - decrease instability of the gain parameters (pass-through gain)*** . To do this, perform the following procedures:

3.1) Install amplifier V original state With open chain OOS:

– close key ***S8*** (button E), short-circuiting (disconnecting) the emitter resistance, which acts as a resistance in the feedback circuit.

– open the switches ***S1*** (button D), ***S2*** (button A), ***S3*** (button B), ***S4*** (button C), - disconnecting the resistance and all capacitances in the feedback circuits;

– install with the ***S6*** key (P button) supply voltage +30 V.

3.2) Apply a harmonic signal from the function generator to the amplifier input current voltage E_g = 10 mV With taking into account Togo, What V generator is being installed signal amplitude .

3.3) Define relative instability through coefficient gains without OOS. To do this, follow these steps:

– measure With help voltmeter voltage weekend signal amplifier $U1_{output}$ and enter the result in table 4;

– calculate the throughput gain at the initial supply voltage and enter the result into Table 4 using the formula

$$K1_E = U1_{out} / E_G ; \quad (15)$$

– install key ***S7*** (button R) voltage nutrition +24 IN, unlocked key ***S6*** (P button);

– measure With help voltmeter voltage weekend signal amplifier $U2_{out}$ at changed nutrition And bring in result V table 4;

– calculate the throughput gain for a changed supply voltage and enter the result into table 4 using the formula

$$K2_E = U2_{exit} / E_G; \quad (16)$$

– calculate And bring in V table 4 relative instability through coefficient gains without OOS By received values at different voltage nutrition By formula mule

$$q_o = \frac{K1_E - K2_E}{K1_E}. \quad (17)$$

Table 4 – Calculation results and measurements.

View OOS		Parameters		
Without OOS	U_{pit} = 30 IN	$U1_{out}$ =	$K1_E$ =	q_o =
	U_{pit} = 24 IN	$U2_{out}$ =	$K2_E$ =	F =
Consistent OOS by current	U_{pit} = 30 IN	$U1_{out}$ =	$K1_E$ =	q_{OS} =
	U_{pit} = 24 IN	$U2_{out}$ =	$K2_E$ =	F =
Parallel voltage feedback	U_{pit} = 30 IN	$U1_{out}$ =	$K1_E$ =	q_{os} =
	U_{pit} = 24 IN	$U2_{out}$ =	$K2_E$ =	F =
Combined environmental protection	U_{pit} = 30 IN	$U1_{out}$ =	$K1_E$ =	q_{OS} =
	U_{pit} = 24 IN	$U2_{out}$ =	$K2_E$ =	F =

3.4) Connect V amplifier consistent frequency-independent OOS By current:

– open key ***S8*** (button E), having connected resistance emitter, acting as a resistance in the feedback circuit;

– rest keys ***S1*** (button D), ***S2*** (button A), ***S3*** (button B), ***S4*** (button C) leave in the open state;

– install key ***S6*** (button R) voltage nutrition +30 IN, unlocked key ***S7*** (R button).

3.5) Define relative instability through coefficient gains in the presence of a serial current feedback. To do this, perform the following operations:

– measure With help voltmeter voltage weekend signal amplifier $U1_{output}$ and enter the result in table 4;

– calculate through coefficient gains at original voltage nutrition and enter the result into table 4 using formula (15);

– install key ***S7*** (button R) voltage nutrition +24 IN, unlocked key ***S6*** (P button);

– measure With help voltmeter voltage weekend signal amplifier $U2_{out}$ at changed nutrition And bring in result V table 4;

– calculate the end-to-end gain factor for a changed supply voltage and enter the result in Table 4 using formula (16);

– calculate And bring in V table 4 relative instability through coefficient gains at availability consistent OOS By current With taking into account received values at different supply voltages according to formula (17);

– calculate And bring in V table 4 depth reverse connections according to the formula

$$F = \frac{q_o}{q_{OS}}, \quad (18)$$

Where q_o - relative instability through coefficient gains without OOS.

3.6) Connect V amplifier parallel OOS by voltage:

– close the key ***S8*** (button E), turning off resistance emitter, acting as a resistance in the feedback circuit;

– close key ***S1*** (button D), having connected resistance reverse connections R_{os}, leave the remaining keys ***S2*** (button A), ***S3*** (button B), ***S4 (button C) in the open state;***

– install key ***S6*** (button R) voltage nutrition +30 IN, unlocked key ***S7*** (R button).

3.7) Define relative instability through coefficient gains in the presence of parallel voltage feedback. To do this, perform the following steps:

– measure With help voltmeter voltage weekend signal amplifier $U1_{output}$ and enter the result in table 4;

– calculate the through gain at the initial supply voltage and enter the result into Table 4 using formula (15);

– install key ***S7*** (button R) voltage nutrition +24 IN, unlocked key ***S6*** (P button);

– measure With help voltmeter voltage weekend signal amplifier $U2_{out}$ at changed nutrition And bring in result V table 4;

– calculate the end-to-end gain factor for a changed supply voltage and enter the result in Table 4 using formula (16);

– calculate And bring in V table 4 relative instability through gain coefficient in the presence of parallel voltage feedback, taking into account the values obtained at different supply voltages according to formula (17);

– calculate And bring in V table 4 depth of reverse connections By formula (18).

3.8) Connect V amplifier combined environmental protection:

– open key ***S8*** (button E), having connected resistance emitter, acting as a resistance in the feedback circuit, close the switch ***S1*** (button D), connecting the feedback resistance R_{os};

– leave the remaining keys ***S2*** (button A), ***S3*** (button B), ***S4 (button C) in the open*** state;

– install key ***S6*** (button R) voltage nutrition +30 IN, unlocked key ***S7*** (R button).

3.9) Define relative instability through coefficient gains If there is a combined OOS, perform the following steps:

– measure With help voltmeter voltage weekend signal amplifier $U1_{output}$ and enter the result in table 4;

– calculate the through gain at the initial supply voltage and enter the result into Table 4 using formula (15);

– install key ***S7*** (button R) voltage nutrition +24 IN, unlocked key ***S6*** (P button);

– measure With help voltmeter voltage weekend signal amplifier $U2_{out}$ at changed nutrition And bring in result V table 4;

– calculate the end-to-end gain factor for a changed supply voltage and enter the result in Table 4 using formula (16);

– calculate And bring in V table 4 relative instability through gain coefficient in the presence of combined feedback based on the values obtained at different supply voltages according to formula (17);

– calculate And bring in V table 4 depth of reverse connections By formula (18).

3.10) Draw conclusions based on the results of the conducted research on how the negative feedback affects the instability of the gain parameters.

Task 3. Conduct a study of the influence of negative feedback on the amplification properties and frequency characteristics of the amplifier.

statement :

In this task, it is necessary to establish how different types of feedback affect the voltage gain, the clamping gain, the current gain, and the power factor in an amplifier built using a common emitter circuit, as well as its frequency characteristics using the frequency response as an example.

IN quality models For research use assembled V first task an amplifier with a common emitter circuit, which has the ability to connect various types of feedback and means for measuring primary parameters: input and output currents and voltages.

Order execution tasks

1) ***Conduct a study of the effect of negative feedback on the gain properties of the simulated amplifier*** . To do this, perform the following procedures:

1.1) Install amplifier V original state With open chain OOS:

– close key ***S8*** (button E), short-circuiting (disconnecting) the emitter resistance, which acts as a resistance in the feedback circuit.

– open the switches ***S1*** (button D), ***S2*** (button A), ***S3*** (button B), ***S4*** (button C), - disconnecting the resistance and all capacitors in the feedback circuits.

1.2) Set the amplitude of the harmonic signal in the function generator so that its effective voltage is equal to 10 mV.

1.3) Launched EWB, With help oscilloscope analyze form weekend signal , making sure that there are no nonlinear distortions.

1.4) Determine the amplifier's gain in non-feedback mode. To do this, perform the following steps:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and U_{out} , and with the help of ammeters the currents I_{in} and I_{exit} , enter the results in table 5;

– calculate the through gain K_E , voltage gain K , current gain K_I and power gain K_P If there is no OOS, enter the results in Table 5.

Table 5 - Calculation results And measurements.

Parameters	View OOS			
	Without OOS	**Sequential OOS By current**	**Parallel OOS for voltage**	**Combined - environment al protection**
E_G , mV				
U_{in} , mV				
I_{in} , μA				
U_{out} , mV				
$I'_{m\ out}$, mA				
K_E				
K				
K_I				
K_P				
F	1			

1.5) Switch the amplifier to the operating mode with the series current feedback connected:

– open key ***S8*** (button E), having connected resistance emitter, acting as a resistance in the feedback circuit, close the switch ***S4*** (button C), connecting the optimal capacitance to the feedback circuit;

– keys ***S1*** (button D), ***S2*** (button A), ***S3*** (button B) leave open.

1.6) Define coefficients enhancements amplifier V mode work at connected serial current feedback. To do this, perform the following operations:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and U_{out} , and with the help of ammeters the currents I_{in} and I_{exit} , enter the results in table 5;

– calculate the end-to-end gain K_{EOC} , voltage gain K_{OS} , coefficient gains By current K_{IOS} And coefficient gains By capacity of K_{POS} with the series current feedback connected, enter the results into table 5;

– calculate And bring in V Table 5 depth value reverse connections, using the formula

$$F = \frac{K_{E}}{K_{EOC}}. \quad (19)$$

1.7) Switch the amplifier to the operating mode with parallel voltage feedback connected :

– close switch ***S8*** (button E) and open switch ***S4*** (button C), respectively disconnecting the resistance and capacitance in the series feedback circuit;

– close switch ***S1*** (button D), connecting the resistance in the parallel feedback circuit ;

– keys ***S2*** (button A), ***S3*** (button B) leave open.

1.8) Define coefficients enhancements amplifier V mode work at connected parallel voltage feedback. To do this, perform the following operations:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and U_{out} , and with the help of ammeters the currents I_{in} and I_{exit} , enter the results in table 5;

– calculate the through gain K_{E} , voltage gain K , current gain K_{I} and power gain K_{P} with the parallel voltage feedback connected, enter the results into table 5;

– calculate And bring in V Table 5 depth value reverse connections, using formula (19).

1.9) Translate amplifier V mode work at combined OOS:

– open key ***S8*** (button E) And close key ***S4*** (button C), respectively by connecting resistance and capacitance in the series feedback circuit;

– close switch ***S1*** (button D), connecting the resistance in the parallel feedback circuit ;

– keys ***S2*** (button A), ***S3*** (button B) leave open.

1.10) Define coefficients enhancements amplifier V mode work at connected combined OOS. To do this, perform the following operations:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and U_{out} , and with the help of ammeters the currents I_{in} and I_{exit} , enter the results in table 5;

– calculate the through gain K_{E} , voltage gain K , current gain K_{I} and power gain K_{P} when the combined OOS is connected, enter the results into table 5;

– calculate And bring in V Table 5 depth value reverse connections, using formula (19).

1.11) Analyze received coefficients gains And do conclusions, O how negative feedback affects the amplification properties of an amplifier with a common emitter circuit.

2) ***Conduct study useful influences OOS on frequency characteristics of the modeled amplifier*** . To do this, perform the following procedures:

2.1) Install amplifier V original state With open chain OOS:

– close key ***S8*** (button E), short-circuiting (disconnecting) the emitter resistance, which acts as a resistance in the feedback circuit.

– open the switches ***S1*** (button D), ***S2*** (button A), ***S3*** (button B), ***S4*** (button C), - disconnecting the resistance and all capacitors in the feedback circuits.

2.2) Determine the amplifier's amplified frequency range using a graph plotter. To do this, perform the following steps:

– set up the graph plotter (Bode plotter) in the frequency response meter mode, to do this, turn on Magnitude button, in select Vertical frame linear scale along the amplitude axis, and set the upper and lower threshold values F=100 or 500, I=0, in the Horizontal frame select the logarithmic scale along the frequency axis, and set the upper and lower threshold values F=10 GHz, I=1 Hz;

– launch simulator EWB, get With help graph plotter (Bode plotter) frequency response amplifier without OOS, measure on frequency response coefficient gains By voltage V region of mid frequencies K_{sr} , by moving the frequency response meter cursor to the flat section of the frequency response in the region of f_{sr} = 3 kHz. The obtained frequency response with the result of the gain measurement should be entered into the PZ report ;

– define With help frequency response meter border frequencies gains, For this moving guy cursor on level gains, equal 0.707 from K_{sr} , With start to the left, A then to the right from average frequency, measure the values of the lower $f_{gr.n}$ **accordingly and the upper** gain limit frequency f . The obtained results are entered into Table 6;

Table 6 - Calculation results And measurements.

View OS	Parameter	Frequency		
		$f_{gr.n}$, Hz	f_{cf} , kHz	$f_{gr.v}$, MHz
without OOS	Coefficient gains *TO* , dB			
	frequency			
	Phase shift φ , hail.			
	frequency			
Sequential OOS By current	Coefficient gains *TO* , dB			
	frequency			
	Phase shift φ , hail.			
	frequency			
Parallel OOS By tension	Coefficient gains *TO* , dB			
	frequency			
	Phase shift φ , hail.			
	frequency			
Combined - environmental protection	Coefficient gains *TO* , dB			
	frequency			
	Phase shift φ , hail.			
	frequency			

– rebuild plotter (Bode plotter) V mode frequency response meter, For this turn on button Phase, V frame Vertical choose linear scale By axes amplitudes, And set the upper and lower threshold values F=0 ° , I= -360 ° , in the Horizontal frame leave the previous upper and lower threshold values F=10 GHz, I=1 Hz;

– launch simulator EWB, get With help graph plotter (Bode plotter) phase response of the amplifier without negative feedback, measure the phase shift in the mid-frequency region φ_{cp} **on the phase response** by moving cursor phase response meter on flat plot phase response V area f_{cf} = 3 kHz. Received The phase response with the result of the gain measurement shall be entered into the PZ report;

– define With help phase response meter border frequencies gains, For this moving the cursor to the left to the phase shift level φ_{cp} +45 ° , and then to the right to the phase shift level φ_{cf} - 45 ° , measure accordingly, the value of the lower $f_{gr.n}$ **and the** upper gain limit frequency f . The obtained results are entered into Table 6.

2.3) Switch the amplifier to the operating mode with the series current feedback connected:

– open key ***S8*** (button E), having connected resistance emitter, acting as a resistance in the feedback circuit, close the switch ***S4*** (button C), connecting the optimal capacitance to the feedback circuit;

– keys ***S1*** (button D), ***S2*** (button A), ***S3*** (button B) leave open.

2.4) of the amplifier using a graph plotter at availability consistent OOS By current. For this take advantage of methodology, given in paragraph 2.2). The obtained frequency response and phase response, as well as the results of measurements and calculations, are entered into Table 6.

2.5) Switch the amplifier to the operating mode with parallel voltage feedback connected :

– close switch ***S8*** (button E) and open switch ***S4*** (button C), respectively disconnecting the resistance and capacitance in the series feedback circuit;

– close switch ***S1*** (button D), connecting the resistance in the parallel feedback circuit ;

– keys ***S2*** (button A), ***S3*** (button B) leave open.

2.6) Using a graph plotter, determine the amplifier's amplified frequency range in the presence of parallel voltage feedback. To do this, use the method described in section 2.2. Enter the resulting frequency response and phase response, as well as the measurement and calculation results, into Table 6.

2.7) Translate amplifier V mode work at combined OOS:

– open key ***S8*** (button E) And close key ***S4*** (button C), respectively by connecting resistance and capacitance in the series feedback circuit;

– close switch ***S1*** (button D), connecting the resistance in the parallel feedback circuit ;

– keys ***S2*** (button A), ***S3*** (button B) leave open.

2.8) of the amplifier using a graph plotter at availability combined OOS. For this take advantage of methodology, given in paragraph 2.2). The obtained frequency response and phase response, as well as the results of measurements and calculations, are entered into Table 6.

2.9) Analyze the obtained frequency response, phase response, and gain range cutoff - frequencies And do conclusions, O volume, How influences OOS on frequency characteristics amplifier By common emitter circuit.

<u>Task 4.</u> Conduct a study of the influence of negative feedback on the input and output resistance of an amplifier (high level).

statement :

This task requires analyzing the capabilities of negative feedback to change the amplifier's input or output impedance in the desired direction to improve its matching with the signal source and load. To do this, research should determine how different types of negative feedback affect the amplifier's input or output impedance.

IN quality models For research use assembled V first task an amplifier with a common emitter circuit, which has the ability to connect various types of feedback and means for measuring primary parameters: input and output currents and voltages.

Order execution tasks:

1.1) Set the amplifier to its initial state with the feedback circuit open and the load connected.

1.2) Install V functional generator such amplitude, equal 10 mV.

1.3) After running EWB, determine the input and output impedance of the amplifier in non-feedback mode. To do this, perform the following steps:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and $U_{out\ (R_H=360)}$, and with the help of ammeters the currents I_{in} and I_{exit}, enter the results in table 7;

Table 7– Calculation results And measurements.

Parameters	View OOS			
	Without OOS	Sequential OOS By current	Parallel OOS for voltage	Combined - environmental protection
U_{in}, mV				
I_{in}, μA				
$U_{out\ (R_H=360)}$, IN				
$I_{'m\ out}$, mA				
$U_{out\ (R_H=\infty)}$, IN				
R_{in}, Ohm				
R_{out}, Ohm				

– open ***S5*** key (button N), turning off load and having translated exit amplifier in mode single move, measure With help voltmeter voltage weekend signals amplifier $U_{out(R_H=\infty)}$, enter the result into table 7;

– calculate and enter into table 7 the values of the input and output impedance of the amplifier using the formulas

$$R_{in} = \frac{U_{in}}{I_{in}}, \quad R_{out}\,\text{Ohm} = R_{n=360}\left(\frac{U_{out\ R_H=\infty}}{U_{out\ R_H=360}} - 1\right). \qquad (20)$$

1.4) Switch the amplifier to the operating mode with the series feedback connected for current and load.

1.5) After running EWB, determine the input and output impedance of the amplifier in the - mode work at connected consistent OOS By current. For this execute the following operations:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and $U_{out\ (R_H=360)}$, and with the help of ammeters the currents I_{in} and I_{exit}, enter the results in table 7;

– open ***S5*** key (button N), turning off load and having translated exit amplifier in mode single move, measure With help voltmeter voltage weekend signals amplifier $U_{out(R_H=\infty)}$, enter the result into table 7;

– calculate and enter into table 7 the values of the input and output impedance of the amplifier using formulas (20).

1.6) Switch the amplifier to the operating mode with parallel feedback connected for voltage and load.

1.7) After running EWB, determine the input and output impedance of the amplifier in - operating mode with parallel voltage feedback connected. To do this, perform the following steps:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and $U_{out\ (R_H=360)}$, and with the help of ammeters the currents I_{in} and I_{exit}, enter the results in table 7;

– open ***S5*** key (button N), turning off load and having translated exit amplifier in mode single move, measure With help voltmeter voltage weekend signals amplifier $U_{out(R_H=\infty)}$, enter the result into table 7;

– calculate and enter into table 7 the values of the input and output impedance of the amplifier using formulas (20).

1.8) Switch the amplifier to the operating mode with the combined feedback and load connected.

1.9) After running EWB, determine the input and output impedance of the amplifier in - operating mode with the combined feedback connected. To do this, perform the following steps:

– measure With help voltmeters voltage input And weekend signals amplifier U_{in} and $U_{out\ (R_H=360)}$, and with the help of ammeters the currents I_{in} and I_{exit}, enter the results in table 7;

– open ***S5*** key (button N), turning off load and having translated exit amplifier in mode single move, measure With help voltmeter voltage weekend signals amplifier $U_{out(R_H=\infty)}$, enter the result into table 7;

– calculate and enter into table 7 the values of the input and output impedance of the amplifier using formulas (20).

1.10) Analyze received values resistances And do conclusions, O how the environmental protection system influences changes in the approval properties amplifier with a common emitter circuit.

<u>Task 5. (for independent work)</u> Present the research results in the form of a laboratory report and defend it.

1) IN report according to PZ display:

– topic and target work, tasks For research And brief order their execution;

– simulated V editor schematic modeling a basic electrical circuit diagram of an amplifier using a common emitter and various types of negative feedback;

– oscillograms input and weekend signals;

– graphs frequency response And phase response With results measurements border frequencies stripes gains;

– research results in the form of tables with measurements and calculations of the specified primary and secondary parameters of the amplifiers;

– conclusions By results execution tasks And V in general By work done .

2) Protect report By done laboratory work, having completed individual for the assignment specified by the teacher, within the framework of the research conducted.

Control questions For preparation To protection:

1. For what V amplifying devices applies OOS?
2. Provide a definition of the terms "feedback", "loop gain", "return ratio", "feedback depth".
3. Classification OS By sign And frequency dependencies parameter OS.
4. Classification OS by method of obtaining OS signal at the amplifier output.
5. Classification OS by route of administration OS signal to the amplifier input
6. Influence OS on coefficients gains at consistent OS.
7. Influence OS on coefficients gains at combined by the OS input **.**
8. Influence OS on coefficients gains at parallel OS.
9. Influence OS for stability gain factors .
10. OS influence for nonlinear distortions and interference.
11. OS influence for linear distortions.
12. Influence on input resistance consistent OS.
13. Influence on input resistance parallel OS.
14. Influence on input resistance combined By entrance to the OOS.
15. Influence on the output resistance of the current feedback.
16. Influence on the output resistance of the feedback voltage.
17. Influence on weekend resistance combined By exit OOS.
18. Properties amplifier With deep OOS.
19. Principle And target corrections frequency response With help frequency-dependent OOS.

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 4

Subject: **STUDY APERIODIC REINFORCEMENT CASCADES**

Time – 4 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– realize circuit design (computer) modeling various typical amplifiers cascades With using universal packages applied computer programs;

– conduct a study of the design principles and main characteristics and parameters of typical amplifier stages;

– collection and analysis of information to generate initial data for the design of electronic amplifying devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Calculation and modeling of aperiodic amplification stage.	25 min
2. Study aperiodic amplifying cascade.	50 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	90 min
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**65 min**
3. Calculation and emitter follower modeling.	20 min
4. Research of emitter follower.	45 min
The final part	**15 min**
Defense of practical work reports	10 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

The calculation of an aperiodic amplifier on transistors includes the following main - stages:

1) Choice transistor And elemental bases.

2) Calculation static regime (i.e. calculation transistor By direct current).

3) Calculation dynamic regime (those. calculation transistor By variable current).

As a rule, in practice, when designing an amplifier, the engineer is given ***the initial data*** :

– input (U_{in}) and output (U_{out}) voltage of the amplifier (or the gain factors of the current amplifier K_I and by voltage K_U);

– input resistance amplifier (R_{in});

– resistance loads (R_n);

– amplifier bandwidth $\Delta f = f_{in} - f_h$, where f_{in} , f_{in} – lower and upper limit frequencies of gain;

– range workers temperatures $T_0 \pm \Delta T$;

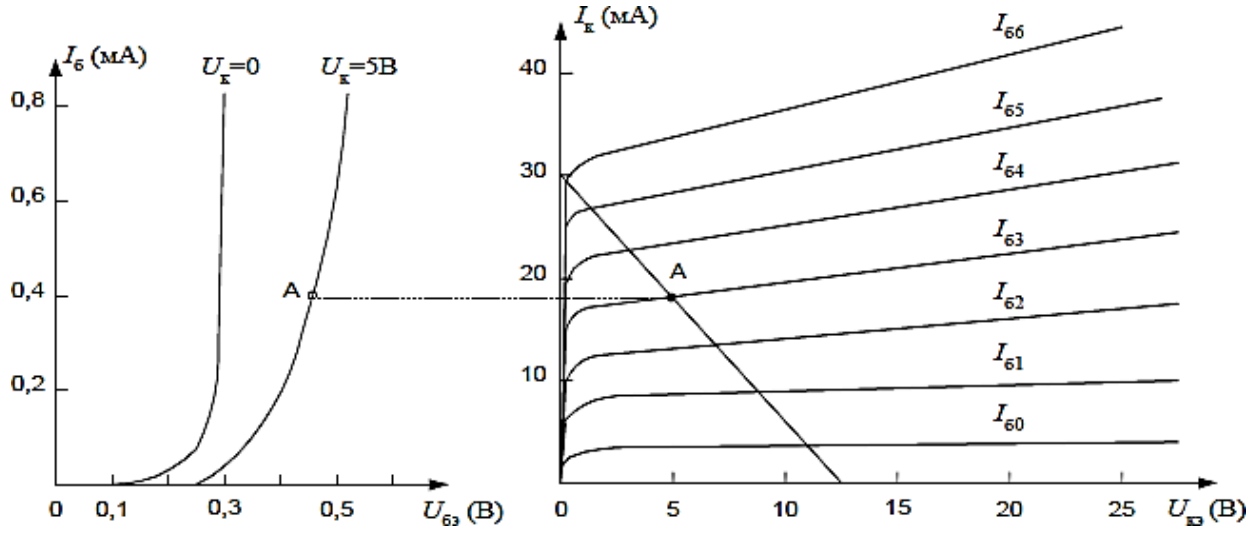
– power supply voltage E_{to} .

The number of initial parameters generated by the consumer may be greater or less than those given.

Calculation static regime work bipolar transistor at a constant rate current

Calculation static regime consists of V definition permanent currents And stresses on conclusions transistors, A Also consumed power. Calculation it begins With tasks working points on input And day off volt-ampere characteristics (VAH) transistor. After this, the resistor resistances for the selected cascade circuit are calculated using Ohm's law . The calculation is completed by determining the temperature instability coefficient *S* and the collector current increment with temperature change *T*.

Setting the operating point means setting its position on the input and output characteristics (Fig. 1). From Fig. 1 it is clear that setting the collector load resistance R_{to} fixes position working points V within loading direct. Exercise current bases (in this case I_{b3}) fixes position working points already on one point loading straight (point "A" in Fig. 1).



Rice. 1 - Position working points "A" on input And day off characteristics of the transzistor

The base current can be set using a current (voltage) source included in the base circuit. However inclusion V diagram additional source voltage irrational, That 's why other methods are used.

Most effective is combination ways fixed base voltage and setting the operating point using negative current feedback.

Task calculation transistor By direct current consists of V definition nominal values resistors V scheme, which ask working point of the transistor. Let's consider diagram on rice. 2. IN this case We should find quantities resistances R to, R 1, R 2, R e, A also the temperature instability coefficient S .

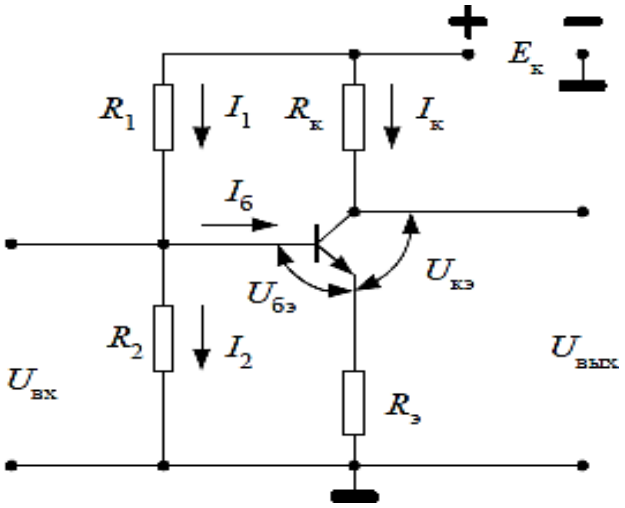
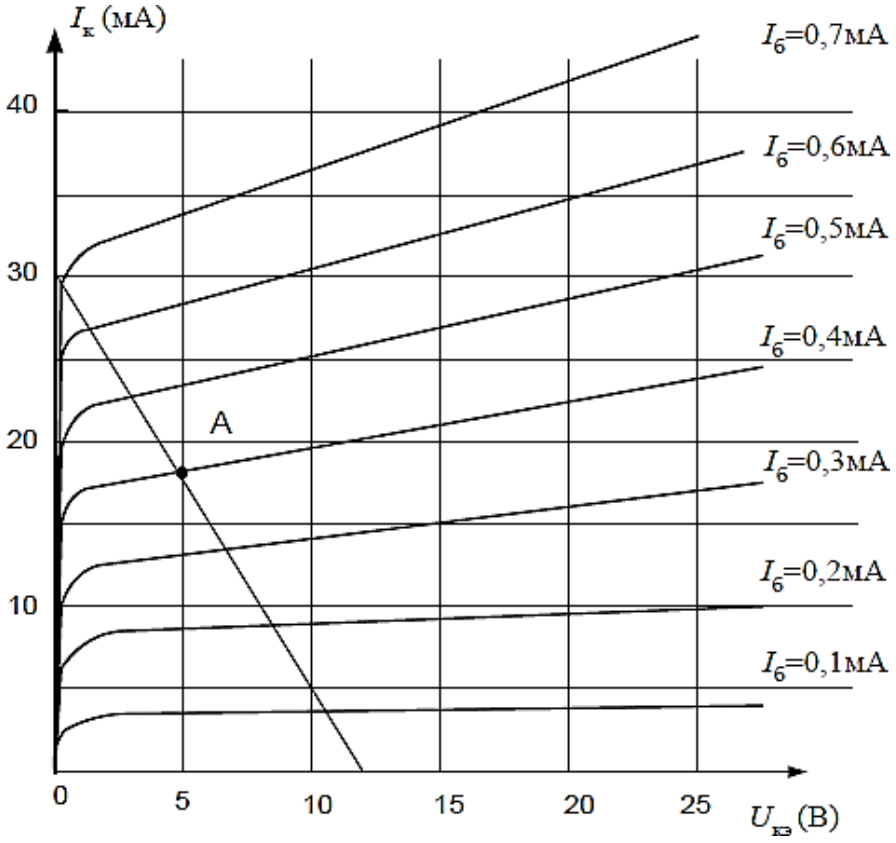
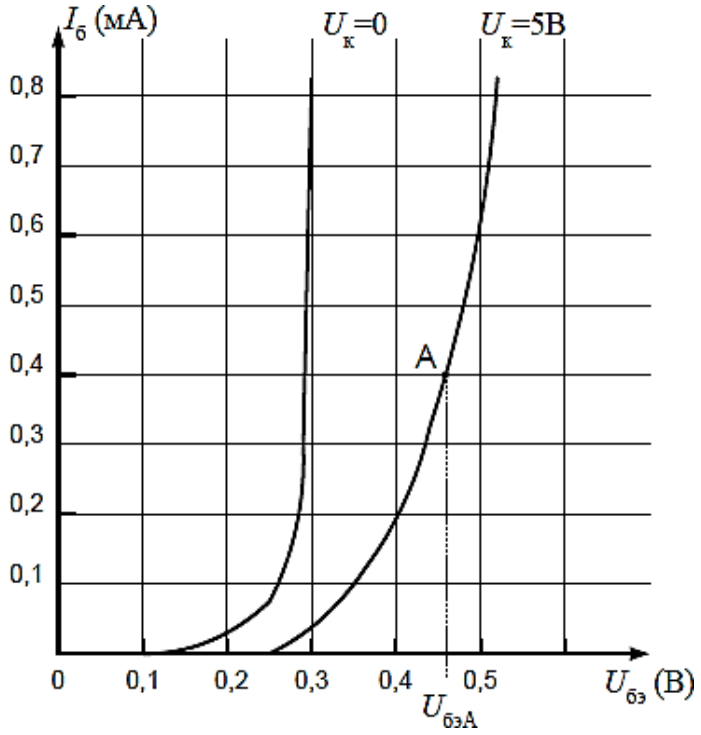


Fig. 2 – Schematic diagram of an aperiodic (resistive) amplifier with negative feedback on current Let us consider solution this tasks on specific example. Let we have standard

source nutrition $E_к$ = 12 IN, low-power transistor KT-312B, For whom we choose operating mode class A. For this transistor V reference book given All necessary characteristics (Fig. 3 – 4).



Rice. 3 - Weekend characteristics transistor KT312B



Rice. 4 - Entrance characteristics transistor KT312B

Let's select the operating point "A" of the transistor with parameters U_{keA} = 5 V, I_{keA} = 18 mA. We draw a load line through point "A" and through the point with coordinates $U_{ke} = E_k$ = 12 V, I_{ke} = 0 to intersections With axis current. By loading characteristics we find maximum The transistor's saturation current value. For the case under consideration, it is equal to I_{kN} = 30 mA. Knowing the transistor's saturation current, we can now find the value of the resistor in the collector circuit, R_k

$$I_{кн} = \frac{E_к}{R_к} \quad \rightarrow \quad R_к = \frac{E_к}{I_{кн}} = \frac{12\ В}{30 \cdot 10^{-3}\ А} = 400\ Ом \quad . \qquad (1)$$

From the standard series of resistances we select the closest value R_k = 430 Ohm or 390 Ohm, V dependencies from requirements To coefficient gains *KU* or strip transmission. If we need to obtain the maximum gain K_U, then we need to choose the value collector resistance, equal R_k = 430 Ohm, If same us required maximum bandwidth, then you need to take R_k =390 Ohm.

Next, using the output characteristic of the transistor, we determine the base current at point "A" $I_{бA}$ (Fig. 3). In this case, it is equal to: I_{bA} = 0.4 mA. Then, using the input characteristic, we find the value voltage on base V point "A" $U_{бэA}$. IN ours example fall voltage on the base will be equal to: $U_{bэA}$ = 0.46 V.

Current emitter is sum currents collector And bases, i.e.

$$I_{эА} = I_{кА} + I_{бА} = 18\ мА + 0{,}4\ мА = 18{,}4\ мА \quad .$$

We are composing equation equilibrium stresses By to the second rule Kirchhoff For emitter-collector circuits

$$E_k = I_{kA} \cdot R_k + U_{ke} + I_{eA} R_e \quad . \qquad (2)$$

For input chains By to the second rule Kirchhoff Can make up two equations equal-equilibrium :

$$E_{to} = I1 \cdot R1 + I2 \cdot R2 \; ; \qquad (3)$$

$$E_k = I1 \cdot R1 + U_{beA} + U_{Re} = I1 \cdot R1 + U_{beA} + I_{eA} \cdot R_e \quad . \qquad (4)$$

From equations (3) And (4) follows, What

$$U_{R2} = I2 \cdot R2 = U_{Re} + U_{beA} = I_{eA} \cdot R_e + U_{beA} \quad .$$

Resistance R e carries out negative reverse connection By current (OOS). Fall voltage on him should be small, That's why usually from practical considerations choose $U_{Re} \approx (0.1 \div 0.3) E_к$. Let's take in in our case $U_{Re} = 0.1 E_к$, Then from this conditions you can find the resistance value in the emitter circuit:

$$R_э = \frac{U_{Rэ}}{I_{эА}} = \frac{0.1 \cdot E_к}{I_{эА}} = \frac{0{,}1 \cdot 12\,В}{18{,}4 \cdot 10^{-3}\,А} \approx 66\,Ом.$$

We choose denomination resistor By standard row resistances type MLT, equal to 100 ohms. Then the voltage drop across the emitter resistance will be:

$$U_{Rэ} = I_{эА} \cdot R_э = 18{,}4 \cdot 10^{-3}\,А \cdot 100\,Ом = 1{,}84\,В.$$

For tasks fixed voltage on base transistor necessary, to $U_{R2} = U_{Rэ} + U_{bэ}$ =1.84 + 0.46 = 2.3 IN.

For calculation resistance R 2 necessary know size current I 2. How And V In the previous case, for practical reasons, we choose the values of currents I 1 and I 2 to be equal to:

$$I_1 = 5 \cdot I_{bA} = 5 \cdot 0.4\,мА = 2\,мА,\ I_2 = I_1 - I_{bA} = 2 - 0.4 = 1.6\,мА.$$

Now Can calculate size resistor R 2:

$$R_2 = \frac{U_{R2}}{I_2} = \frac{2{,}3\,В}{1{,}6\,мА} = 1438\,Ом.$$

We select the closest value from the standard series of MLT type resistances, equal to R 2 = 1.5 kOhm. Next By equation (1) For input chains we are counting on size resistor R 1:

$$R_1 = \frac{E_к - U_{R2}}{I_1} = \frac{(12 - 2{,}3)\,В}{2 \cdot 10^{-3}\,А} = 4850\,Ом.$$

We choose denomination from standard rows, equal R 1=5.1 kOhm. Let's calculate Now power - dissipation on the resistances we have chosen:

$$P_1 = I_1^2 \cdot R_1 = \left(2 \cdot 10^{-3}\right)^2 \cdot 5{,}1 \cdot 10^3 = 20{,}4 \cdot 10^{-3}\,Вт;$$

$$P_1 = I_1^2 \cdot R_1 = \left(1{,}6 \cdot 10^{-3}\right)^2 \cdot 1{,}5 \cdot 10^3 = 3{,}84 \cdot 10^{-3}\,Вт;$$

$$P_к = I_к^2 \cdot R_к = \left(18 \cdot 10^{-3}\right)^2 \cdot 430 = 139{,}32 \cdot 10^{-3}\,Вт;$$

$$P_э = I_э^2 \cdot R_э = \left(18{,}4 \cdot 10^{-3}\right)^2 \cdot 100 = 33{,}856 \cdot 10^{-3}\,Вт.$$

Thus, in our circuit, to set the operating point, it is necessary to put resistors of the following values:

R 1 – MLT – 0.125 Tue – 5.1 kOhm; R 2 – MLT – 0.125 W – 1.5 kOhm;

R k – MLT – 0.250 Wt. – 430 Ohm; R e – MLT – 0.125 W – 100 Ohms.

Next let's calculate coefficient temperature instability. For this at first Let's calculate the parameters D and α:

$$D = \frac{R_э}{R_1} + \frac{R_э}{R_2} + \frac{R_э \cdot R_к}{R_1 \cdot R_2} = \frac{100}{5100} + \frac{100}{1500} + \frac{100 \cdot 430}{5100 \cdot 1500} =$$

$$= 0{,}020 + 0{,}067 + 0{,}006 = 0{,}093;$$

$$\alpha = \frac{h_{21э}}{h_{21э} + 1} = \frac{50}{50 + 1} = 0{,}9804.$$

Now we can determine the temperature instability coefficient for a circuit with negative current feedback:

$$S = \frac{1 + D}{1 - \alpha + D} = \frac{1 + 0{,}093}{1 - 0{,}98 + 0{,}093} = \frac{1{,}093}{0{,}113} = 9{,}67.$$

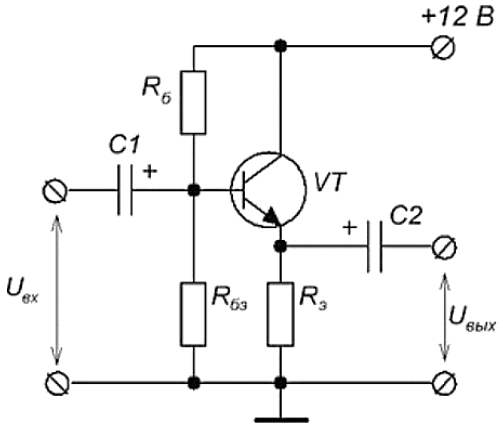
Knowing coefficient temperature instability, Can find size increment of collector current ΔI_{to} when the temperature changes within a given range ΔT .

Calculation emitter follower

Emitter repeater V electronics performs role cascade, providing matching between a signal source with a high output impedance and a low-impedance load. In even simpler terms, ***an emitter follower lowers the output impedance of the signal source*** .

In this case, you should remember a simple rule: ***an emitter follower provides amplification By current, A Not By voltage*** . Because is increasing strength current, hence, increases And power, given away V load, So How $P=IU$, Where P - This power, I -power current, U – voltage.

Let's calculate diagram emitter repeater For sound signal (rice. 5) at $U_{pit} = 12$ Volt.



Rice. 5 – Emitter follower circuit

To ensure the signal has the highest possible amplitude, the operating point (quiescent) must be in the middle of the transistor's active mode (the linear portion of the output characteristic). For this, the emitter voltage must be equal to half the supply voltage :

$$U_E = U_{pit} / 2 = 12/2 = 6 \text{ IN} .$$

To avoid wasting heat on the transistor, the optimal quiescent current is usually taken V 1 mA. This Means, What By chains *+12V —> collector —-> emitter —>*R_e*—>earth* must flow current With by force V 1 mA. Here We Not we take into account tiny current bases. How How can this be achieved? Let's recall Ohm's law for a section of a circuit and calculate the resistor value:

$$I_e = U_e / R_e , R_e = U_e / I_e , R_e = 6 \text{ В} / 0.001 \text{ А} = 6\,000 \text{ Ohm} = 6 \text{ kOhm} .$$

Let's take it nearest from rows on 6.2 kOhm.

What current must flow through the base-emitter to provide a quiescent current of 1 mA? So How V ours example current emitter I_e almost equal collector current I_{to} (If, of course not consider tiny base current) That we remember formula dependencies current bases from collector current :

$$\beta = \frac{I_{\text{коллектора}}}{I_{\text{базы}}}.$$

Let's take a powerful transistor KT81 7B, which has β equal to about 300, and the voltage drop at the base-emitter junction is 0.55 volts.

Hence, $I_b = I_{to} / \beta = 1/300 = 3.3 \text{ μA}$.

We calculate the current of the voltage divider, which is formed by two resistors: R_b and $R_э$. It is usually taken 10 times greater than the base current:

$$I'm_{\text{in business}} = 10 \cdot I_b = 10 \cdot 3.3 = 33 \text{ μA}.$$

Let's count voltage at the base. It is equal to:

$$U_B = U_E + U_{BE} = 6 + 0.55 = 6.55 \text{ IN.}$$

From Ohm's law we obtain the following calculations:

$R_{BE} = 6.55 \text{ IN} / 33 \mu A = 200 \text{ kOhm}$.

We take the closest one from the 200 kilo-ohm series. Since the sum of the voltage drops across the resistors is equal to U_{supply} , therefore, across R_b the voltage will be 12 - 6.55 = 5.45 Volts.

$R_b = 5.45 \text{ V} / 33 \mu A = 165 \text{ kOhm}$. We take the closest one from the 150 kilo-Ohm series.

Capacitors V scheme they serve us For in order to put away constant component, That There is constant current, which present on base And emitter. For choice capacitors exist simple rule: *constant time RC chains* $t=R_{in} C1$ *should be more the period of the transmitted signal of the lowest frequency is approximately 100 times.*

Input resistance emitter repeater is calculated By formula:

$R_{in} = R_e \beta = 6000 \cdot 300 = 1.8 \text{ Mohm.}$

For sound signal the most low frequency - This 20 Hertz (limit hearing (person), from this we find a period of 0.05 sec and a capacitor value *of* $2.7 \mu F$. That is, we take a capacitor larger than 2.7 μF, for example, 10 μF.

Table 1 – Rows of radio component ratings

E12	E24		E96						
1,0	1,0	4,3	100	143	210	301	432	619	887
1,2	1,1	4,7	102	147	215	309	442	634	909
1,5	1,2	5,1	105	150	221	316	453	649	931
1,8	1,3	5,6	107	154	226	324	464	665	953
2,2	1,5	6,2	110	158	232	332	475	681	976
2,7	1,6	6,8	113	162	237	340	487	698	
3,3	1,8	7,5	115	165	243	348	499	715	
3,9	2,0	8,2	118	174	249	357	511	732	
4,7	2,2	9,1	121	178	255	365	523	750	
5,6	2,4		124	182	261	374	536	768	
6,8	2,7		127	187	267	383	549	787	
8,2	3,0		130	191	274	392	562	806	
	3,3		133	196	280	402	576	825	
	3,6		137	200	287	412	590	845	
	3,9		140	205	294	422	604	866	

Contents of the practical work performed students V in the course classes

Description laboratory equipment:

– PC for each student;

– program editor schematic modeling Electronics Workbench" (EWB) version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher.

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) At occurrence emergency situations necessary immediately turn off equipment from the power supply networks, report about this to the teacher And act according to him instructions.

6) At fire equipment his necessary immediately de-energize, report about this to the teacher, accept measures By elimination fires And act By instructions pre teacher.

7) Upon completion of work with laboratory equipment (computers) it must be turned off in the established order.

Initial data for modeling and research

Options for tasks for individual modeling and research by students are presented in Table 2.

Table 2 - Options tasks For calculation and modeling.

No. vari anta	Transistor	Source power supply ($E_к$), V	No. vari anta	Transistor	Source power supply ($E_к$), V
1.	2N 2218	9	2.	2N 2218	20
3.	2N 2222	12	4.	2N 2222	18
5.	2N 2369	15	6.	2N 2369	9
7.	2N 4124	18	8.	2N 4124	12
9.	2N 3391	20	10.	2N 3391	15
11.	2N 3707	9	12.	2N 3707	20
13.	2N 3903	12	14.	2N 3903	18
15.	2N 3904	15	16.	2N 3904	9
17.	2N 3947	18	18.	2N 3947	12
19.	2N 4014	20	20.	2N 4014	15

Tasks to be completed during practical work

Tasks basic level:

1) Conduct calculation And modeling aperiodic amplifying cascade.

2) Conduct study aperiodic amplification stage.

Tasks increased level:

3) Conduct calculation And modeling emitter repeater.

4) Conduct study emitter repeater.

Order execution work

Exercise 1. Conduct calculation And modeling aperiodic amplifying cas-Kada

. statement :

Calculate For given By option original data And simulate V programs-nom package computer modeling EWB diagram electrical principled aperiodic amplifying stage with a common emitter circuit.

Initial data are given type transistor And voltage source nutrition (cm. table 2). Tasks is being carried out at condition absence reference (passport) data about the transistor.

The task must be performed under the following constraints: since the specified transistors are low-power, That collector current peace Not must exceed 10 mA for 2N 2xxx transistors, 15 mA for 2N 3xxx transistors and 20 mA for 2N 4xxx transistors, and the emitter-base voltage is about 800 mV plus or minus 50 mV.

IN quality source signal from frequency f = 1 kHz use measuring functional generator With internal resistance R_G, equal 50 Ohm. IN quality loads use active resistance R_N = 10 kOhm.

For conducting research scheme should have measuring instruments :

- ammeters For measurements currents V amplifier circuits ;
- voltmeters For measurements stresses on amplifier elements ;

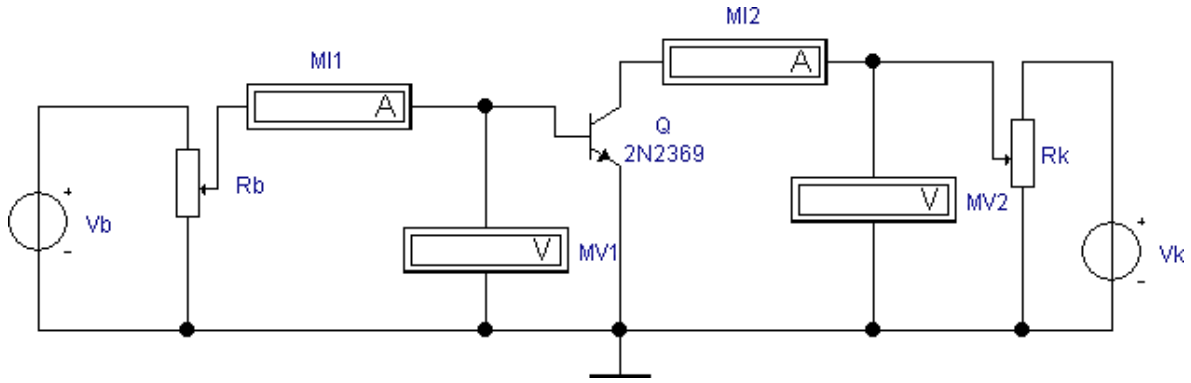
– oscilloscope for analyzing the shape of input and output signals and measuring their - parameters;

– plotter frequency response (Bode plotter) For constructions amplitude-frequency And phase-frequency characteristics (AFC and PFC).

Order execution tasks 1

1.1) ***Modeling schemes measurements statistical VAH given bipolar transistor using a common emitter circuit and determining the transistor's quiescent parameters*** **.** To do this, perform the following procedures:

1.1.1) Build a circuit diagram using the EWB program to measure the statistical current-voltage characteristic (CVC) of a given transistor using a common emitter circuit. An example of the circuit is shown in Fig. 7.



Rice. 7 - Fundamental electric scheme measurements statistical VAH common-emitter bipolar transistor

1.1.2) Install V collected scheme, using For this windows properties elements, their required parameters:

– type transistor **Q** And voltage source nutrition collector **VK** according to vari-antu;

– variables resistance **Rb** and **Rk** respectively - 1 kOhm And 2 kOhm With step by step re-construction sites (increment) 1%;

– For changes quantities variables resistances **Rb** And **Rk** enter keys ***B*** And ***K*** respectively on English layout;

1.1.3) Translate ammeters And voltmeters V mode measurements permanent quantities.

1.1.4) Define voltage And currents peace (working dots) transistor. For this you perform the following actions:

– smoothly changing size resistance **Rk** , pressing simultaneously keys ***Shift*** and ***K*** For increases or key ***K*** For decrease, install voltage collector-emitter of the transistor, equal to half the voltage of the collector power source;

– smoothly changing size resistance **Rb ,** pressing simultaneously keys ***Shift*** and ***B*** to increase or ***B key*** to decrease, set the base-emitter voltage of the transistor, approximately equal 800 mV plus or minus 50 mV, like this in this way, to collector quiescent current $\mathbf{I}_{\mathbf{K0}}$ did not exceed the specified value - 10 or 15 or 20 mA;

– If voltage collector-emitter transistor changed, That smoothly changing the value of resistance **Rk** , restore the collector-emitter voltage of the transistor, equal to half the voltage of the collector power source;

– having achieved required values stresses, produce measurement current bases And collector current in idle mode;

– bring in V report By laboratory work V table 3 results measurements voltages and currents in the idle mode (no input signal).

Table 3 - Voltage And currents rest (working) points) of the transistor

Parameters			
U_{BE0}, mV	**I_{B0}, μA**	**$U_{KЭ0}$, IN**	**I_{K0}, mA**

1.1.5) Do conclusions By results done V task 1.1 work.

1.2) ***Calculation of an aperiodic amplifier cascade*** . To do this, perform the following - procedures:

1.2.1) Launch the Mathcad Professional application for mathematical and engineering calculations, in the window that opens, enter the initial data: the specified voltage of the power source **E_K** and the constant voltages and quiescent currents obtained during the measurement process, which set the operating point of the transistor, are listed in Table 3.

1.2.2) Enter formulas For calculation following amplifier parameters :

– resistance chains emitter- collector

$$R_{ke} := \frac{E_k - U_{ke0}}{I_{k0}};$$

– constant collector current saturation transistor

$$I_{kн} := \frac{E_k}{R_{ke}};$$

– constant emitter current V mode transistor quiescent state

$$I_{e0} := I_{k0} + I_{b0};$$

– fall voltage on resistance emitter

$$U_{Re} := 0.01 \cdot E_k;$$

– resistance V chains emitter, providing negative reverse connection By curre nt

$$R_e := \frac{U_{Re}}{I_{e0}};$$

– resistance V collector chains

$$R_k := R_{ke} - R_e;$$

– fixed fall voltage on base transistor

$$U_{R2} := U_{be0} + U_{Re};$$

– current V branches divider stresses, leaking through resistance **R_1**

$$I_1 := 10 \cdot I_{b0};$$

– current V branches divider stresses, leaking through resistance **R_2**

$$I_2 := I_1 - I_{b0};$$

– resistance resistor **R_2** voltage divider

$$R_2 := \frac{U_{R2}}{I_2};$$

– resistance resistor **R_1** voltage divider

$$R_1 := \frac{E_k - U_{R2}}{I_1} ;$$

– own input resistance transistor By direct current

$$h_{11} := \frac{U_{be0}}{I_{b0}} ;$$

– own weekend transistor resistance By permanent current

$$h_{22} := \frac{U_{ke0}}{I_{k0}} .$$

– capacity dividing capacitors And capacitor V chains emitter

$$C_r := \frac{1}{2\pi \cdot f} \quad C_e := \frac{3}{2\pi \cdot f} ,$$ And

Where ***f*** - given signal frequency .

1.2.3) The program listing with calculation results and units of measurement should be included in the laboratory report.

1.2.4) By results calculations choose from rows denominations radio components, given in Table 1, the resistance values of the capacitors closest to the calculated values and enter them into Table 4.

Table 4 - Calculated And selected quantities resistances for the calculated aperiodic amplifying stage.

Calculated parameters					
R 1 , kOhm	**R 2** , kOhm	**R k ,** Ohm	**R e** , Ohm	**C r ,** μF	**C e** , μF
Selected parameters from a series of denominations					
R 1 , kOhm	**R 2** , kOhm	**R k ,** Ohm	**R e** , Ohm	**C r ,** μF	**C e** , μF

1.2.5) Do conclusions By results done V task 1.2 works.

1.3) ***Modeling an aperiodic gain stage*** . To do this, perform the following procedures:

1.3.1) Assemble the electrical circuit diagram of an aperiodic waveform in the EWB - program amplifying cascade By scheme With common emitter. Example schemes given on rice. 8.

1.3.2) Connect measuring instruments to the elements of the amplifying cascade that provide :

– measuring the electric current in the branches of the voltage divider, in the base and collector circuits of the transistor, as well as in the load circuit;

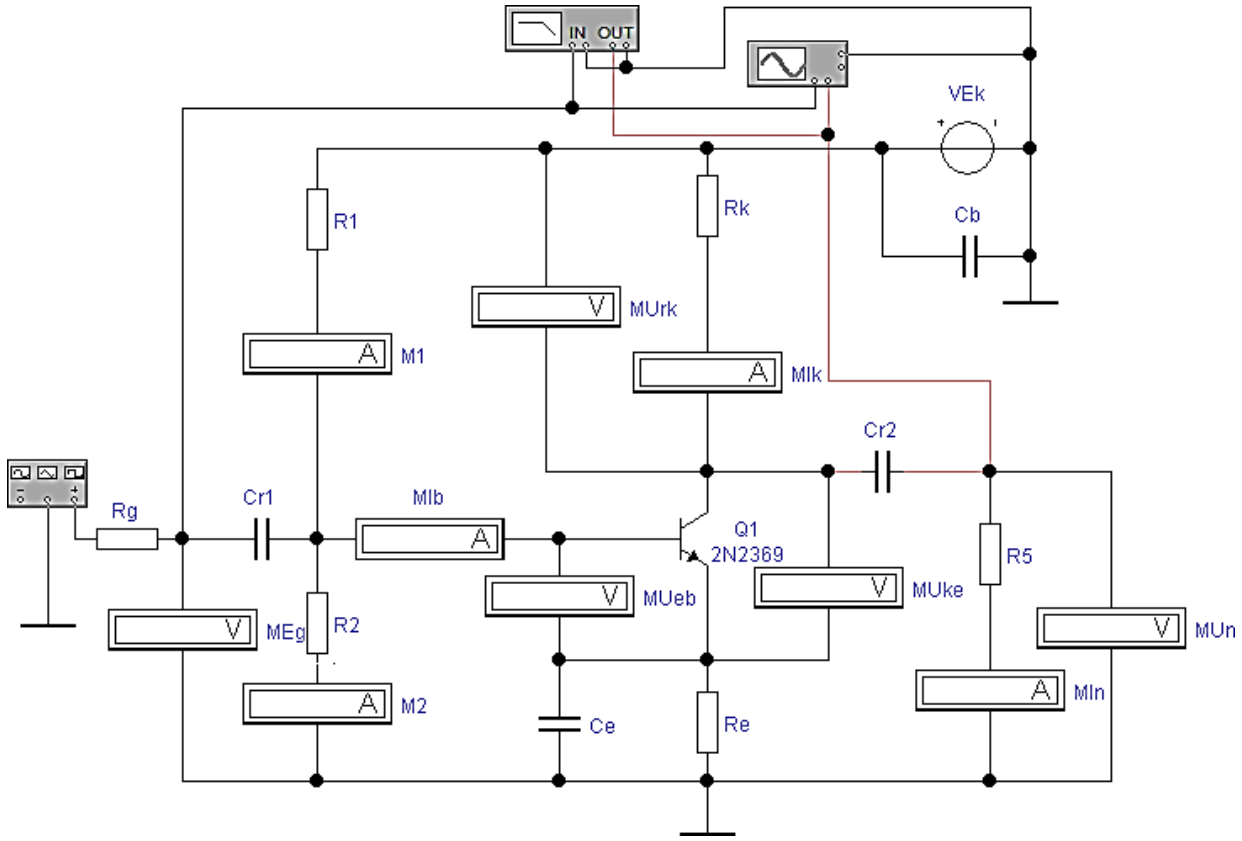
– measuring the voltage drop at the input and output of the amplifier stage, at the emitter-base and collector-emitter electrodes of the transistor, at the resistance in the collector circuit;

– analysis forms input And weekend signals, measurement their parameters;

– receiving amplitude-frequency And phase-frequency characteristics (frequency response And Phase-frequency response). Set the ammeters and voltmeters to the mode of measuring constant values, with the exception of voltmeters And ammeters, measuring values input And weekend signal-hunting.

1.3.3) Install V collected scheme given transistor And voltage source power supply, as well as the selected values of the element parameters (from Table 4). Set the capacity of the blocking capacitor - 100 μF. IN functional generator install frequency

input harmonic signal equal to 1 kHz, and the amplitude is initially ***Eg*** = 10 mV. The generator and load resistances should be 50 Ohms and 10 kOhms respectively.



Rice. 8 - Electric principled scheme aperiodic amplifying cascade according to the common emitter circuit

1.3.4) Check right assemblies schemes. For this, before in total, check the correct connections of the circuit elements to each other, as well as the connection of measuring instruments, paying particular attention to the connection of the power source and grounding.

1.3.5) **Check the circuit's functionality and, if necessary, adjust it for DC** . To do this, activate the EWB program using the switch located in the upper right corner of the program's working window. If it works correctly, schemes variables voltmeters And ammeters they will show respectively values input and weekend currents And stresses, Not equal 0, at this weekend values will be significantly more input. Check are served whether required voltage on electrodes base-emitter U_{BE0} and collector-emitter U_{KE0} . If the collector-emitter voltage is not approximately equal to half voltage nutrition, That changing size resistance collector, like this in such a way that it is included in the given series of denominations, to achieve this.

1.3.6) Set up the oscilloscope by setting the horizontal and vertical sweeps as follows: in this way, to on his screen was located 3 - 4 period fluctuations, A amplitudes the input and output signals were approximately the same. Enter in report on the software received oscillograms.

1.3.7) Verify the correct tuning of the AC amplifier circuit . To do this, use an oscilloscope to analyze the input and output signal shapes. In a common-emitter amplifier, they should be out of phase. If the amplifier is correctly designed and modeled, the output signal should be linear and free of nonlinear distortion. If this is not the case, it is necessary to find the error in the circuit or calculations and correct it, achieving correct operation. Include a screenshot of the assembled and operational amplifier circuit in your lab report.

1.3.8) Launch Fourier analyzer And get spectrum weekend signal. At When setting up the amplifier stage correctly , make sure that it does not distort the output signal, i.e. Not contributes nonlinear distortions. Bring in V report By laboratory work screenshot output signal spectrum .

1.3.9) Do conclusions By results done V task 1.3 works.

1.4) ***Do generalizing conclusions*** By results conducted calculation And modeling of an aperiodic amplifying cascade.

Exercise 2. Conduct study aperiodic amplifying cascade Problem statement:

This assignment requires three specific research objectives to be completed: first, necessary define various coefficients gains aperiodic amplifier stage, secondly, to obtain its amplitude-frequency characteristic (AFC) and evaluate its range properties, and, thirdly, to conduct research on the influence of resistance values on position working points transistor, on parameters And high quality indicators of the amplification cascade.

By the quality of an amplifier's performance, we mean its ability to amplify a signal without changing its shape. This means that an ideal amplifier should precisely repeat all changes in voltage (or current). Deviations in the output signal shape from the input signal shape are called distortion, which reduces the amplifier's performance. Thus, distortion is a qualitative indicator of an amplifier.

When performing this task, use the harmonic distortion coefficient indicator to evaluate the quality of the amplifier.

Order execution tasks

2.1) ***Determine the gain (transfer) coefficients of the aperiodic amplifier stage*** :

- coefficient gains by tension;
- through coefficient gains;
- coefficient gains by current;
- coefficient gains by power.

This part of the assignment is completed by students independently . The methodology for completing it is similar to the methodology used in previous laboratory assignments.

Results research bring in V table 5.

Table 5 – Measured and calculated parameters of the aperiodic amplifier stage.

Measured parameters				
E_G, **mV**	U_{BX}, **mV**	I_{BX}, μA	U_{OUTPUT}, mV	I_{EXIT}, mA
Calculated parameters				
K_E	K	K_I	K_P	

Analyze the obtained gain factors and draw conclusions about the amplifying properties of an aperiodic amplifying cascade using a common emitter circuit.

2.2) ***Construct the amplitude-frequency response (AFR) of an aperiodic amplifier stage and evaluate its range properties*** .

For execution this point tasks on one's own necessary:

2.2.1) Get With help graph plotter (Bode plotter) frequency response amplifying cascade and include it in the laboratory report.

2.2.2) Determine the lower and upper limit gain bands of the aperiodic cascade, and its amplified frequency band.

2.2.3) Estimate, based on the ratio f_{GDV} / f_{GRN}, what class of amplifiers the aperiodic amplifier stage belongs to in terms of the range of amplified frequencies.

Results research bring in V table 6.

Table 6 – Measured and calculated parameters of the aperiodic amplifier stage.

f_{UAH}, [Hz]	f_{UAH}, [MHz]	$\Delta f = f_{GRV} - f_{UAH}$, [MHz]	f_{GRV} / f_{GRN}

2.2.4) Do conclusions O range properties aperiodic amplifying cas-
Kada.

2.3) ***Conduct research influences quantities resistances on provisions work-whose transistor points, on the parameters and quality indicators of the amplification stage*** .

For this execute next procedures:

2.3.1) Conduct measurements quantities permanent stresses And currents, asking And determining the operating point (quiescent point) of the transistor in a tuned aperiodic amplifying - stage. For this purpose, perform the following actions (operations):

– disable the input signal by setting the amplitude in the function generator to 0;

– I_1 using ammeters M1 and M2 and I_2, flowing in the voltage divider circuits formed by resistances R_1 and R_2, enter the obtained results into table 7;

– measure the constant base and collector currents of the transistor using ammeters MIb and MIk, and enter the obtained results into Table 7;

– measure With help voltmeters MUeb, MUke And MUrk respectively constant voltages on transitions base-emitter And collector-emitter transistor And on resistance R_k in the collector circuit, enter the obtained results into table 7;

– Compare the measured values with the calculated values obtained when completing the 1st task, draw conclusions about why these values differ.

Table 7 - Measured And calculated values permanent currents And stresses V aperiodic amplifying stage.

Calculated parameters						
I_1, [mA]	In_2, [mA]	For_{b0}, [μA]	For_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [B]	U_{Rk0}, [B]
Measured parameters						
In_1, [mA]	In_2, [mA]	I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [IN]	U_{Rk0}, [V]

2.3.2) Calculate the following parameters of the tuned aperiodic amplifier stage in the quiescent mode:

– input And weekend resistances active element (transistor) By direct current;

– steepness transistor at a constant rate current according to the formula

$$G_0 = I_{k0} / U_{be0};$$

– coefficient transmissions By current.

Received results bring in V Table 8.

Table 8 – Calculated parameters of the aperiodic amplifier stage in the quiescent mode .

Calculated parameters			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]

2.3.3) Calculate and analyze the operation of a tuned aperiodic amplifier stage. To do this, perform the following steps:

– With functional generator submit on amplifier input signal With amplitude 10 mV;

– translate ammeters MIb, MIk, voltmeters MUeb, MUke, MUrk V mode measured nia variables quantities;

– carry out measurements of the variable components of currents and voltages occurring in the amplifier stage, and enter the results into Table 9;

– calculate input And weekend resistance active element (transistor) for alternating current, enter the obtained results in Table 9;

– calculate And bring in V table 9 meaning steepness transistor By variable current, using the formula

$$G = I_{k} / U_{be};$$

Table 9 - Measured And calculated parameters aperiodic amplifying AC cascade.

Measured parameters				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]
Calculated parameters				
R_{in}, [Ohm]	R_{out}, [Ohm]	G, [A/B]	K_I	K_U	**KGI, %**

– calculate coefficient transmissions transistor By variable current And voltage, the obtained results should be entered into Table 9;

– through the Analysis menu, launch the Fourier analyzer, in which set the following options: output node – the node number corresponding to the amplifier output, fundamental - frequency – 1 kHz, number of harmonics – 10. The Fourier analyzer will launch a window in which the spectrum of the output signal will be displayed;

– With help cursors Fourier analyzer produce measurement amplitudes first 3 harmonics of the output signal, include screenshots of the measurements of the amplitudes of the spectrum harmonics in the laboratory report;

– calculate And bring in V table 9 coefficient harmonic distortions (KGI), determined by the formula

$$K_{\Gamma} = \frac{\sqrt{U_2^2 + U_3^2 + U_4^2 + \ldots + U_n^2 + \ldots}}{U_1};$$

– do conclusion O quality work configured aperiodic amplifying cas- kada;

– conduct comparative analysis received values parameters amplifier By By- standing And variable currents.

2.3.4) Conduct a study of the effect of the ***R1 resistance in the voltage divider circuit on the transistor's quiescent mode, input and output parameters,*** **and** the DC gain of the amplifier stage. To do this, perform the following steps:

– bring in measured previously values parameters (from table 7) configured amplifier stage (with the set resistance value ***R1) in the idle mode in Table*** **10** , and the previously calculated parameters (from Table 8) in Table 11;

Table 10 – Measured direct currents and voltages in the aperiodic amplifier stage in quiescent mode

Measured parameters at meaning resistance R1 - 1 kOhm						
I_1, [mA]	I_2, [mA]	I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [IN]	U_{Rk0}, [V]
Measured parameters at established meaning resistance R1						
I_1, [mA]	I_2, [ma]	I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [IN]	U_{Rk0}, [V]
Measured parameters at meaning resistance R1 + 1 kOhm						
I_1, [mA]	I_2, [mA]	I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [IN]	U_{Rk0}, [V]

– turn off the input signal and switch the ammeters and voltmeters to the constant value measurement mode;

– change size resistance ***R* 1** on 1 kOhm, With beginning reducing his, A then increasing ;

– For both cases produce measurements And calculation given parameters, enter the results in tables 10 and 11;

Table 11 - Calculated parameters aperiodic amplifying cascade V mode for peace.

Calculated parameters at meaning resistance R1 - 1 kOhm			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]
Calculated parameters at established meaning resistance R1			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]
Calculated parameters at meaning resistance R1 + 1 kOhm			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]

– do conclusion O volume, How have changed constant currents And voltage V amplification stage in the idle mode with decreasing and increasing resistance ***R* 1** ;

– analyze and determine how the position of the operating point on the output and input characteristics of the transistor changed with a decrease and increase in resistance R ***1* .** To do this, use the graphs in Fig. 3 and 4 as an example;

– analyze and determine how the input and output parameters have changed , coefficient transmissions By permanent current at decrease And increase resistance ***R* 1** .

2.3.5) Conduct a study of the influence of the resistance value **R1** in the voltage divider circuit on the input and output parameters for alternating current, transmission coefficients And qualitative indicator amplifying cascade. WITH this purpose execute the following actions:

– turn on input signal And translate ammeters And voltmeters V mode measurements of variable quantities;

– enter the previously measured values of the parameters for alternating current (from Table 9) of the configured amplification stage (at the established resistance value ***R* 1**) in Table 12, and the previously calculated parameters (from Table 9) in Table 13;

– change size resistance ***R* 1** on 1 kOhm, With beginning reducing his, A then increasing ;

– For both cases produce measurements And calculation given parameters, enter the results in tables 12 and 13;

Table 12 – Measured parameters for alternating current of the aperiodic amplifier stage.

Measured parameters at meaning resistance R1 - 1 kOhm				
***I* b** , [μA]	***I* k** , [mA]	**U be** , [mV]	**U ke** , [IN]	**U Rk** , [B]
Measured parameters at established meaning resistance R1				
***I* b** , [μA]	***I* k** , [mA]	**U be** , [mV]	**U ke** , [IN]	**U Rk** , [B]
Measured parameters at meaning resistance R1 + 1 kOhm				
***I* b** , [μA]	***I* k** , [mA]	**U be** , [mV]	**U ke** , [IN]	**U Rk** , [B]

Table 13 - Calculated parameters By variable current aperiodic amplification stage.

Calculated parameters at meaning resistance R1 - 1 kOhm					
***R* in** , [Ohm]	***R* out** , [Ohm]	***G*** , [A/B]	***K* I**	***K* U**	**KGI, %**
Calculated parameters at established meaning resistance R1					
***R* in** , [Ohm]	***R* out** , [Ohm]	***G*** [A/B]	***K* I**	***K* U**	**KGI, %**
Calculated parameters at meaning resistance R1 + 1 kOhm					
***R* in** , [Ohm]	***R* out** , [Ohm]	***G*** , [A/B]	***K* I**	***K* U**	**KGI, %**

– do conclusion O volume, How have changed variables currents And voltage V amplification cascade with decreasing and increasing resistance ***R* 1** ;

– for both cases, use an oscilloscope to obtain oscillograms of the output signals, A With help Fourier analyzer their spectra, which bring in V report By laboratory work;

– define And evaluate, How changed qualitative indicator (KGI) amplifier stage, in which of the two cases did signal distortions occur and why;

– analyze And define, How How have changed entrance And weekend parameters by variable current, A Also coefficients transmissions at decrease And increase resistance ***R* 1** .

2.3.6) Conduct a study of the effect of the ***R2 resistance in the voltage divider circuit on the transistor's quiescent mode, input and output parameters,* and** the DC gain of the amplifier stage. To do this, perform the following steps:

– turn off the input signal and switch the ammeters and voltmeters to the constant value measurement mode;

– bring in measured previously values parameters (from table 7) configured amplifier stage (with the set resistance value ***R2) in the idle mode in Table* 14** , and the previously calculated parameters (from Table 8) in Table 15;

– change the value of resistance ***R* 2** to 300 Ohm, first decreasing it and then increasing it;

– For both cases produce measurements And calculation given parameters, enter the results in tables 14 and 15;

– do conclusion O volume, How have changed constant currents And voltage V amplification stage in the idle mode with decreasing and increasing resistance ***R* 2** ;

Table 14 – Measured direct currents and voltages in the aperiodic amplifier cascade in rest mode

Measured parameters at meaning resistance R2 - 300 Ohm						
***I* 1** , [mA]	***I* 2** , [mA]	***I* b0** , [μA]	***I* k0** , [mA]	**U be0** , [mV]	**U ke0** , [IN]	**U Rk0** , [V]
Measured parameters at established meaning resistance R2						
***I* 1** , [mA]	***I* 2** , [ma]	***I* b0** , [μA]	***I* k0** , [mA]	**U be0** , [mV]	**U ke0** , [IN]	**U Rk0** , [V]
Measured parameters at meaning resistance R2 + 300 Ohm						
***I* 1** , [mA]	***I* 2** , [mA]	***I* b0** , [μA]	***I* k0** , [mA]	**U be0** , [mV]	**U ke0** , [IN]	**U Rk0** , [V]

Table 15 - Calculated parameters aperiodic amplifying cascade V mode for peace.

Calculated parameters at meaning resistance R2 - 300 Ohm			
***R* in0** , [Ohm]	***R* out0** , [Ohm]	***K* I0** ,	***G* 0** , [A/B]
Calculated parameters at established meaning resistance R2			
***R* in0** , [Ohm]	***R* out0** , [Ohm]	***K* I0** ,	***G* 0** , [A/B]
Calculated parameters at meaning resistance R2 + 300 Ohm			
***R* in0** , [Ohm]	***R* out0** , [Ohm]	***K* I0** ,	***G* 0** , [A/B]

– analyze and determine how the position of the operating point on the output and input characteristics of the transistor changed with a decrease and increase in resistance R2 **. To** do this, use the graphs in Fig. 3 and 4 as an example;

– analyze and determine how the input and output parameters have changed , coefficient transmissions By permanent current at decrease And increase resistance ***R* 2** .

2.3.7) Conduct a study of the influence of the resistance value **R2** in the voltage divider circuit on the input and output parameters for alternating current, transmission coefficients And qualitative indicator amplifying cascade. WITH this purpose execute the following actions:

– turn on input signal And translate ammeters And voltmeters V mode measurements of variable quantities;

– enter the previously measured values of the parameters for alternating current (from Table 9) of the configured amplification stage (at the established resistance value ***R* 2**) in Table 16, and the previously calculated parameters (from Table 9) in Table 17;

– change the value of resistance ***R* 2** to 300 Ohm, first decreasing it and then increasing it;

– For both cases produce measurements And calculation given parameters, enter the results in tables 16 and 17;

Table 16 – Measured parameters for alternating current of the aperiodic amplifier stage.

Measured parameters at meaning resistance R2 - 300 Ohm				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]
Measured parameters at established meaning resistance R2				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]
Measured parameters at meaning resistance R2 + 300 Ohm				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]

Table 17 - Calculated parameters By variable current aperiodic amplification stage.

Calculated parameters at meaning resistance R2 - 300 Ohm					
R_{in}, [Ohm]	R_{out}, [Ohm]	G, [A/B]	K_I	K_U	**KGI, %**
Calculated parameters at established meaning resistance R2					
R_{in}, [Ohm]	R_{out}, [Ohm]	G, [A/B]	K_I	K_U	**KGI, %**
Calculated parameters at meaning resistance R2 + 300 Ohm					
R_{in}, [Ohm]	R_{out}, [Ohm]	G, [A/B]	K_I	K_U	**KGI, %**

– do conclusion O volume, How have changed variables currents And voltage V amplification cascade with decreasing and increasing resistance R_2 ;

– for both cases, use an oscilloscope to obtain oscillograms of the output signals, A With help Fourier analyzer their spectra, which bring in V report By laboratory work;

– define And evaluate, How changed qualitative indicator (KGI) amplifier stage, in which of the two cases did signal distortions occur and why;

– analyze And define, How How have changed entrance And weekend parameters by variable current, A Also coefficients transmissions at decrease And increase resistance R_2 .

2.3.8) Conduct a study of the influence of the collector resistance R_K The load line slope, output parameters, and DC gain of the amplifier stage are all affected. To do this, perform the following steps:

– turn off the input signal and switch the ammeters and voltmeters to the constant value measurement mode;

– bring in measured previously values parameters (from table 7) configured leg amplifier cascade (at established meaning collector resistance R_K) V mode rest in table 18, and the previously calculated parameters (from table 8) in table 19;

– change the value of resistance R_K , first decreasing it by 2 times, and then increasing it successively by 1.5 and 2 times;

– for three cases, carry out measurements and calculations of the specified parameters, enter the results in tables 18 and 19;

Table 18 – Measured direct currents and voltages in the aperiodic amplifier cascade in rest mode

Measured parameters at meaning resistance 0.5 R_K				
I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [B]	U_{Rk0}, [V]
Measured parameters at established meaning resistance R_K				
I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [B]	U_{Rk0}, [V]
Measured parameters at meaning resistance 1.5 R_K				
I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [B]	U_{Rk0}, [V]
Measured parameters at meaning resistance 2 R_K				
I_{b0}, [μA]	I_{k0}, [mA]	U_{be0}, [mV]	U_{ke0}, [B]	U_{Rk0}, [V]

Table 19 - Calculated parameters aperiodic amplifying cascade V mode for peace.

Calculated parameters at meaning resistance 0.5 R_K			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]
Calculated parameters at established meaning resistance R_K			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]
Calculated parameters at meaning resistance 1.5 R_K			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]
Calculated parameters at meaning resistance 2 R_K			
R_{in0}, [Ohm]	R_{out0}, [Ohm]	K_{I0},	G_0, [A/B]

– do conclusion O volume, How have changed constant currents And voltage V amplification stage in the idle mode with decreasing and increasing collector resistance R_K;

– analyze And define, How How has changed steepness lines loads transistor with direct current with decreasing and increasing collector resistance R_K. To do this, use the graph in Fig. 3 as an example;

– analyze and determine how the input and output parameters , the DC transfer coefficient have changed with a decrease and increase in the collector resistance R_K.

2.3.9) Conduct a study of the influence of the collector resistance R_K on the input and output parameters for alternating current, the gain coefficients and the quality indicator of the amplifier stage. To do this, perform the following steps:

– turn on input signal And translate ammeters And voltmeters V mode measurements of variable quantities;

– enter the previously measured values of the parameters for alternating current (from Table 9) of the tuned amplifier stage (with the set value of the collector resistance R K) into Table 20, and the previously calculated parameters (from Table 9) into Table 21;

– change the value of resistance R_K, first decreasing it by 2 times, and then increasing it successively by 1.5 and 2 times;

– for three cases, carry out measurements and calculations of the specified parameters, enter the results in tables 20 and 21;

Table 20 – Measured parameters for alternating current of the aperiodic amplifier stage.

Measured parameters at meaning resistance 0.5 R_K				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]
Measured parameters at established meaning resistance R_K				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]
Measured parameters at meaning resistance 1.5 R_K				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]
Measured parameters at meaning resistance 2 R_K				
I_b, [μA]	I_k, [mA]	U_{be}, [mV]	U_{ke}, [IN]	U_{Rk}, [B]

Table 21 - Calculated parameters By variable current aperiodic amplification stage.

Calculated parameters at meaning resistance 0.5 R_K					
R_{in}, [Ohm]	R_{out}, [Ohm]	G, [A/B]	K_I	K_U	**KGI, %**
Calculated parameters at established meaning resistance R_K					
R_{in}, [Ohm]	R_{out}, [Ohm]	G [A/B]	K_I	K_U	**KGI, %**
Calculated parameters at meaning resistance 1.5 R_K					
R_{in}, [Ohm]	R_{out}, [Ohm]	G, [A/B]	K_I	K_U	**KGI, %**
Calculated parameters at meaning resistance 2 R_K					
R_{in}, [Ohm]	R_{out}, [Ohm]	G, [A/B]	K_I	K_U	**KGI, %**

– do conclusion O volume, How have changed variables currents And voltage V amplification stage with decreasing and increasing collector resistance R_K;

– analyze And define, How How has changed steepness lines loads transistor with alternating current with decreasing and increasing collector resistance R_K. To do this, use the graph in Fig. 3 as an example;

– For three cases With help oscilloscope get oscillograms weekend signals , A With help Fourier analyzer their spectra, which bring in V report By laboratory work;

– define And evaluate, How changed qualitative indicator (KGI) amplifier stage, in which of the 3 cases did signal distortions occur and why;

– analyze And define, How How have changed entrance And weekend parameters for alternating current, as well as transmission coefficients with decreasing and increasing collector resistance R_K.

2.4) ***Do generalizing conclusions*** By results conducted research aperiodic amplifying cascade.

<u>Task 5. (for independent work)</u> Present the research results in the form of a laboratory report and defend it.

5.1) IN report By laboratory work display:

– topic and target work, tasks For research And brief order their execution;

– produced calculations studied amplifying cascades;

– simulated V editor schematic modeling basic electrical circuit diagrams of the studied amplifier stages;

– oscillograms input and weekend signals;

– graphs frequency response With results measurements border frequencies gain bands ;

– results studies in the form of tables with measured and calculated parameters of the studied amplifier stages;

– spectrograms of output signals, with the help of which the harmonic distortion coefficient was determined;

– conclusions By results execution tasks And V in general By work done .

5.2) Defend a report on the completed laboratory work by completing an individual assignment specified by the teacher, within the framework of the research conducted.

Control questions For preparation To protection:

1) How install modes work cascade By permanent And variable currents so that nonlinear distortions of the output signal are minimal?

2) What way define voltage on base transistor at given position of the resting point?

3) Under what conditions are constant potentials set at the collector and emitter of a transistor in the quiescent mode?

4) Justify justice schemes substitutions cascade OE By alternating current.

5) Thanks to what properties transistor provided signal amplification by current and voltage?

6) How is being formed signal OOS By permanent current With help resistor Re in the laboratory setup diagram?

7) What is it like? appointment dividing capacitors V scheme amplifier?

8) Why is the current and voltage gain of the cascade the lowest at the lower frequency of the $f_н$ range?

9) What kind reasons conditioned by decline frequency response V top frequency range ?

10) Why on average frequencies range coefficients transmissions amplifier By current and voltage remain practically unchanged?

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 5

Subject: **STUDY POWER AMPLIFIERS**

Time – 4 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– realize circuit design (computer) modeling amplifiers capacity using universal software packages;

– to conduct a study of the main parameters and characteristics of the amplifying device - a push-pull power amplifier and a power amplifier with transformer coupling;

– collection and analysis of information to generate initial data for the design of electronic amplifying devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program schematic editor Electronics Workbench (EWB) simulation , version 5.12 or later, or NI Multisim Education version;

– application for mathematical and engineering calculations Mathcad Professional version not lower than 15.0;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Modeling two-stroke power amplifier .	25 min
2. Study two-stroke amplifier power.	45 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**65 min**
3. Modeling amplifier power With transformer communication.	20 min
4. Study amplifier power With transformer communication.	45 min
The final part	**15 min**
Defense of practical work reports	10 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

1. General Provisions

An electronic amplifier is a device that converts a low-power electrical signal at the input into a higher-power signal at the output with minimal distortion. These amplifiers are called electronic because the operating principle used in them amplifying elements (transistors, (electronic tubes, integrated circuits , thyristors and other devices) is based on electronic processes occurring in a semiconductor or vacuum.

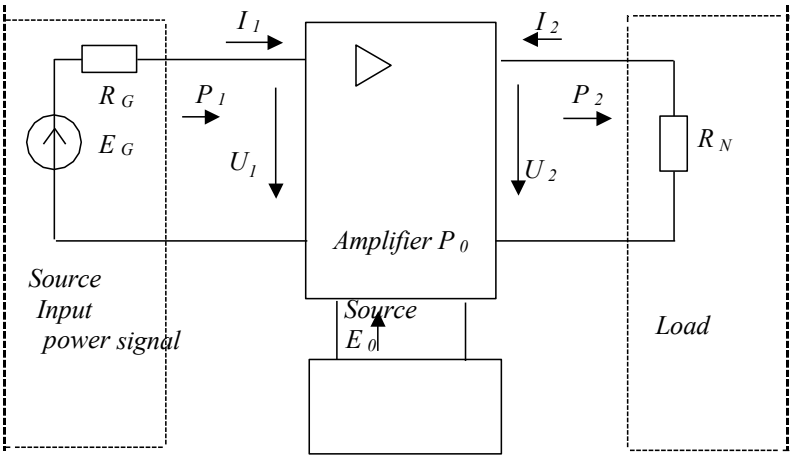
A power amplifier is called amplifier, designed For provision given load power Pн at a given load resistance RH. A power amplifier is an example of power electronics devices. The main goal in developing such devices is consists of V volume, to hand over load given power. IN amplifier The active device can be a bipolar transistor, a field-effect transistor, or a vacuum tube.

By principle actions amplifiers power Not differ from amplifiers voltage (current), however mode their work is selected So, to get on exit the greatest power , not the highest voltage.

Big power means work With large currents And voltages, which significantly exceed voltage And currents V amplifiers voltage. If V amplifiers voltage usually uses only a small section of the characteristic of the active device, then in power amplifiers they always strive to make the most of its entire characteristic, What leads To noticeable increase nonlinear distortions. From here flows out the need to evaluate nonlinear distortions of a power amplifier.

The signal power is increased by consuming energy from the amplifier. additional source, called source nutrition. Hence, the amplifier represents by yourself device, input signal whom controls transformation The energy of the power source is converted into the energy of the output signal. This conversion is accomplished using the active elements of the amplifier (amplifying elements). The amplifier's output electrical signal is fed to a device called a load. The relationship between the amplifier, the input signal source, the load, and the power source is shown in Figure 1.

microphone, can act as an input signal source , photocell, thermocouple And etc., A Also preceding amplifier, because The gain provided by a single amplifying element is often insufficient for practical purposes. Then, several amplifying elements are used in the amplifier, connected in such a way in this way, What reinforced first element signals are served on entrance second, amplified by the second - to the input of the third, etc. In this case, one amplifying element and the coupling elements assigned to it are called a cascade. Most amplifiers are multi-cascade .



Rice. 1 Generalized scheme amplifying device

The operating conditions of a power amplifier depend on the nature of the load and its constancy. In general, the load resistance is complex. For transmission, it is possible greater power V load should be completed coordination between resistance loads And internal resistance active device. Most A common matching device is a transformer.

The load can be a telephone, a speaker, various oscilloscope systems , a relay, an electric motor, a communication channel, etc., as well as a subsequent amplifier.

At use V amplifier power bipolar transistor most The most common configuration is the common-emitter configuration, which provides the highest signal gain and therefore requires less output power from the preamplifier and the lowest gain from the preamplifier. Connecting a common-base transistor reduces nonlinear distortion and improves the stability of all circuit parameters. However, with this configuration, the input conductance of the power amplifier is high, and the preamplifier must be designed with a transformer load.

Power amplifier transistors operate in large-signal mode, when the amplitudes of the alternating current and voltage components are quite large. This exposes the transistors' nonlinear properties to significant effect, resulting in nonlinear distortion of the input signal.

Level nonlinear distortions amplifier power significantly depend from the initial operating mode, and nonlinear distortions are caused by the nonlinearity of not only the input but also the output characteristics of the transistors, since they operate in large signal mode. The minimum possible level of nonlinear distortions can be ensured V mode class "A", A maximum possible Efficiency — V mode classes "IN" or "AB" Amplifiers power there are single-stroke And two-stroke, and first they work V class "A" mode, and the latter - in class "B" or "AB" mode. Single-ended power amplifiers are used at relatively low output powers.

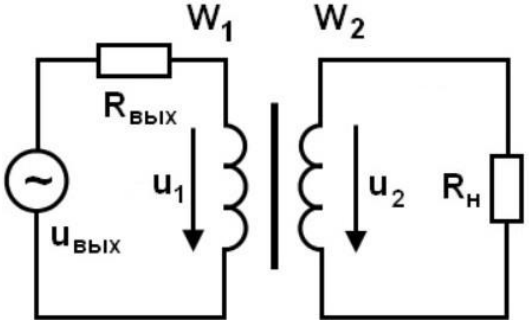
In accordance with the requirement to ensure a specified load power Pn, when developing a power amplifier, the issue of the appropriate choice of amplifier supply voltage E must be resolved. Let us assume that an amplifier with the specified supply voltage can create a sinusoidal signal with the maximum possible voltage amplitude on the load . Then the maximum possible load power $P_{n\,max}$ will be determined by the expression

$$P_{n\,max} = \left(\frac{U_m}{\sqrt{2}}\right)^2 \frac{1}{R_n} = \frac{U_m}{2R_n} = \frac{E^2}{8R_n},$$

where $U_m = \frac{E}{2E} = 2\sqrt{P_{n\,max} 2R_n}$

If By any reasons choose received meaning E Not seems to be WHO-possible, For approvals amplifier And loads Can use transformer. However, a transformer is often an undesirable element of a power amplifier, as it is a relatively expensive and difficult to manufacture device.

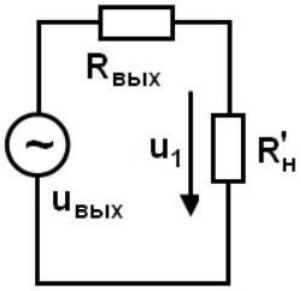
Let's consider coordination loads And amplifier With help transformer (rice. 2).



Drawing 2 - Coordination with load through a transformer

Through W1 And W2 designated respectively quantity turns primary And secondary windings of the transformer, and through u output and R out — respectively, the output voltage and - output resistance of the amplifier.

When determining the load power, this circuit can be replaced by the equivalent circuit shown in Fig. 3.



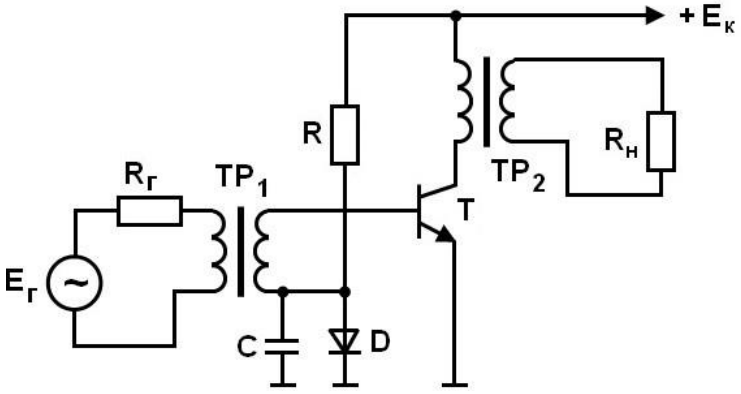
Drawing 3 - Equivalent scheme substitutions

IN her through R′ n designated given resistance loads R′ n = R n / n 2 Where n — transformation ratio (n = W2 / W1).

By changing the transformation ratio, the required amplifier matching can be achieved. And loads, and it is known, What maximum power V the load is given at R output = R′ n . From here we determine the optimal value of the transformation ratio:

$$n_n = \sqrt{\frac{R_n}{R_{вых}}}$$

In transformer power amplifiers, transistors are most often connected according to the circuit With common emitter. The simplest option schemes single-stroke transformer The power amplifier - with such a transistor connection is shown in Figure 4.



Drawing 4. Single-stroke circuit diagram transformer power amplifier

IN this scheme applied thermal stabilization current bases, So How inclusion V chain emitter significant resistance impossible because of big quantities weekend current. Therefore , DC feedback is ineffective and does not ensure stability of the mode.

The primary winding of the transformer serves as the collector load of the transistor. Its resistance to the alternating component of the collector current is high and depends on the - coefficient transformations transformer And quantities loads, connected ko secondary winding.

The frequency properties of an amplifier determine its bandwidth and linear response level . (frequency) distortion of the signal at its output. Frequency analysis properties can be conveniently calculated using an equivalent circuit.

Contents of the practical work performed students V in the course classes

Description laboratory equipment:

- PC for each student;
- program editor schematic modeling Electronics Workbench" (EWB) version no lower than 5.12 or NI Multisim Education version;
- Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher.

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) In case of emergency situations, it is necessary to immediately disconnect the equipment from the power supply, inform the teacher about this and act according to his instructions .

6) If equipment catches fire, it must be immediately de-energized, the teacher must be informed, measures must be taken to eliminate the fire, and the teacher must act as instructed.

7) By ending work With laboratory equipment (computers) his must be switched off in the established order.

Tasks to be completed during practical work

Tasks basic level:

1) Modeling And study characteristics of a two-stroke power amplifier

Tasks increased level:

2) Modeling and study of the characteristics of a transformer- coupled power amplifier

Order execution work

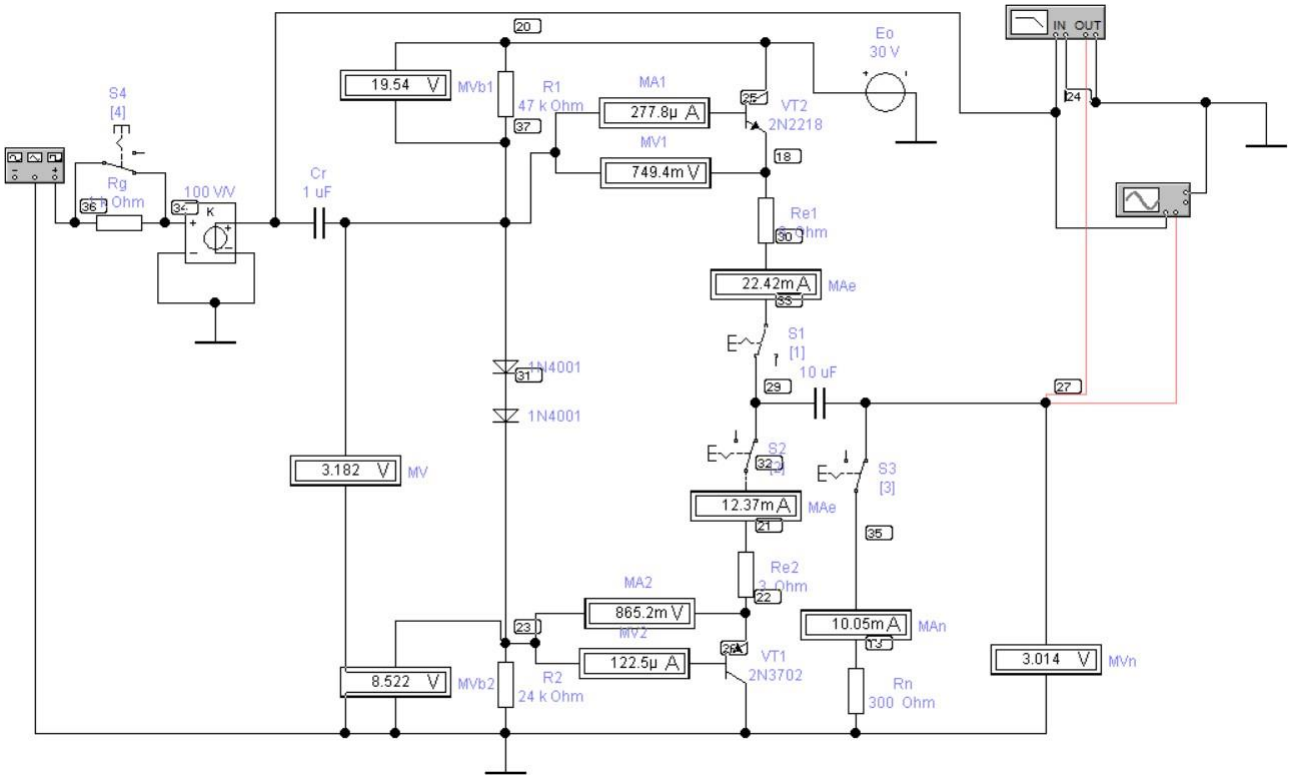
Exercise 1. Modeling And study characteristics two-stroke power amplifier .

Problem and initial data of the simulation . In this task, two operating modes of the preamplifier are studied: without load (idle) and with load ($R_н$ = 300 Ohm). At this To amplifier connects or ideal source signal whose internal resistance is 0, or a real current source with a resistance of 1 kOhm. The amplifier must provide an output voltage equal to Uout and equal to Uin. The task requires the following actions to be performed at a center frequency of fcp = 10 kHz:

- take off oscillograms input And weekend signal, define introduced they have a phase shift in the output signal,
- define primary And secondary amplifier parameters ;
- evaluate transmission (amplifying) properties By tension, By current And By power-nost

Order circuit design modeling.

1)Collect diagram, presented on drawing 5.



Rice. 5 - Scheme two-stroke amplifier power

1.1) Install V collected scheme values quantities elements, How shown on rice.

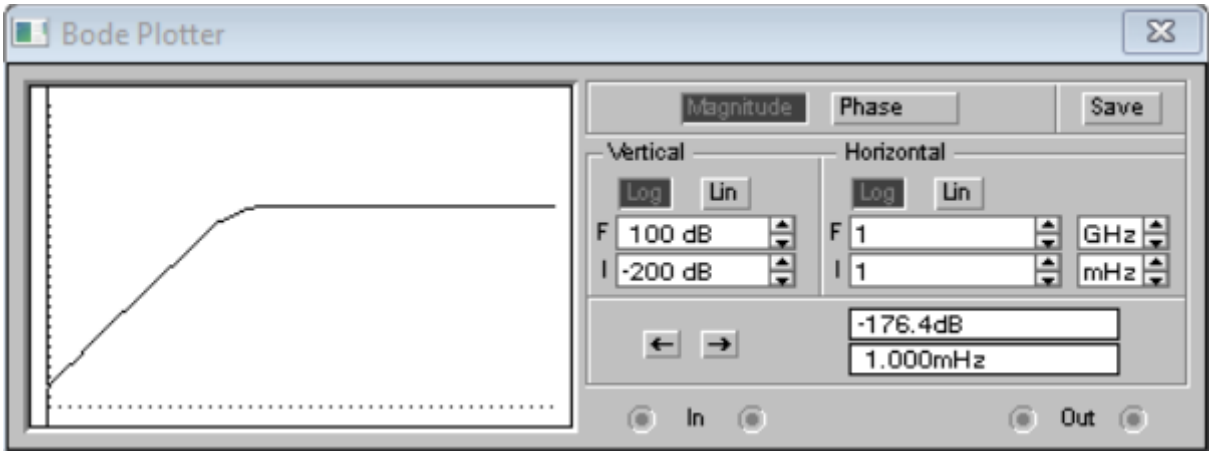
5. IN functional generator install frequency input signal 10 kHz, A amplitude **Eg** =10 mV. Keys **S1** And **S2, S3** And **S4** install V provisions, How shown on Fig. 5.

2) Check performance schemes. For this activate work schemes button located in the upper right corner of the screen. If the circuit is operating correctly, the variable voltmeters and ammeters will show the values shown in Figure 5, respectively.

3) Get oscillogram, having set up oscilloscope So, to on his screen 3-4 oscillation periods were displayed, and the signal amplitudes were approximately equal. The resulting time diagram should be included in the laboratory report.

4) Next take off frequency response And Phase-frequency response. For this necessary

- launch double click left button mice Bode plotter;
- V opened dialogic window, choose mode work Magnitude, This means, that the Bode plotter will operate in frequency response meter mode;
- V frame Vertical choose linear scale By axes amplitudes, And install upper and lower threshold values F=100, I=-200.
- in the Horizontal frame, select the logarithmic scale along the frequency axis, and set the upper and lower threshold values F=1 GHz, I=1 mHz.
- activate the circuit using the button located in the upper right corner of the screen; Bode plotter will display the amplifier's frequency response on its screen (example in Fig. 6);
- bring in received frequency response V report according to PZ ;
- install V Bode plotter mode work Phase, having translated his in mode Frequency response meter;
- V frame Vertical For linear scale By axes amplitudes install values the top and bottom thresholds F= 180 degrees, I= -45 degrees;
- bring in received phase response V report according to PZ .



Drawing 6 – Example of setup Bode plotter

6) Order actions at conducting measurements primary parameters amplifier:

6.1) Close key S4 So, to short-circuit internally resistance generator Rg, thereby making it equal to zero, as in an ideal EMF source (see Fig. 1).

6.2) Unlock key "S3", turning off at this load, those the most having installed idle mode, when $R_H = \infty$.

6.3) Results of measurements of E_G, U_{BX} and U_{EXIT} For this case, the ideal EMF source (Rg=0) and the disconnected load are entered into Table 1. (U_{IN} is taken from the voltmeter MV, and U_{OUT} – with MVn).

6.4) Calculate the coefficient K gain by voltage, through coefficient amplification K_E. Received results bring in V table 1. For this take advantage of formulas:

$$K = \frac{U_{out}}{U_{in}}, K_E = \frac{U_{out}}{E_G},$$

Table 1 - Results measurements And experimental calculations.

Parameters	E_G, mV	U_{vx}, In	U_{output}, In	K	K_E
Rg = 0					
Rg = 1 Om					
Rg = 0.5 kΩ					
Rg = 2 kΩ					

6.6) Repeat the measurements with the X key open, thereby connecting the internal - resistance of the generator Rg = 1.0 kOhm; determine the value of Eg at which the output voltage of the amplifier will be U_{OUTPUT} = 300 mV.

6.7) Repeat All measurements For both cases (Rg = 1.0 kOhm And Rg = 0) With with the load disconnected and enter the results into Table 2.

Table 2 - Results measurements And experimental calculations.

Parameters	E_G, mV	U_{in}, IN	U_{out}, IN	K	K_E
Rg = 0					
Rg = 1 Ohm					
Rg = 0.5 kOhm					
Rg = 2 kOhm					

7) The procedure for carrying out experimental calculations of the primary and secondary - parameters of the amplifier:

7.1) Calculate the experimental values of the input and output currents I_{in} and I_{output}, - coefficients gains current And power K_I And K_R For situations With real source signal (Rg = 1.0 kOhm) of the connected and disconnected load, investigated in the previous paragraph 6).

For this V package For mathematical And engineering calculations Mathcad Professional enter the initial data for calculations and write down the formulas for calculation:

$$I_{\text{вх}} = \frac{E_{\text{г}} - U_{\text{вх}}}{R_{\text{г}}},\ I_{\text{вых}} = \frac{U_{\text{вых}}}{R'_{\text{н}}},$$

где
$$R'_{\text{н}} = \begin{cases} \dfrac{R_{\text{к}} R_{\text{н}}}{R_{\text{к}} + R_{\text{н}}}, & \text{if } R_{\text{н}} = 360\ \text{Ом} \\ R_{\text{к}}, & \text{if } R_{\text{н}} = \infty \end{cases},$$

$$K_I = \frac{I_{\text{вых}}}{I_{\text{вх}}},\ K_{\text{р}} = K \cdot K_I.$$

The results obtained are entered into Table 3. Table 3 – Results of experimental calculations.

Parameters	I_{in}, mA	I_{out}, mA	K_I	K_P
With load				
Rg = 0				
Rg = 1 Ohm				
Rg = 0.5 kOhm				
Rg = 2 kOhm				
No load				
Rg = 0				
Rg = 1 Ohm				
Rg = 0.5 kOhm				
Rg = 2 kOhm				

Calculate for the established operating mode the experimental values of the secondary - parameters **R in , R out , h 11** and **Y 22** amplifier, using the data from tables 2 and 3. For this V package For mathematical And engineering calculations Mathcad Professional enter the initial data for the calculations and write down the formulas for the calculations:

- input and output resistances:

$$R_{\text{in}} = \frac{U_{\text{in}}}{I_{\text{in}}}, R_{\text{out}} = R_{\substack{\text{n=300} \\ \text{Ohm}}} \left(\frac{U_{\text{out}\,R\text{н}=\infty}}{U_{\text{out}\,R\text{н}=300}} - 1\right);$$

-own input resistance of the amplifying element:

$$h_{11} = \frac{R_{\text{in}} R_{\text{b}}}{R_{\text{in}} - R_{\text{b}}}, \text{where } R_{\text{b}} = \frac{R_1 R_2}{R_1 + R_2};$$

- day off conductivity amplifying element:

$$Y_{22} = \frac{R_{\text{to}} - R_{\text{out}}}{R_{\text{out}} R_{\text{to}}};$$

Table 4 - Results experimental calculations.

Parameters	R_{in}, Ohm	R_{out}, Ohm	h_{11}, Ohm	Y_{22}, CM
With load				
No load				

Do conclusions By results conducted research

Disconnect the lower branch of the circuit with transistor VT2 using switch S2, record an oscilloscope trace, and record it in the lab report. Perform the same steps when disconnecting VT1 using switch S1.

Draw conclusions by comparing the obtained timing diagrams with the oscillogram obtained during normal operation of the circuit.

1.2 Study nonlinear distortions

Simulate and investigate nonlinear distortion. To do this, perform the following operations. Return the circuit to its original state in Figure 5. Sequentially change the voltage from 100 mV to the original value and perform the following steps:

– Fix it temporary diagram And bring in her V report.

– Using a Fourier analyzer, determine the harmonic distortion coefficient using the formula:

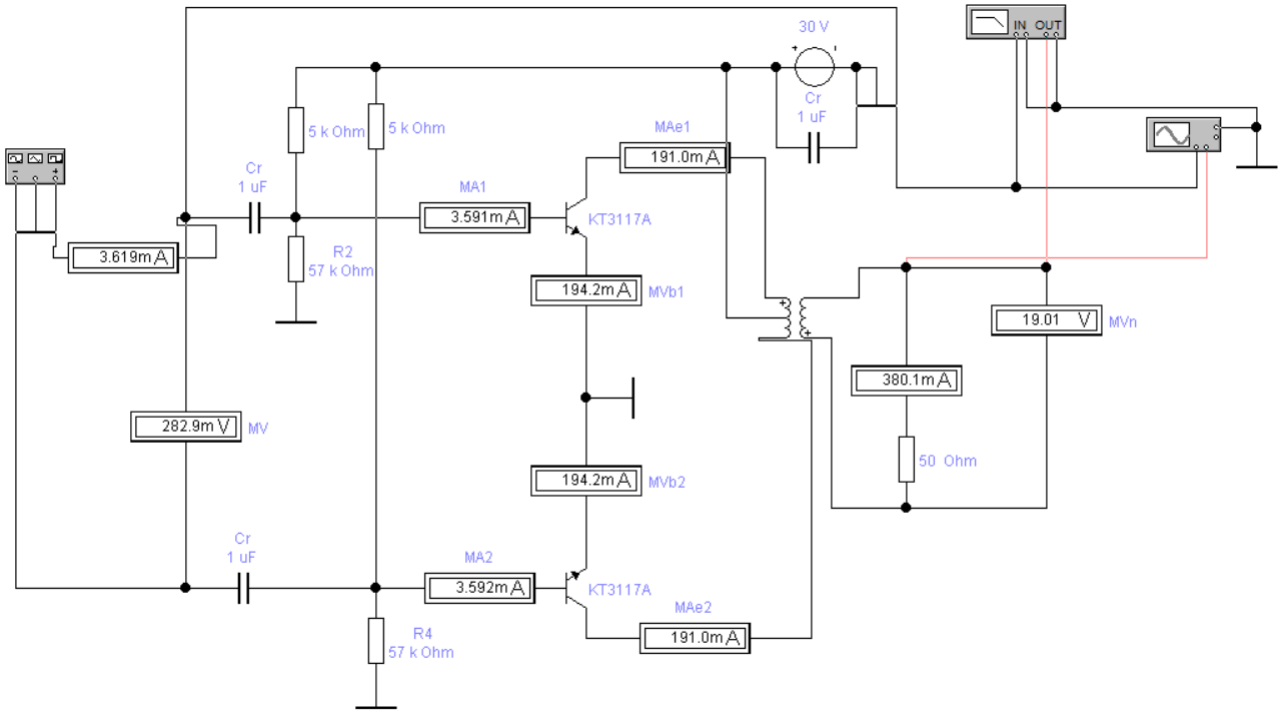
$$K_\Gamma = \frac{\sqrt{U_2^2 + U_3^2 + U_4^2 + \ldots + U_n^2 + \ldots}}{U_1}$$

– Rate amplifying properties.

Do conclusion O volume, How nonlinear distortions influence on amplifying properties of the cascade under study.

<u>Task 2.</u> Modeling and studying the characteristics of a transformer-coupled power amplifier. Order circuit design modeling.

1) Collect diagram, presented on drawing 7.



Rice. 7 - Scheme power amplifier With transformer connection

1.1) Install V collected scheme values quantities elements, How shown on rice. 7. On functional generator install frequency input signal 1 MHz, A amplitude **Eg** =200 mV.

2) Check performance schemes. For this activate work schemes button located in the upper right corner of the screen. If the circuit is operating correctly, the variable voltmeters and ammeters will show the values shown in Figure 7, respectively.

3) Get oscillogram, having set up oscilloscope So, to on his screen 3-4 oscillation periods were displayed, and the signal amplitudes were approximately equal. The resulting time diagram should be included in the laboratory report.

4) Next take off frequency response And Phase-frequency response. For this necessary

- launch double click left button mice Bode plotter;

- V opened dialogic window, choose mode work Magnitude, This means, that the Bode plotter will operate in frequency response meter mode;

- V frame Vertical choose linear scale By axes amplitudes, And install upper and lower threshold values F=200, I=-200.

- in the Horizontal frame, select the logarithmic scale along the frequency axis, and set the upper and lower threshold values F=10 GHz, I=1 Hz.

- activate the circuit using the button located in the upper right corner of the screen; Bode plotter will display the amplifier's frequency response on its screen;

- bring in received frequency response V report according to PZ ;

- install V Bode plotter mode work Phase, having translated his V in the frequency response meter mode ;

- V frame Vertical For linear scale By axes amplitudes install values the upper and lower thresholds F= 225 degrees, I= -180 degrees;

- bring in received phase response V report according to PZ .

5) Calculate coefficient gains K By tension, through coefficient amplification KE. Received results bring in V Table 5. For this take advantage of formulas:

$$K = \frac{U_{\text{out}}}{U_{\text{in}}}, K_E = \frac{U_{\text{out}}}{E_G},$$

Table 5 - Results measurements And experimental calculations.

Parameters	E_G, mV	U_{in}, IN	U_{out}, IN	K	K_E

6) Calculate experimental values input And weekend currents I_{in} And $I'_{\text{m out}}$, current and power gain factors K_I and K_R.

For this V package For mathematical And engineering calculations Mathcad Professional enter the initial data for calculations and write down the formulas for calculation:

$$I_{\text{вх}} = \frac{E_{\text{г}} - U_{\text{вх}}}{R_{\text{г}}}, \; I_{\text{вых}} = \frac{U_{\text{вых}}}{R'_{\text{н}}},$$

где

$$R'_{\text{н}} = \begin{cases} \dfrac{R_{\text{к}} R_{\text{н}}}{R_{\text{к}} + R_{\text{н}}}, & \text{if } R_{\text{н}} = 360 \text{ Ом} \\ R_{\text{к}}, & \text{if } R_{\text{н}} = \infty \end{cases},$$

$$K_I = \frac{I_{\text{вых}}}{I_{\text{вх}}}, \; K_{\text{р}} = K \cdot K_I.$$

The results obtained are entered into Table 6. Table 6 –
Results of experimental calculations.

Options	I_{input}, mA	I_{out}, mA	K_I	K_P

Calculate for the established operating mode the experimental values of the secondary - parameters **R in , R out , h 11** and **Y 22** amplifier, using the data from Tables 5 and 6. For this V package For mathematical And engineering calculations Mathcad Professional enter the initial data for the calculations and write down the formulas for the calculations:

- input and output resistances:

$$R_{\text{in}} = \frac{U_{\text{in}}}{I_{\text{in}}}, R_{\text{out}} = R_{\substack{\text{n=300} \\ \text{Ohm}}} \left(\frac{U_{\text{out } R\text{н}=\infty}}{U_{\text{out } R\text{н}=300}} - 1 \right);$$

-own input resistance of the amplifying element:

$$h_{11} = \frac{R_{\text{in}} R_{\text{b}}}{R_{\text{in}} - R_{\text{b}}}, \text{where } R_{\text{b}} = \frac{R_1 R_2}{R_1 + R_2};$$

- day off conductivity amplifying element:

$$Y_{22} = \frac{R_{\text{to}} - R_{\text{out}}}{R_{\text{out}} R_{\text{to}}};$$

Table 7 – Results of experimental calculations.

Parameters	R_{in}, Ohm	R_{out}, Ohm	h_{11}, Ohm	Y_{22}, CM

Do conclusions By results conducted research. Compare the previously studied amplifier with the one being analyzed during this task.

2.2 Study nonlinear distortions

To simulate and investigate nonlinear distortions, perform the following steps: operations. Return diagram V original state on Figure 7. Install voltage on the generator equal to 10 mV. Consistently change the voltage from 10 mV (the step change is taken as 10 mV) to the initial one and for each voltage value perform the following actions :

– Fix it temporary diagram And bring in her V report;

– Using a Fourier analyzer, determine the harmonic distortion coefficient using the formula:

$$K_{\Gamma} = \frac{\sqrt{U_2^2 + U_3^2 + U_4^2 + \ldots + U_n^2 + \ldots}}{U_1}$$

– Rate amplifying properties.

Compare influence nonlinear distortions two studied amplifiers And do you draw conclusions based on the analysis.

<u>Task 3. (for independent work)</u> Present the research results in the form of a laboratory report and defend it.

3.1) IN report By laboratory work display:

– topic and target work, tasks For research And brief order their execution;

– simulated V editor schematic modeling Schematic diagrams of the amplifiers under study;

– oscillograms input and output signals;

– graphs frequency response With results measurements frequency parameters;

– results studies in the form of tables with measured and calculated parameters of the amplifiers under study;

– conclusions By results execution tasks And V in general By work done .

3.2) Defend a report on the completed laboratory work by completing an individual assignment specified by the teacher, within the framework of the research conducted.

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 6

Subject: STUDY OPERATING AMPLIFIERS

Time – 4 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– realize circuit design (computer) modeling operating amplifiers with various connection schemes using universal packages of applied computer programs;

– conduct research into the operating principles, main characteristics and parameters of operational amplifiers in various connection schemes;

– collection and analysis of information to form initial data for the design of electronic amplifying devices based on operational amplifiers.

Competencies, being formed V in the course laboratory work

OPK-4: ability have skills independent work on computer And V computer networks, to carry out computer modeling of devices, systems and processes using universal packages of computer application programs.

PC-8: ability to collect and analyze information to generate initial data for the design of communication facilities and networks and their elements.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study parameters And characteristics operating amplifiers.	30 min
2. Study principles work, parameters And characteristics non-inverted tating amplifier.	45 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**65 min**
3. Study principles work, parameters And characteristics invert-amplifier .	40 min
4. Study features work And parameters differential amplifier.	25 min
The final part	**15 min**
Defense of practical work reports	10 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

Integral operating amplifier (OU) characterized by near parameters, describing this component With points vision quality execution them their own functions. Among Of the parameters usually given in reference data, the main ones are the following.

1) ***Average input current I*** **in** . In the absence of a signal at the inputs of the op amp, through its input terminals are leaking currents, conditioned basic currents input bipolar transistors or currents leaks shutters For OU With field transistors on at the entrance. ***Entrance currents, passing - through the internal resistance of the input signal source, they create voltage drops on at the entrance OU, which can call appearance voltage on exit V from absence signal on at the entrance*** . Compensation this falls voltage difficult those, What The input currents of real op amps can differ from each other by 10...20%. ***The input currents of op amps can be estimated by the average input current, calculated as the arithmetic mean of the currents of the inverting and non-inverting inputs*** :

$$I_{\text{in}} = \frac{I_1 + I_2}{2}, \quad (1)$$

Where I_1 And I_2 respectively currents inverting And non-inverting inputs.

2) ***Difference input currents*** ΔI_{in} . IN reference books indicate module this values. The difference in input currents is determined by the expression:

$$\Delta I_{\text{BX}} = |I_1 - I_2|. \quad (2)$$

3) ***DC voltage gain factor K*** **U** – the OU indicator that determines as far as Fine performs OU the main one function - gain input signals . The gain of an ideal amplifier should tend to infinity.

Coefficient gains voltage For schemes inverting amplifier on The OU is calculated using the formula:

$$K_{\text{U}} = -\frac{R_{\text{OS}}}{R_1}, \quad (3)$$

Where - sign "minus" V formula means, What weekend voltage inverting the amplifier is in antiphase with the input voltage.

The voltage gain for a non-inverting amplifier circuit using an op-amp is calculated using the formula:

$$K_{\text{U}} = 1 + \frac{R_{\text{OS}}}{R_1} \quad (4)$$

4) ***Voltage mixing U*** **SM** - meaning voltage, which necessary submit to the input of the op-amp so that the voltage at its output is zero. Bias voltage U_{CM} Can calculate, knowing weekend voltage at absence voltage on at the entrance And voltage gain factor :

$$U_{\text{cm}} = \frac{\Delta U_{\text{out}}}{K_{\text{U}}}. \quad (5)$$

5) ***Input resistance R*** **BX** . Distinguish two components input resistance-niya:

– ***differential input resistance*** . Input differential support-resistance For bipolar OU located usually V within 10 kOhm ... 10 Mohm. The differential input resistance is observed between the inputs of the op amp and ***can be determined by the formula*** :

$$R_{\text{input diff.}} = \frac{\Delta U_{\text{in}}}{\Delta I_{\text{in}}} \quad (6)$$

Where ΔU_{in} - change voltage between entrances OU, ΔI_{in} - change input current;

– ***input resistance By in-phase signal*** (resistance leaks between each input and "ground"). The input common-mode impedance ***is defined as the ratio*** of the increment in the input common-mode voltage to the induced increment in the average input current:

$$R_{\text{in.sf}} = \frac{\Delta U}{\Delta I_{\text{in.avg}}}. \quad (7)$$

6) ***Output resistance R*** **OUT** in integrated op amps it is 20...2000 Ohm. Output resistance reduces amplitude weekend signal, especially at work amplifier , on comparable With him resistance loads. It ***Maybe be defined By formula*** :

$$R_{\text{out}} = \frac{\Delta U_{\text{out}}}{\Delta I_{\text{out}}}. \quad (8)$$

7) ***Speed growth weekend voltage V*** **Uout** equal relation to change weekend voltage OU ΔU_{out} ko time his growth at filing on entrance jump voltage. Time growth is determined interval time t_{mouth} , V current whom weekend voltage OU changes from 10% to 90% from their own established values. Determined by the formula

$$V_{U_{\text{out}}} = \frac{\Delta U_{\text{out}}}{t_{\text{mouth}}}. \quad (9)$$

8) ***Differential coefficient gains*** **To d** - This coefficient gains identical coefficient gains By voltage OU without reverse connections. This is explained the fact that when the differential feedback signals are amplified by the emitter coupling resistor in the differential cascade Not arises (because variable component emitters flows through resistances **R E** in opposite directions). It is determined by the formula:

$$K_{\text{D}} = \frac{\Delta U_{\text{exit}}}{\Delta U_{\text{oh}_{\text{D}}}}, \quad (10)$$

Where **ΔU inD = U in1 - U in 2** - change (difference) input stresses (between two inputs).

9) ***Coefficient gains in-phase voltage*** . This coefficient gains **To sf** is usually small, since the emitter currents flow along **R E** in one direction (for common-mode signals) And arises deep OOS, reducing **To sf** in many once. It is being determined By formula:

$$K_{\text{SF}} = \frac{\Delta U_{\text{out}}}{\Delta U_{\text{in}_{\text{SF}}}}, \quad (11)$$

where $\Delta U_{\text{in}_{\text{SF}}} = \frac{\Delta U_{\text{in1}} + \Delta U_{\text{in1}}}{2}$

This change in common mode voltage coming in to the entrances from the line connections.

10) ***The common mode rejection ratio (CMRR)*** is the main parameter of the differential stage included in the op amp, characterizing the ability to attenuate (not amplify) signals applied to both inputs simultaneously (i.e. in-phase signals). For **To sf** condition **U in1 = U in2** V absolute meaning Not is carried out because resistors, transistors Not adjusted exactly, And appears difference collector stresses **U k1 -U k2** . This effect is minimized, But never Not is eliminated. Respectively, with an asymmetric output there will always be **U out** $\neq 0$ when **U in1 = U in2** (even with a symmetrical input). Reinforced difference And characterized by **To sf** , which must be minimal (A **To the Joint Forces Operation** should be maximum). It is determined by the formula:

$$To_{\text{ the OOS}} = 20 \cdot \lg\left(\frac{K_{\text{D}}}{K_{\text{SF}}}\right), \quad [\, dB \,]. \tag{12}$$

Contents of the practical work performed students V in the course classes

Description laboratory equipment:

– PC for each student;

– program editor schematic modeling Electronics Workbench" (EWB) version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher.

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) At occurrence emergency situations necessary immediately turn off equipment from the power supply networks, report about this to the teacher And act according to him instructions.

6) At fire equipment his necessary immediately de-energize, report about this to the teacher, accept measures By elimination fires And act By instructions pre teacher.

7) Upon completion of work with laboratory equipment (computers) it must be turned off in the established order.

Initial data for research

The task options for individual modeling of operational amplifier circuits and conducting research are presented in Table 1.

Table 1 - Options tasks for research.

No. vari anta	Given model of operational unit	Model OU to replace when and - research	No. vari anta	Given model - OU	Model OU to replace when and research
1	LM 101A	LM 124A	11	LM 218	LM 741
2	LM 107	LM 124	12	LM 307	LM 124A
3	LM 108	LM 741	13	LM 308	LM 741
4	LM 112	LM 124	14	LM 311	LM 124A
5	LM 118	LM 101A	15	LM 318	LM 741
6	LM 124	LM 741	16	LM 324	LM 124A
7	LM 124A	LM 318	17	LM 741	LM 324
8	LM 144	LM 318	18	LM 124A	LM 124
9	LM 158	LM 112	19	LM 318	LM 107
10	LM 208	LM 318	20	LM 107	LM 144

Tasks to be completed during practical work

Tasks basic level:

1) Conduct study parameters operating amplifier By permanent current.

2) Conduct study principles work, parameters And characteristics non- inverting amplifier.

3) Conduct study principles work, parameters And characteristics inverting amplifier.

Tasks increased level:

4) Conduct study features work And parameters differential the force of the litel.

Order execution work

<u>Exercise 1.</u> Conduct study parameters operating amplifier By direct current .

statement :

Initial data For research are given models OU (cm. table 1).

Tasks is being carried out at condition absence reference (passport) data about the educational institution.

IN task necessary For given OU define next his parameters By for direct current:

- input currents displacements;
- coefficient gains voltage;
- bias voltage ;
- input And output resistance;
- time And speed growth weekend voltage.

For this take advantage of typical schemes, providing conducting measurements of the required parameters.

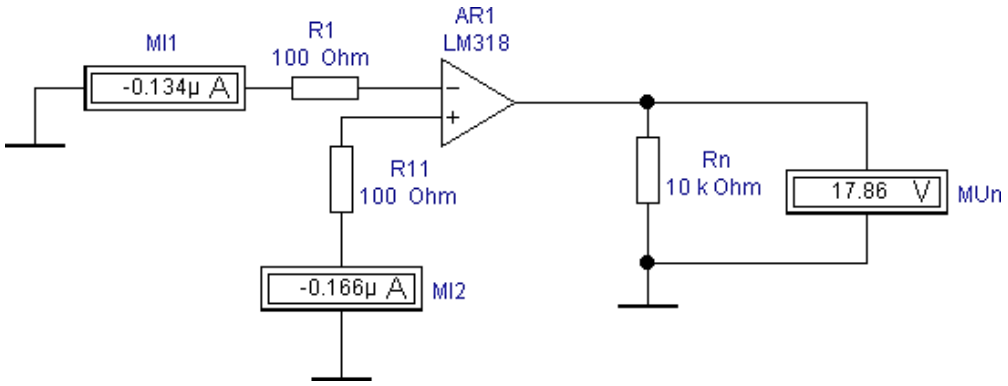
For conducting research scheme should have measuring instruments :

- ammeters For measurements input currents;
- voltmeters For measurements voltage displacements And weekend voltage;
- functional generator For tasks pulsed input impacts;
- oscilloscope for analyzing the output voltage waveform and measuring its settling time;

Order execution tasks 1

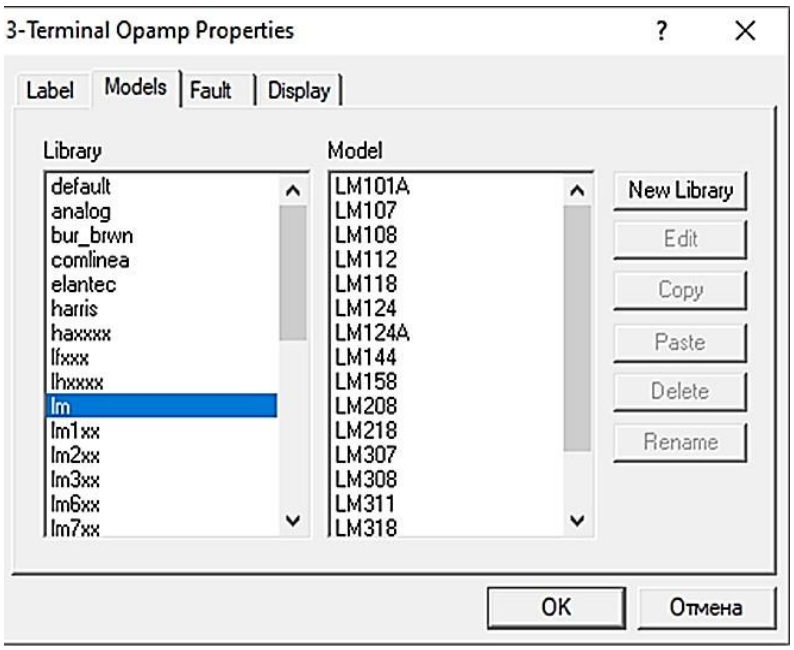
1.1) Define entrance constant currents OU, creating voltage displacement . To do this, perform the following procedures:

1.1.1) Assemble in the EWB program a basic electrical circuit for measuring the input currents of the op-amp, with the parameters input resistances ***R1*** , ***R2*** and load resistance ***Rn*** , as shown in Fig. 6.



Rice. 6 - Scheme for measurement input constants currents OU

1.1.2) Set the specified op-amp model in the assembled circuit by launching the properties window for this purpose. elements, V which find models LM And choose given, How shown on rice. 7:



Rice. 7 – 3-pole operating properties window amplifier.

1.1.3) Install ammeters and set the voltmeters to the DC measurement mode, start program EWB, make sure V availability input currents And permanent voltage at the output of the op amp in the absence of input signals. Include the measurement diagram with the obtained results in the lab report.

1.1.4) Measure the input currents and calculate the parameters that are the op-amp's datasheet—the average input bias current and the absolute value of the input current difference—using formulas (1) and (2). Record the results in the lab report.

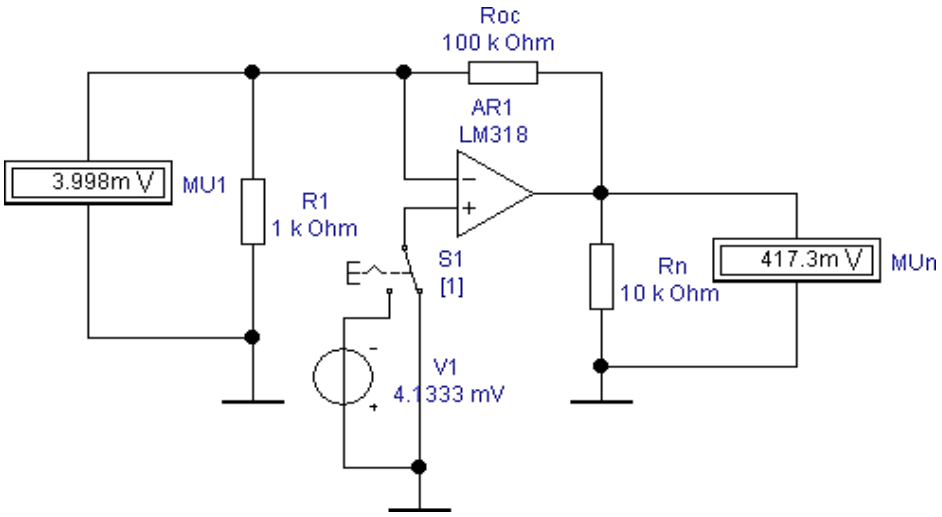
1.1.5) Replace original model OU on another model, indicated V table 1 By your own - version, repeat all measurements and calculations according to point 1.1.4), and also record the obtained results in the laboratory report.

1.1.6) Do conclusions By results conducted research.

1.2) Define coefficient gains voltage By permanent current and bias voltage. To do this, perform the following procedures:

1.2.1) Assemble the circuit diagram of the measurement using the EWB program with the parameters of the input resistance ***R1*** , the feedback resistance ***R* os** and the load resistance ***Rn*** , as shown in Fig. 8. Install the specified op-amp model in the assembled circuit. Set the switch **S1** to the right position, grounding the non-inverting input.

1.2.2) Calculate the theoretical DC voltage gain, taking advantage of formula (3) or (4), bring in received result V report By laboratory work.



Rice. 8 - Scheme for voltage measurements op-amp bias

1.2.3) Install voltmeters V mode measurements permanent quantities, launch about the EWB program, measure the voltages at the input and output of the op amp, enter the measurement diagram with the obtained results into the laboratory report.

1.2.4) Calculate the actual DC voltage gain and include the result in your lab report.

1.2.5) Calculate size voltage mixing, taking advantage of formula (5), to include the obtained result in the laboratory work report.

1.2.6) Set the voltage in the **V1 source** equal to the bias voltage to compensate for it, run the EWB program, make sure that there is a constant voltage on exit OU even at availability voltage compensation on at the entrance. Bring in diagram measurements with the obtained results in the laboratory work report.

1.2.7) Explain what causes the presence of residual voltage at the output of the op amp. Define on what size necessary increase voltage displacements For full compensation of the bias voltage, enter the obtained result in the laboratory report .

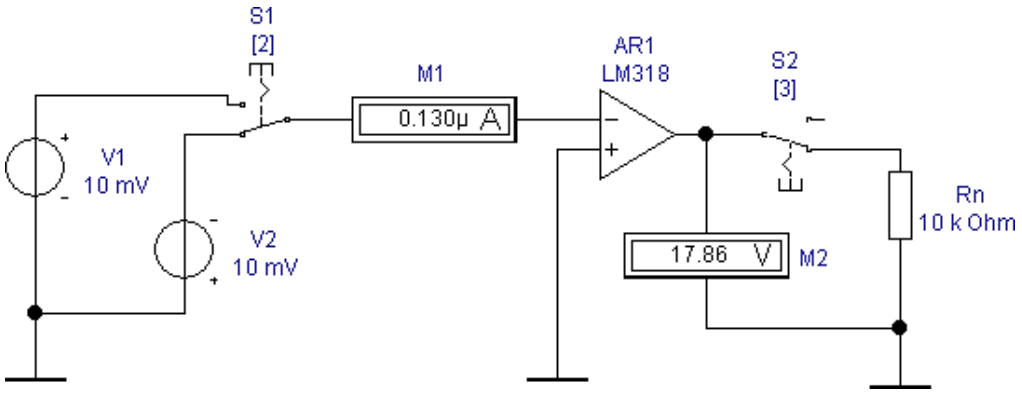
1.2.8) Set the voltage in source **V1** to the value required for full compensation of the offset voltage, at which the DC voltage at the output of the op-amp will not exceed 100 μV. Bring in diagram measurements With received results V report By laboratory work.

1.2.9) Replace original model OU on another model, indicated V table 1 By your own version, repeat all measurements and calculations according to points 1.2.5) – 1.2.8), and also record the obtained results in the laboratory work report.

1.2.10) Do conclusions By results conducted research.

1.3) Define input And weekend resistance OU. For this execute the following procedures:

1.3.1) Collect V program EWB principled electrical diagram measurements with the values of voltage sources **V1** , **V2** and load resistance ***Rn*** , as shown in Fig. 9. Install the specified op-amp model in the assembled circuit. Set switch **S2** to the lower position, connecting the load.



Rice. 9 - Scheme For measurements input And weekend resistances OU

1.3.2) Install ammeter And voltmeter V mode measurements permanent quantities, to run the EWB program, measure the input current $\mathbf{I}_{\mathbf{in}}$ and the output voltage $\mathbf{U}_{\mathbf{out}}$, enter the measurement diagram with the obtained results into the laboratory report.

1.3.3) Switch key **S1** V other position, measure input current $\mathbf{I}_{\mathbf{in}}$ And output voltage $\mathbf{U}_{\mathbf{out}}$ After switching the key, enter the measurement diagram with the obtained results into the laboratory report.

1.3.4) Calculate the change in input voltage $\Delta \mathbf{U}_{\mathbf{in}}$ and current $\Delta \mathbf{I}_{\mathbf{in}}$. Based on the results obtained, calculate differential input resistance $\mathbf{R}_{\mathbf{in.dif}}$ OU, using formula (6), enter the result into the laboratory report.

1.3.5) Turn switches **S1** and **S2** to the up position, disconnecting the load. Measure the output voltage $\mathbf{U}_{\mathbf{out.xx}}$ in idle mode.

1.3.6) To determine the output resistance of the op amp, connect the load resistance. Reduce size resistance $\mathbf{R}_{\mathbf{n}}$ to those pores, Bye weekend voltage $\mathbf{U}_{\mathbf{out}}$ Not will equals half weekend voltage V mode single move, those. $\mathbf{U}_{\mathbf{out}} = \mathbf{U}_{\mathbf{out.xx}}/2$. Received resistance $\mathbf{R}_{\mathbf{n}}$, equal weekend resistance $\mathbf{R}_{\mathbf{out}}$ OU bring in V report for laboratory work.

1.3.7) Replace original model OU on another model, indicated V table 1 By your own version, repeat all measurements and calculations according to points 1.3.2) – 1.3.6), and also record the obtained results in the laboratory work report.

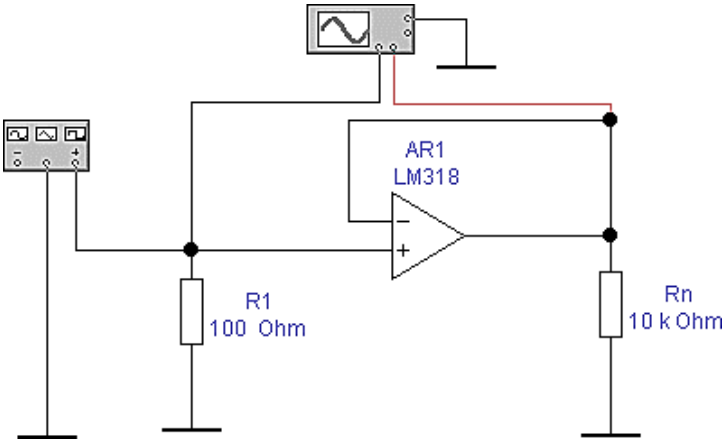
1.3.8) Do conclusions on results of the study.

1.4) Determine the output voltage rise time and rate. To do this, perform the following procedures:

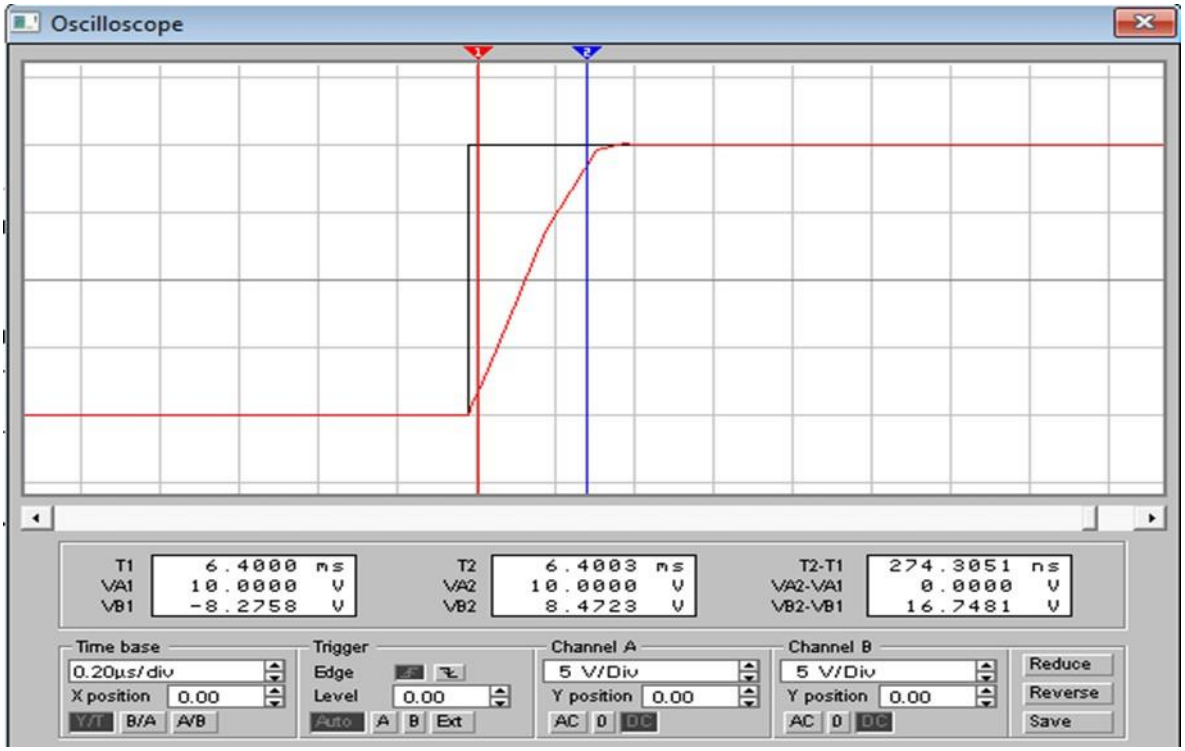
1.4.1) Collect V program EWB principled electrical diagram measurements with resistance values as shown in Fig. 10. Install the specified op-amp model in the assembled circuit.

1.4.2) Set the function generator to rectangular pulse mode with a repetition rate of 5 kHz, a duty cycle of 50%, and a voltage of 10 V.

1.4.3) Connect oscilloscope, So to By first channel conduct analysis input signal, and through the second channel – the output signal. Adjust horizontal (time) and vertical sweep of the oscilloscope on both channels, as shown in Fig. 11.



Rice. 10 - Scheme For time measurements growth weekend op amp voltage



Rice. 11 - Example settings oscilloscope For measurements time growth (setting) the output voltage of the op amp

1.4.4) Launch EWB program, get oscillogram, having view How on Fig. 11, showing the rising edge of the output pulse. Include the oscillogram in your lab report.

1.4.5) Measure the output voltage rise time. To do this, set the first cursor of the oscilloscope to a value approximately equal to **0.1U** $_{out}$, for this schemes measurements - This minus 8 IN, A second cursor approximately on size, equal to **0.9U** $_{out}$, for this measurement circuit this is plus 8 V. Using the oscilloscope's measurement window, determine the magnitude of the change in output voltage Δ **U** $_{out}$ = VB2 – VB1 and its rise time **t** $_{set}$ = T2 – T1. Enter the obtained results in the report for laboratory work.

1.4.6) Calculate the output voltage slew rate of the op amp using formula (9). Convert the result to [V/µs] and include it in the lab report.

1.4.7) Replace original model OU on another model, indicated V table 1 By your own version, repeat all measurements and calculations according to points 1.4.4) – 1.4.6), and also record the obtained results in the laboratory report.

1.4.8) Do conclusions on results of the study.

1.5) Draw conclusions based on the results of the research conducted in the first task, comparing the obtained parameters of the given educational institutions.

<u>Task 2.</u> Conduct a study of the operating principles, parameters and characteristics of a non-inverting amplifier.

statement :

Initial data For research are given models OU (cm. table 1) and their parameters for direct current obtained in task 1.

IN task necessary on base given OU simulate non-inverting amplifier , analyze the principles of its operation, determine and conduct research on the following parameters and characteristics:

- coefficient gains voltage at availability OOS, differential voltage gain factor (without feedback);
- entrance And weekend resistance;
- difference phases between output and input sinusoidal voltage of the op amp;
- voltage displacements And degree influences coefficient gains schemes on constant - component of the output voltage;
- amplitude characteristics (OH), dynamic range And maximum input voltage at which the signal is not subject to nonlinear distortion;
- amplitude-frequency characteristics (frequency response), width stripes gains, gain area and gain cutoff frequency.

For this take advantage of typical schemes, providing conducting measurements of the required parameters.

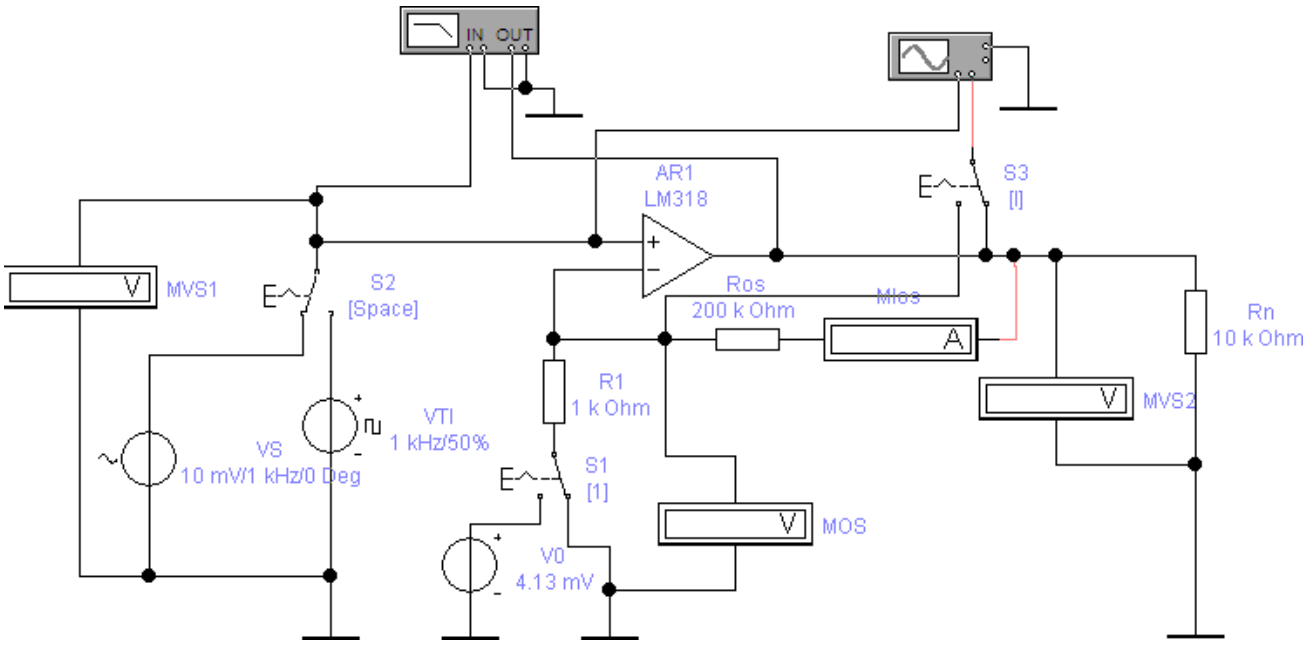
For conducting research scheme should have measuring instruments :

- ammeters And voltmeters For current measurements and stress;
- sources signals For tasks input impacts;
- oscilloscope For analysis forms weekend signals;
- meter frequency response (Bode plotter).

Order execution tasks 2

2.1) Simulate a non-inverting op-amp amplifier circuit. To do this, perform the following procedures:

2.1.1) Collect V program EWB principled electrical diagram non-inverting amplifier with an op-amp with an unbalanced input. Set the op-amp model as indicated in the initial data (Table 1), and the resistance values as shown in Fig. 12, i.e. **Ros** = 200 kOhm, **R1** = 1 kOhm, **Rn** = 10 kOhm.



Rice. 12 - Scheme For research parameters And characteristics of non-inverting amplifier at the educational institution

2.1.2) Install next parameters input signals:

– V source harmonic signal **Vs** - current voltage 10 mV, A frequency – 1 kHz;

– **VTI** pulse signal source – amplitude of 5 mV, pulse repetition frequency of 1 kHz, and pulse duration of 50%;

– in a constant voltage source **V0** is the bias voltage for a given op-amp model, determined in paragraph 1.2) of the previous task.

2.1.3) Schematic switches bring V original position next way:

– key S1 – to the right position (bias voltage source is disconnected);

– key S2 - V left position (connected source harmonic signal);

– key S3 - V right position (second channel oscilloscope connected To load).

2.1.4) All ammeters And voltmeters translate V mode measurements variables great-rank.

2.1.5) Launch simulator programs EWB And check performance schemes. **MVS1** voltmeter should show an input signal voltage of approximately 10 mV, and the **MVS2 voltmeter** should show an output signal voltage of approximately 2 V. Otherwise, the circuit is assembled with errors; find them and fix them.

2.2) To investigate the operating principles, parameters, and characteristics of a non-inverting op-amp amplifier, perform the following procedures:

2.2.1) Conduct measurements, calculations, and analysis of the AC parameters of a non-inverting op-amp amplifier. To do this, perform the following steps:

– calculate the theoretical voltage gain factor **K** $_U$ for the circuit of a non- inverting amplifier on an op-amp, using formula (4), enter the obtained result into Table 2;

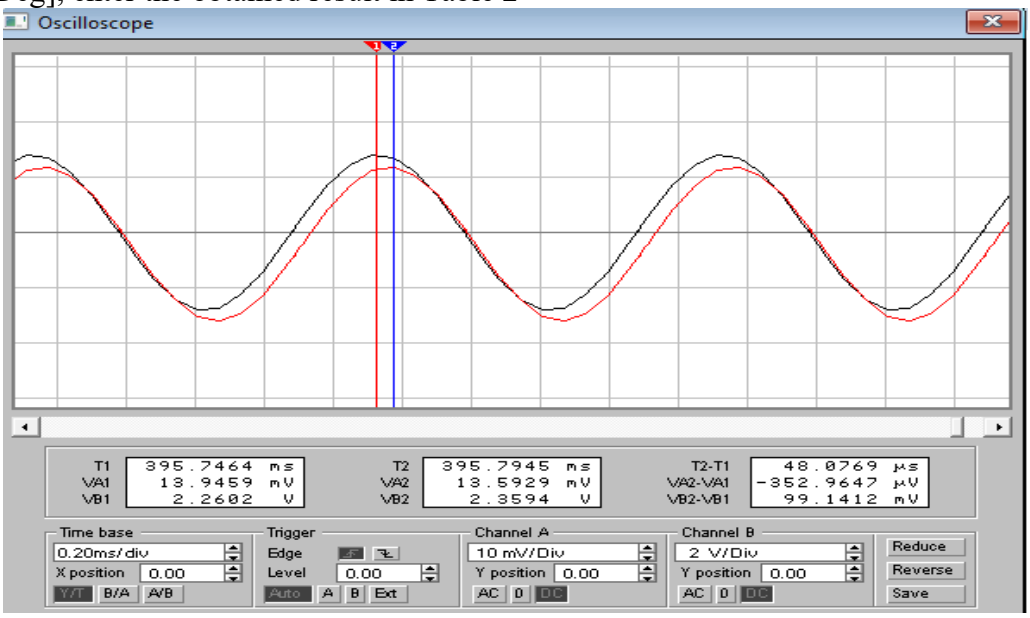
– run the EWB program simulator and obtain oscillograms of the input and output signals, while the 2nd channel should be configured to measure constant signals (press the DC button), this will make sure that the output signal contains constant component voltage. Received oscillograms bring in V report for laboratory work;

– eliminate constant component, For this translate key **S1** V left position , connecting a source that compensates for the offset voltage to the inverse input of the op amp;

– obtain oscillograms of the input and output signals in the absence of a constant - component of the output voltage, which should be included in the laboratory report;

– measure With help voltmeters MVS1, MOS And MVS2 respectively input voltage signals $\mathbf{U}_{\mathbf{in}}^{+}$ And $\mathbf{U}_{\mathbf{in}}^{-}$, weekend signals $\mathbf{U}_{\mathbf{out}}$, A Also calculate difference input voltage $\mathbf{\Delta U}_{\mathbf{inD}}$ and the actual voltage gain factor $\mathbf{K}_{\mathbf{U}}$, enter the obtained results into Table 2;

– determine the phase difference between the output and input using the oscilloscope cursors harmonic voltage, at absence in-phase signals, For example, as in Fig. 13, measure the time shift between signals $\Delta \mathbf{t} = T2 - T1$, and then determine the phase shift using the formula: $\Delta\varphi = \Delta \mathbf{t} \cdot \mathbf{f} \cdot \mathbf{360}$ [Deg], enter the obtained result in Table 2



Rice. 13 - Difference measurements phases between weekends And input signals

– Obtain the amplifier's frequency response using a Bode plotter. To do this, configure it so that the frequency changes in the range from 1 Hz to 100 MHz, and the voltage gain is measured from 0 to 120 dB. Record the resulting frequency response in the lab report;

– measure the differential voltage gain $\mathbf{K}_{\mathbf{diff}}$, For this open chain reverse connections (disconnect red wire V chains feedback), run the EWB program simulator and measure the maximum gain in dB in the graph plotter, and then enter the result, recalculated in times, into Table 2 using the formula:

$$\mathbf{K}_{\mathbf{diff}} = \mathbf{10}^{\mathbf{Kdif\,[dB]/20}};$$

Table 2 – Results of measurements and calculations in the study of a non-inverting amplifier based on an op-amp.

$\mathbf{U}_{\mathbf{in}}^{+}$, mV	$\mathbf{U}_{\mathbf{in}}^{-}$, mV	$\Delta \mathbf{U}_{\mathbf{input}} = \mathbf{U}_{\mathbf{input}}^{+} - \mathbf{U}_{\mathbf{input}}^{-}$, µV	**calculated. To** $\mathbf{K}_{\mathbf{U}}$	**measured** $\mathbf{K}_{\mathbf{U}}$	**calculated. To the differential**
measured $\mathbf{U}_{\mathbf{out}}$, V	$\mathbf{U}_{\mathbf{out}} = \mathbf{U}_{\mathbf{in}}^{+} \cdot \mathbf{K}_{\mathbf{U}}$, V	$\mathbf{U}_{\mathbf{out}} = \Delta \mathbf{U}_{\mathbf{inhD}} \cdot \mathbf{K}_{\mathbf{diff}}$, IN	Δτ, mks	Δφ, Grad	**Ft**

– define By frequency response amplifier without OOS ultimate frequency gains $\mathbf{F_t}$, on in which the natural gain is equal to one (0 dB), the obtained result should be entered into the laboratory work report in Table 2.

2.2.2) Conduct a study of the frequency and gain properties of a non-inverting op-amp amplifier depending on the feedback resistance. To do this, perform the following steps:

– restore the circuit to its original state by connecting the feedback, run the EWB program simulator;

– carry out measurements of the input signal voltages $\mathbf{U_{in}^+}$ and $\mathbf{U_{in}^-}$, and calculate the - difference input stresses $\mathbf{\Delta U_{inlet}}$, received result bring in V report By laboratory work in table 3;

– open the graph plotter (Bode plotter), use the frequency response of the amplifier to determine the differential gain $\mathbf{K_{diff}}$ in the presence of negative feedback, the gain bandwidth Δ **f** (transmission), the obtained results should be entered into the laboratory work report in Table 3;

– calculate the gain area of the amplifier **P** as the product of the differential gain $\mathbf{K_{diff}}$ on the gain bandwidth Δ **f** (transmission), enter the obtained result into the laboratory work report in Table 3;

– changing resistance **Ros** , sequentially installing his 1 Mohm, 50 kOhm And 10 kOhm, repeat measurements stresses input signals $\mathbf{U_{in}^+}$ And $\mathbf{U_{in}^-}$ And calculation differences input stresses $\mathbf{\Delta U_{inlet}}$, A Also measurements differential coefficient gains **To the differential** in the presence of negative feedback, the gain bandwidth Δ **f** (transmission), and also the calculation of the gain area P. **The** obtained results are recorded in the laboratory report in Table 3.

Table 3 – Results of measurements and calculations in the study of a non-inverting amplifier based on an op-amp.

Ros	$\mathbf{U_{in}^+}$, mV	$\mathbf{U_{in}^-}$, mV	$\Delta \mathbf{U_{вхД}}$, μV	**To the differential**	Δ **f,** Hz	**P**
1000 kOhm						
200 kOhm						
50 kOhm						
10 kOhm						

– analyze how the magnitude of the feedback resistance affects the phase difference between input And weekend signals, For this, changing resistance **Ros** , sequentially installing his 1 Mohm, 200 kOhm, 50 kOhm, get oscillograms input And output signals, on which the time shift between signals Δ **t** = T2 – T1 is measured, and then the phase shift is determined using the formula: $\Delta\varphi = \Delta \mathbf{t} \cdot \mathbf{f} \cdot \mathbf{360}$ [Deg], the obtained results together with the oscillograms are recorded in the laboratory work report;

– to analyze how the value of the feedback resistance affects the amplification of pulse signals, to do this, switch the **S2 switch** to the right position, connecting it to the input OU source pulsed signals, changing resistance **Ros** , sequentially lips his 1 Mohm, 200 kOhm And 50 kOhm, get oscillograms weekend signals And include them in the lab report;

– analyze all the obtained oscillograms, frequency response and the results listed in Table 3 , draw conclusions about what (what parameters) and how the change in feedback resistance affects, and what this leads to.

2.2.3) Conduct study amplitude characteristics non-inverting amplifier on OU at condition, What sensitivity OU equal 10 μV . For this execute next steps:

– bring diagram V original state, How shown on rice. 12;

– install V source harmonic signal **VS** minimum voltage input signal equal to sensitivity;

– launch simulator programs EWB, With help oscilloscope get oscillograms of the input and output signals, using a voltmeter measure the voltage of the output signal $\mathbf{U}_{out}$, enter the obtained result in Table 4;

– change voltage input signal $\mathbf{U}_{in}^{+}$, sequentially installing his 100 μV, 1 mV, 10 mV, 100 mV and 1 V, for each input voltage, analyze the oscillogram weekend signal With purpose definitions availability or absence nonlinear distortions of feelings, A Also With help voltmeter conduct measurement quantities voltage output signal $\mathbf{U}_{out}$, enter the obtained results into Table 4;

– calculate the value of the maximum input signal at which the signal is not yet subject to nonlinear distortion, using the formula

$$\mathbf{U}_{in.max} = \mathbf{E}_{and} / (\sqrt{2} \cdot \mathbf{K}_{U}),$$

where $\mathbf{E}_{and}$ – power source voltage, located in the parameters window of the specified op-amp model with the Edit button pressed;

– the calculated voltage $\mathbf{U}_{in.max}$ in the harmonic signal source **VS** input signal, run the EWB program simulator, check the output signal oscillogram for the absence of nonlinear distortions, enter the voltage $\mathbf{U}_{in.max}$ in cell X of table 4, using a voltmeter, measure the output signal voltage $\mathbf{U}_{out}$, and enter the obtained result in table 4;

Table 4 – Results of measurements and calculations in the study of a non-inverting amplifier based on an op-amp.

$\mathbf{U}_{in}^{+}$	10 μV	100 μV	1 mV	10 mV	**X**	100 mV	1 B
$\mathbf{U}_{out}$							
The presence of non- linear and - distortions (+/-)							
D , V times							
D , dB							

– calculate And bring in V table 4 meaning dynamic range OU, using the formula

$$D = \mathbf{U}_{in.max} / \mathbf{U}_{in.min};$$

– convert the value of the dynamic range of the OU to relative units of measurement - (decibels) and enter the obtained result into Table 4;

– analyze brought in V table 4 results, do conclusions O volume, Which What is the - amplitude characteristic of a given op-amp, what is the value of the dynamic range?

2.3) ***Draw general conclusions*** based on the results of the conducted study of a non- - inverting amplifier based on an op-amp.

<u>Task 3.</u> Conduct a study of the operating principles, parameters and characteristics of an inverting amplifier.

statement :

Initial data For research are given models OU (cm. table 1) and their parameters for direct current obtained in task 1.

The task requires that an inverting amplifier be modeled on the basis of a given operational amplifier, its operating principles be analyzed, and the following parameters and characteristics be determined and studied:

– coefficient gains voltage at availability OOS, differential voltage gain factor (without feedback);

– entrance And output resistances;

– difference phases between output and input sinusoidal voltage of the op amp;

– voltage displacements And degree influences coefficient gains schemes on constant - component of the output voltage;

– amplitude characteristics (OH), dynamic range And maximum input voltage at which the signal is not subject to nonlinear distortion;

– amplitude-frequency characteristics (frequency response), width stripes gains, gain area and gain cutoff frequency.

For this take advantage of typical schemes, providing conducting measurements of the required parameters.

For conducting research scheme should have measuring instruments :

– ammeters And voltmeters For current measurements and stress;

– sources signals For tasks input impacts;

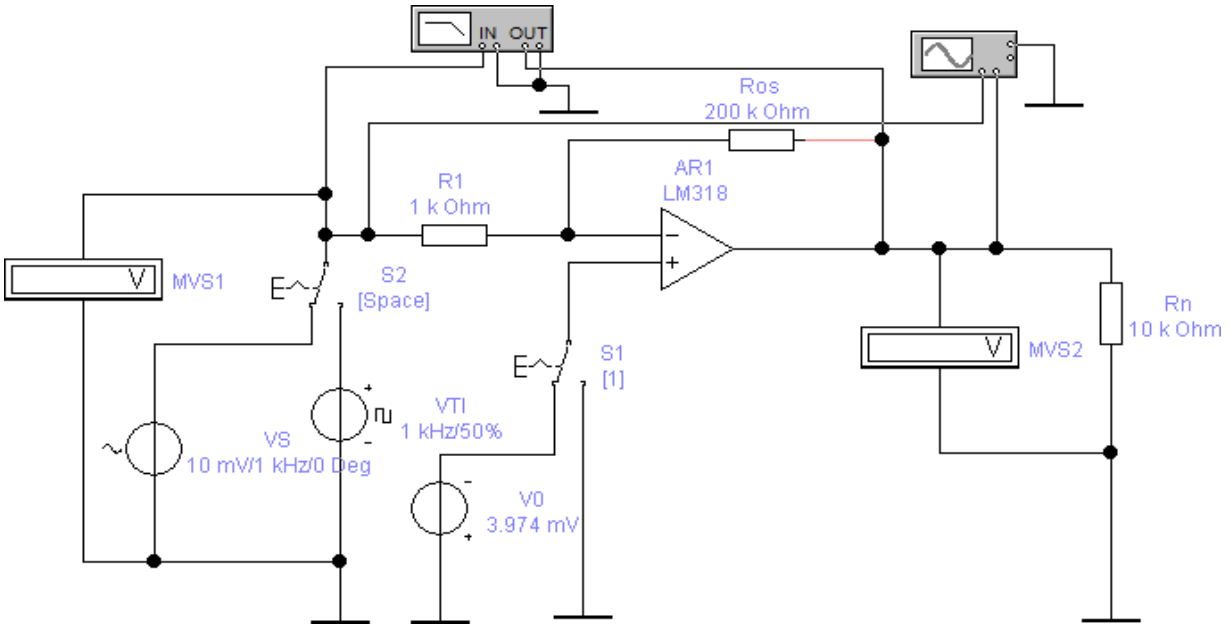
– oscilloscope For analysis forms weekend signals;

– meter frequency response (Bode plotter).

Order execution tasks 3

3.1) Simulate the inverting amplifier circuit using an op amp. To do this, perform the following procedures:

3.1.1) Collect V program EWB principled electrical circuit of an inverting amplifier based on an op amp with an unbalanced input. Set the op amp model as indicated in the initial data (Table 1), and the resistance values as shown in Fig. 14, i.e. **Ros** = 200 kOhm, **R1** = 1 kOhm, **Rn** = 10 kOhm.



Rice. 14 - Scheme For research parameters And characteristics inverting usi- litelya at the OU

3.1.2) Install next parameters input signals:

– V source harmonic signal **Vs** - current voltage 10 mV, And frequency – 1 kHz;

– **VTI** pulse signal source – amplitude of 5 mV, pulse repetition frequency of 1 kHz, and pulse duration of 50%;

– in a constant voltage source **V0** is the bias voltage for a given op-amp model, determined in paragraph 1.2) of the previous task.

3.1.3) Schematic switches bring V original position next way:

– key S1 – to the right position (bias voltage source is disconnected);

– key S2 - V left position (connected source harmonic signal); Switch the voltmeters to the variable measurement mode.

3.1.4) Run the EWB simulator and check the circuit's functionality. If the amplifier is operating correctly, the **MVS1 voltmeter** should show an input signal voltage of approximately 10 mV, and the **MVS2 voltmeter** should show an output signal voltage of approximately 2 V. Otherwise, the circuit is incorrectly assembled; find and fix any errors.

3.2) To investigate the operating principles, parameters, and characteristics of an op-amp inverting amplifier, perform the following procedures:

3.2.1) Conduct measurements, calculation And analysis parameters inverting amplifier to the op amp for alternating current. To do this, perform the following steps:

– calculate theoretical coefficient gains voltage $\mathbf{K}_{U}$ For schemes inverting amplifier on OU, taking advantage of formula (3), received result enter in table 5;

– run the EWB program simulator and obtain oscillograms of the input and output signals, while the 2nd channel should be configured to measure constant signals (press the DC button), this will make sure that the output signal contains constant component voltage. Received oscillograms bring in V report for laboratory work;

– eliminate constant component, For this translate key **S1** V left position by connecting a source compensating for the offset voltage to the direct input of the op-amp; open the feedback circuit (remove the red wire), set the **MVS2 voltmeter** to the DC voltage measurement mode, run the EWB program simulator and change slightly voltage source **V0** compensate permanent voltage on output of the op amp, achieving Togo, to voltage on voltmeter reached minimum By module values (units – tens of millivolts);

– return the circuit to its original state by connecting the feedback, switching the **MVS2** voltmeter to the AC voltage measurement mode, running the EWB program simulator, obtaining oscillograms of the input and output signals in the absence of a DC component of the output voltage, which should be included in the laboratory report;

– measure With help voltmeters MVS1 And MVS2 respectively voltage input signal $\mathbf{U}_{in^-}$, output signal $\mathbf{U}_{out}$, and also calculate the actual voltage gain factor $\mathbf{K}_{U}$, enter the obtained results in Table 5;

– determine the phase difference between the output and input using the oscilloscope cursors harmonic voltage, For this measure temporal shift between signals
$\Delta \mathbf{t}$ = T2 - T1, A then define phase shift By formula: $\Delta\varphi = \Delta \mathbf{t} \cdot \mathbf{f} \cdot \mathbf{360}$ [Grad], enter the obtained result into table 5

– Obtain the amplifier's frequency response using a Bode plotter. To do this, configure it so that the frequency changes in the range from 1 Hz to 100 MHz, and the voltage gain is measured from 0 to 120 dB. Record the resulting frequency response in the lab report;

– measure the differential voltage gain $\mathbf{K}_{diff}$, For this open chain reverse connections (disconnect red wire V chains feedback), run the EWB program simulator and measure the maximum gain in dB in the graph plotter, and then enter the result, recalculated in times, into Table 5 using the formula:

$$\mathbf{K}_{diff} = \mathbf{10}^{\mathbf{Kdif\,[dB]/20}}.$$

Table 5 – Results of measurements and calculations in the study of a non-inverting amplifier based on an op-amp.

measured U_{in^-}, mV	**calculated To U**	**measured To U**	**calculated To the differential**
measured U_{out}, IN	$\mathbf{U}_{out} = \mathbf{U}_{in^+} \cdot \mathbf{K}_{U}$, IN	Δ **t,** ISS	$\Delta\varphi$ **,** Grad

3.2.2) Conduct a study of the frequency and gain properties of an inverting op-amp amplifier depending on the feedback resistance. To do this, perform the following steps:

– restore the circuit to its original state by connecting the feedback, run the EWB program simulator;

– measure the input signal voltage $\mathbf{U}_{\mathbf{in}}^{-}$, enter the result into the laboratory work report in Table 6;

– open plotter (Bode plotter), By frequency response amplifier define voltage gain factor $\mathbf{K}_{\mathbf{U}}$ in the presence of negative feedback, the gain bandwidth Δ **f** (transmission), the obtained results should be recorded in the laboratory work report in Table 6;

– calculate the area gains amplifier **P** , as a product of the coefficient voltage gain $\mathbf{K}_{\mathbf{U}}$ on the bandwidth of the gain Δ **f** (transmission), the obtained result should be included in the laboratory work report in Table 6;

– changing resistance **Ros** , sequentially installing his 1 Mohm, 50 kOhm And 10 kOhm, repeat the measurements of the input signal voltage $\mathbf{U}_{\mathbf{in}}^{-}$, as well as the measurements of the - coefficient gains voltage **To** $_{\mathbf{U}}$ at availability OOS, width stripes gains Δ **f** (transmission), as well as the calculation of the gain area **P.** The obtained results should be included in the laboratory work report in Table 6;

Table 6 – Results of measurements and calculations in the study of a non-inverting amplifier based on an op-amp.

Ros	$\mathbf{U}_{\mathbf{in}}^{-}$, mV	**To** $_{\mathbf{U}}$	Δ **f,** Hz	**P**
1000 kOhm				
200 kOhm				
50 kOhm				
10 kOhm				

– analyze how the magnitude of the feedback resistance affects the phase difference between input And weekend signals, For this, changing resistance **Ros** , sequentially installing his 1 Mohm, 200 kOhm, 50 kOhm, get oscillograms input And output signals, on which the time shift between signals $\Delta \mathbf{t}$ = T2 – T1 is measured, and then the phase shift is determined using the formula: $\Delta\varphi = \Delta \mathbf{t} \cdot \mathbf{f} \cdot \mathbf{360}$ [Deg], the obtained results together with the oscillograms are recorded in the laboratory work report;

– to analyze how the value of the feedback resistance affects the amplification of pulse signals, to do this, switch the **S2 switch** to the right position, connecting it to the input OU source pulsed signals, changing resistance **Ros** , sequentially lips his 1 Mohm, 200 kOhm And 50 kOhm, get oscillograms weekend signals And include them in the lab report;

– analyze all the obtained oscillograms, frequency response and the results entered in Table 6 , draw conclusions about what (what parameters) and how the change in feedback resistance affects, and what this leads to.

3.2.3) Conduct a study of the amplitude characteristic of the inverting amplifier on OU at condition, What sensitivity OU equal 10 μV . For this execute next steps:

– bring diagram V original state, How shown on rice. 14;

– install V source harmonic signal **VS** minimum voltage input signal equal to sensitivity;

– launch simulator programs EWB, With help oscilloscope get oscillograms of the input and output signals, using a voltmeter measure the voltage of the output signal $\mathbf{U}_{\mathbf{out}}$, enter the obtained result in Table 7;

– change voltage input signal U_{in}^{-}, sequentially installing his 100 μV, 1 mV, 10 mV, 100 mV and 1 V, for each input voltage, analyze the oscillogram weekend signal With purpose definitions availability or absence nonlinear distortions of feelings, A Also With help voltmeter conduct measurement quantities voltage output signal U_{out}, enter the obtained results into Table 7;

– calculate the value of the maximum input signal at which the signal is not yet subject to nonlinear distortion, using the formula

$$U_{in.max} = E_{and} / (\sqrt{2} \cdot K_U),$$

where E_{and} – power source voltage, located in the parameters window of the specified op-amp model with the Edit button pressed;

– the calculated voltage $U_{in.max}$ in the harmonic signal source **VS** input signal, run the EWB program simulator, check the output signal oscillogram for the absence of nonlinear distortions, enter the voltage $U_{in.max}$ in cell X of table 7, using a voltmeter, measure the output signal voltage U_{out}, and enter the obtained result in table 7;

Table 7 – Results of measurements and calculations in the study of a non-inverting amplifier based on an op-amp.

U_{in}^{+}	10 μV	100 μV	1 mV	10 mV	**X**	100 mV	1 B
U_{out}							
The presence of non- linear and - distortions (+/-)							
D , V times							
D , dB							

– calculate And bring in V table 7 meaning dynamic range OU, using the formula

$$D = U_{in.max} / U_{in.min};$$

– convert the value of the dynamic range of the OU to relative units of measurement - (decibels) and enter the obtained result into Table 7;

– analyze brought in V table 7 results, do conclusions O volume, Which What is the - amplitude characteristic of a given op-amp, what is the value of the dynamic range?

3.3) ***Do generalizing conclusions*** By results conducted research inverting amplifier on OU, compare principles work, parameters And characteristics inverting and non-inverting amplifiers.

<u>Exercise 4.</u> Conduct study of the features of work and parameters differential amplifier.

statement :

<u>This task is related to advanced level tasks and is completed by students independently.</u>

Initial data For research are given models OU (cm. table 1) and their parameters for direct current obtained in task 1.

The task requires that, based on a given operational amplifier, a differential amplifier with a symmetrical input and an asymmetrical output be modeled and its distinctive features analyzed . its features work, determine And conduct study following its parameters:

– differential coefficient gains voltage,
– coefficient gains common mode voltage,
– coefficient relative weakening in-phase signal;
– difference phases between weekends And input sinusoidal voltages OU.

For this take advantage of typical schemes, providing conducting measurements of the required parameters.

For conducting research scheme should have measuring instruments :

– voltmeters For measurements stress;

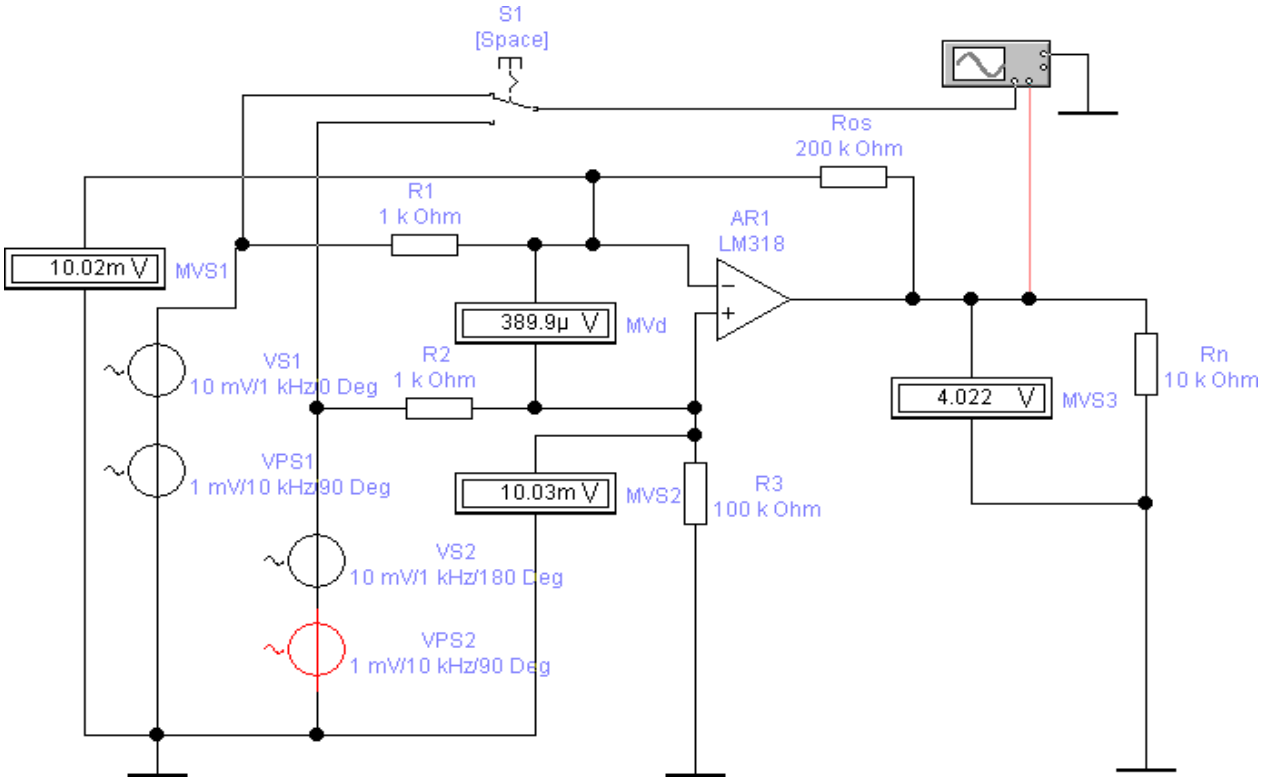
– sources signals For tasks input impacts;

– oscilloscope for form analysis input and output signals.

Order execution tasks 4

4.1) Simulate a differential amplifier circuit using an op amp. To do this, perform the following procedures:

4.1.1) Collect V program EWB principled electrical diagram differential amplifier based on an op-amp with a symmetrical input. Set the op-amp model as specified in the initial data (Table 1), and the resistance values as shown in Fig. 15, i.e. **Ros** = 200 kOhm, **R1** = 1 kOhm, **R2** = 1 kOhm, **R3** = 100 kOhm, **Rn** = 10 kOhm.



Rice. 15 - Scheme For research parameters differential amplifier

4.1.2) Install next parameters input signals:

– V sources harmonic signals **VS1** And **VS2** - identical current voltage By 10 mV, And frequencies - 1 kHz, A phases - opposite V first - 0 hail, A in second - 180 degrees;

– V sources in-phase harmonic interference **VPS1** And **VPS2** - identical effective voltages of 1 mV, matching frequencies of 10 kHz, and phases of 90 degrees;

– switch S1 in upper position.

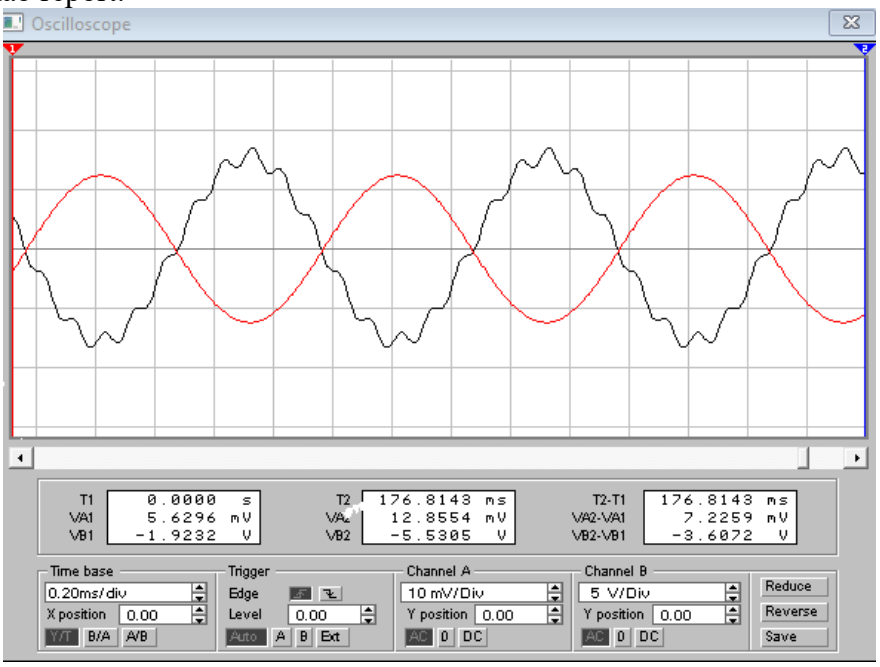
4.1.3) All voltmeters translate V mode measurements variables quantities.

4.1.4) , the MVS1 and **MVS2** voltmeters should show the voltage of the antiphase input signals, about 10 mV, and the **MVd voltmeter** should show the voltage of the differential input signal, approximate equal 0.4 mV (difference input signals). The **MVS2** voltmeter should show an output voltage of about 4 V.

IN otherwise case scheme collected With mistakes, find their And eliminate.

4.2) Research distinctive peculiarities work And parameters differential amplifier with an op-amp. To do this, perform the following procedures:

4.2.1) Run the EWB program simulator and obtain oscillograms of the input and output signals, while both channels are configured to measure variable signals (press button AC). Make sure V volume, What V on the weekend signal V difference from input There is no common-mode interference in the signal. An example is shown in Fig. 16. The resulting oscillograms should be included in the lab report.



Rice. 16 -Input And weekend signals differential amplifier

4.2.2) Conduct measurements, calculation And analysis parameters differential op-amp amplifier for alternating current. To do this, follow these steps:

– turn off in-phase harmonic interference, For this V sources **VPS1** And **VPS2** install current voltage 0 mV;

– $\mathbf{U}_{in}$ using the voltmeters MVS1, MVS2, MVS3 and MVd, respectively and $\mathbf{U}_{in}^{+}$, output signals $\mathbf{U}_{out}$, input voltage difference $\mathbf{\Delta U}_{inD}$, enter the obtained results in Table 8;

– calculate differential input signal $\mathbf{U}_{input} = \mathbf{U}_{input}^{+} + \mathbf{U}_{input}^{-}$, received enter the result in the table. 8;

– calculate the voltage gain $\mathbf{K}_{U} = \mathbf{U}_{out} / \mathbf{U}_{in}$ and differential gain $\mathbf{K}_{diff} = \mathbf{U}_{out} / \Delta \mathbf{U}_{in}$, enter the obtained results into Table 8;

– determine the phase difference between the output and input harmonic voltage using the oscilloscope cursors, measure the time shift between the signals $\Delta \mathbf{t}$ = T2 – T1, A then define phase shift By formula: $\Delta\varphi = \Delta \mathbf{t} \cdot \mathbf{f} \cdot \mathbf{360}$ [Grad], received enter the result in the table. 8

Table 8 – Results of measurements and calculations in the study of a differential amplifier based on an op amp.

$\mathbf{U}_{in}^{+}$, mV	$\mathbf{U}_{in}^{-}$, mV	$\Delta \mathbf{U}_{input} = \mathbf{U}_{input}^{+} - \mathbf{U}_{input}^{-}$, μV	$\mathbf{U}_{вхД} = \mathbf{U}_{вх}^{+} + \mathbf{U}_{вх}^{-}$, μV	$\mathbf{U}_{out}$, In
To $_{U} = \mathbf{U}_{out} / \mathbf{U}_{input}$	**To** $_{diff.} = \mathbf{U}_{out} / \Delta \mathbf{U}_{input}$		Δ **t,** ISS	$\Delta\varphi$ **,** Grad

– turn on in-phase harmonic interference, For this in sources **VPS1** And **VPS2** install current voltage, equal original 1 mV;

– set the effective voltage in sources **VS1** and **VS2** to 0 mV;

– launch simulator programs EWB, get oscillograms input And output common-mode signals, with both channels configured to measure variable signals (press button AC). Received oscillograms bring in V report By laboratory work;

– measure With help cursors oscilloscope amplitudes input And weekend in- phase signals $U_{in.sf}$ and $U_{out.sf}$, enter the obtained results into Table 9;

– calculate the common mode voltage gain factor $K_{SF} = U_{out.sf} / U_{in.sf}$, enter the obtained result into Table 9;

– calculate the coefficient of relative attenuation of common mode signals $K_{OOS} = K_{diff} / K_{SF}$, convert the value of the coefficient into a relative unit of measurement - decibels , enter the obtained results in Table 9.

Table 9 – Results of measurements and calculations in the study of a differential amplifier based on an op amp.

$U_{in.sf}$, **mV**	$U_{out.sf}$, **m** B	**To** $_{the\ SF} = U_{out.sf} / U_{in.sf}$	**To the** $_{Joint\ Forces\ Operation} = K_{diff} / K_{SF}$	**To** $_{the\ OOS}$, **dB**

– analyze All received oscillograms, brought in V Table 8 And 9 results , draw conclusions.

4.2.3) Conduct a study of the operating features of a differential amplifier using an op-amp. To do this, perform the following steps:

– bring diagram V original (initial) state, launch simulator EWB programs, make sure they work correctly;

– switch the circuit to the inverting amplifier mode , for this, set the effective voltage in sources **VS2** , **VPS1** and **VPS2 to 0 mV;**

– run the EWB program simulator, measure the input signal voltage $U_{in.diff^-}$ and the output signal $U_{out.inv}$, enter the obtained results into Table 10;

– calculate the differential gain in the inverting amplifier mode $K_{diff.inv} = U_{out.inv} / U_{in.diff^-}$, enter the obtained result into Table 10;

– get oscillograms input And weekend in-phase signals, at this Set both channels to measure alternating signals (press the AC button). Record the resulting oscillograms in the lab report. Use the oscilloscope cursors to measure the amplitudes of the input and output voltages ($U1_{in.max^-}$ and $U1_{out.max}$), enter the obtained results into Table 10;

– calculate the voltage gain in the inverting amplifier mode $K_{U.inv} = U1_{out.max} / U1_{вх.max^-}$, enter the obtained result into Table 10;

Table 10 - Results measurements And calculations at research differential amplifier on the op-amp.

$U_{in.diff^-}$, μV	$U_{out.inv}$., V	**To** $_{differential\ inv} = U_{out.\ inv} / U_{in.\ differential^-}$	$U1_{in.max^-}$, mV	$U1_{out.max}$, IN	$K_{U.inv} = U1_{out.max} / U1_{in.max^-}$
$U_{in.diff^+}$, μV	$U_{out.neinv}$, IN	$K_{diff.noninv} = U_{out.noninv} / U_{in.diff^+}$	$U2_{input\ max^+}$, mV	$U2_{output\ max}$., In	$K_{U.inv} = U2_{vyh.max} / U2_{vh.max^-}$

– translate diagram V mode non-inverting amplifier , For this V sources **VS1** , **VPS1** and **VPS2** install current voltage, equal 0 mV, and in source **VS2** – voltage 10 mV, and phase – 0 degrees;

– run the EWB program simulator, measure the input signal voltage $\mathbf{U}_{\mathbf{in.dif}^+}$ and the output signal $\mathbf{U}_{\mathbf{out.non\text{-}inv}}$, enter the obtained results into Table 10;

– calculate differential coefficient gains V mode non-inverting amplifier $\mathbf{K}_{\mathbf{diff.neinv}} = \mathbf{U}_{\mathbf{out.non\text{-}inv}} / \mathbf{U}_{\mathbf{in.diff}^+}$, enter the obtained result into Table 10;

– get oscillograms input And weekend in-phase signals, at this Set both channels to measure alternating signals (press the AC button). Record the resulting oscillograms in the lab report. Use the oscilloscope cursors to measure the amplitudes of the input and output voltages ($\mathbf{U2}_{\mathbf{in.max}^+}$ and $\mathbf{U2}_{\mathbf{out.max}}$), enter the obtained results into Table 10;

– calculate coefficient gains voltage V mode non-inverting amplifier $\mathbf{K}_{\mathbf{U.neinv}} = \mathbf{U2}_{\mathbf{out.max}} / \mathbf{U2}_{\mathbf{in.max}^+}$, enter the obtained result into Table 10;

– analyze the results listed in Table 10 and draw conclusions by comparing the two operating modes of the amplifier.

4.3) ***Draw general conclusions*** based on the results of the conducted study of a differential amplifier based on an op-amp, compare the principles of its operation and parameters with inverting and non-inverting amplifiers.

<u>Task 5. (for independent work)</u> Present the research results in the form of a laboratory report and defend it.

5.1) IN report By laboratory work display:

– topic and target work, tasks For research And brief order their execution;

– simulated V editor schematic modeling Schematic diagrams of the amplifiers under study;

– oscillograms input and output signals;

– graphs frequency response With results measurements frequency parameters;

– results studies in the form of tables with measured and calculated parameters of the amplifiers under study;

– conclusions By results execution tasks And V in general By work done .

5.2) Defend a report on the completed laboratory work by completing an individual assignment specified by the teacher, within the framework of the research conducted.

Control questions For preparation To protection:

1. Measurement input currents operating amplifier (op-amp).
2. Measuring bias voltage OU.
3. Measurement speed increase in the output voltage of the op amp.
4. Measurement speed growth output voltage of the op amp.

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 7

Subject: STUDY FUNCTIONAL SCHEMES ON BASE OPERATIONS-THEY AMPLIFIERS

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– realize circuit design (computer) modeling various functional circuits on operational amplifiers using universal software packages;

– conduct research into the operating principles, main characteristics and parameters of various functional circuits using operational amplifiers;

– collection and analysis of information to generate initial data for designing functional circuits using operational amplifiers.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling "ElectronicsWorkbench" (EWB), version no lower than 5.12 or NIMultisim Education version;

– MathcadProfessional application for mathematical and engineering calculations, version not lower than 15.0;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

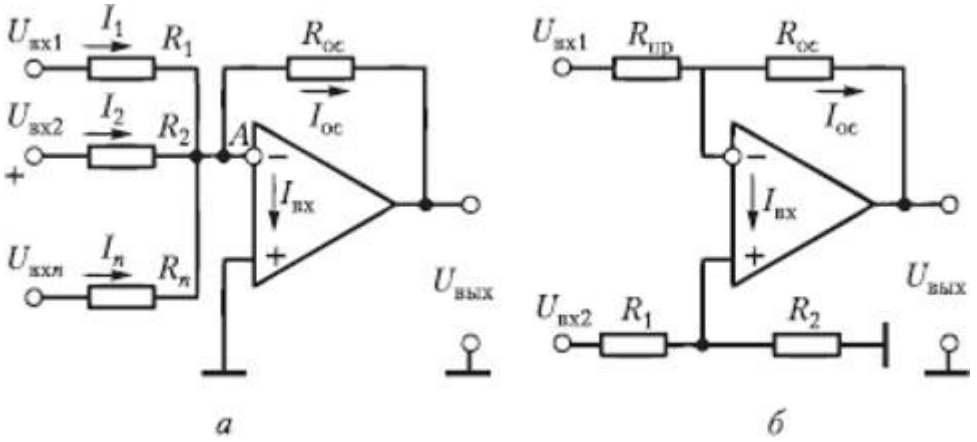
Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study principles work And parameters adder, subtractor on operating amplifier.	50 min
2. Study principles work And parameters differentiator on operational amplifier.	25 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**65 min**
2. Study principles work And parameters differentiator on operational amplifier.	20 min
3. Study principles work And parameters integrator on operations-onnom amplifier.	45 min
The final part	**15 min**
Defense of practical work reports	10 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

1. Adder stresses

To perform the operation of algebraic addition of several electrical signals enough supplement inverting or non-inverting inclusion OU with additional inputs according to the number of terms (Fig. 1, a).



Rice. 1 - Schemes on the basis of the educational institution summation (a), subtractions (b)

Entrance voltage through resistors R_1, …, R_N are served on inverting the amplifier input (point A), which in this circuit is the summing point. Since this point is virtual zero (non-inverting entrance grounded) $\Delta U_{in} \approx 0$, A (The input current of the operational amplifier is negligible), then the currents created by the input voltages will sum up and flow through the resistor R_{OC}.

Values each current is determined level corresponding input voltage and resistance of resistors in the input circuits $I_1 = U_{in1}/R_1$, $I_2 = U_{in2}/R_2$, etc. In the general case, for n input signals we can write:

$$U_{ВЫХ} = -(U_{ВХ1} \cdot \frac{R_{OC}}{R_1} + U_{ВХ2} \cdot \frac{R_{OC}}{R_2} + \ldots + U_{ВХn} \cdot \frac{R_{OC}}{R_n}) \quad (1)$$

The ratio of the resistance in the feedback circuit to the resistances of the corresponding entrances Can count weight coefficients. IN private case at $R_{os} = R_1 = R_2 = \ldots = R_n$ it turns out adder stresses

$$U_{вых} = -(U_{вх1} + U_{вх2} + \cdots + U_{вхn}) \quad (2)$$

If the resistors are different, then each of the input voltages will be summed with the proportionality coefficient $K_i = R_{oc}/R_i$:

$$U_{вых} = -\sum_{i=1}^{n} K_i U_i \quad (3)$$

Fig. 1, b) shows a circuit that provides subtraction of two voltages: If All resistance do

$$U_{вых} = U_2 - U_1. \quad (4)$$

the same, That at absence second voltage
nia, those. $U_2 = 0$, remains scheme with inverting inclusion amplifier for which

$$U_{вых} = -\frac{R_{oc}}{R_{пр}} U_1 = -\frac{R}{R} U_1 = -U_1. \quad (5)$$

In the absence of the first voltage, i.e. $U_1 = 0$, the amplifier must create a voltage U_{out} at the output such that the potentials at the inverting and non-inverting inputs are equal. The potential at the non-inverting input is:

$$U_+ = \frac{U_2 R_2}{R_1 + R_2} = \frac{U_2 R}{R + R} = \frac{U_2}{2}. \quad (6)$$

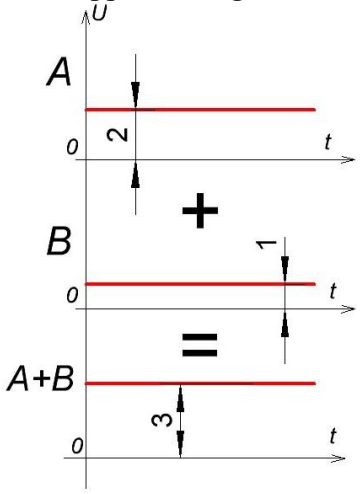
Potential on inverting input is equal to:

$$U_- = \frac{U_{вых} R_1}{R_1 + R_2} = \frac{U_{вых} R}{R + R} = \frac{U_{вых}}{2}. \quad (7)$$

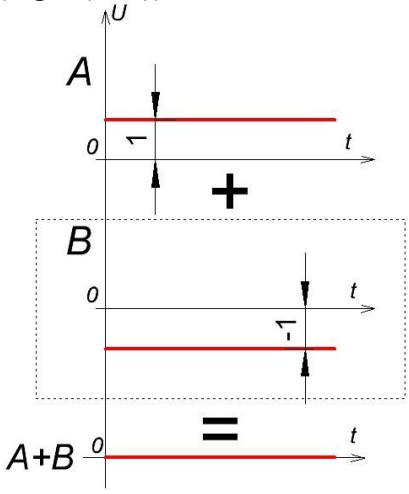
Like this in this way, $U_{out} = U_2$. If same on both entrances are present signals, That $U_{out} = U_2 - U_1$. By changing the ratio of resistances in the dividers so that $R_{pr} = R_{os}/\alpha$; $R_1 = R_2/\alpha$, a $R_{oc} = R_2$, the subtraction operation can be performed with the coefficient α:

$$U_{вых} = \alpha (U_2 - U_1). \quad (8)$$

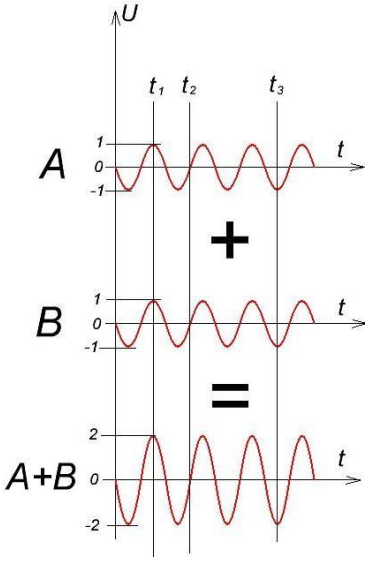
On drawing 2 We we see two signal A And B And amount these signals: A+B (Fig. 2(A,B)). If signal A = 2 IN, signal B = 1 IN, That sum these signals will make up 3 IN. All That same The same applies to signals with negative polarity (Fig. 2(B,G)).



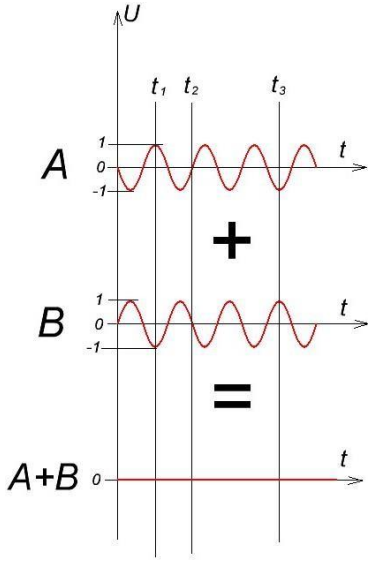
A)



B)



IN)



G)

When adding signals with equal amplitude but different polarity, we get in total 0. That There is these two signal mutually myself compensated: 1 + (-1) = 0. If Add up signals that change over time, that is, variable signals. They can be either periodic or non-periodic.

2. Differentiator

A differentiating circuit is a circuit that performs the mathematical operation of differentiation. (weekend voltage equals derivative input voltage) or the formation of sharp trigger pulses. Differentiation can be performed RC or RL chains (rice. 2, A), A Also With help operating amplifier (rice. 2, b). Differentiation of harmonic signals is performed under the condition $R \ll 1/\omega C$, and pulse signals – under $RC \ll t_и$.

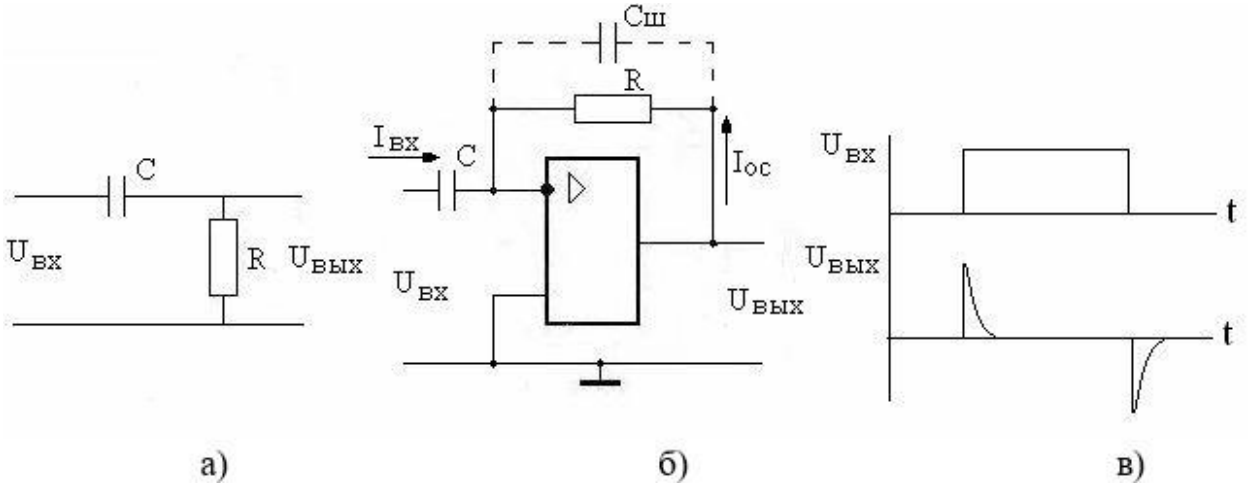


Fig. 2 – Differentiation scheme

The operation of the RC circuit (Fig. 2, a) is as follows. Before the input signal is applied, the voltages across the resistor and capacitor are zero. When the input signal is applied (Fig. 2, c), the output voltage changes abruptly to U_m and begins to decrease to zero due to the capacitor charging. The charging time is approximately equal to t = (3…5)RC. At the end of the input pulse, the capacitor, which has become a voltage source, is discharged from U_m to 0. In this case, due to the change in the direction of the current, the sign of the output voltage changes on opposite. For considered RC chains we can write the ratio

$$U = i \cdot R = RC \cdot \frac{du_c}{dt} = RC \cdot \frac{d(u_{вх} - u_{вых})}{dt} \approx RC \frac{du_{вх}}{dt}. \qquad (11)$$

IN scheme on operating amplifier, accepting his parameters ideal ($K_{df} \to \infty$ and $R_{df} \to \infty$), we can assume that the input current is equal to the feedback current $I_{in} = I_{os}$, and accordingly

$$i_{вх} = C \cdot \frac{dU_c}{dt} = C \cdot \frac{dU_{вх}}{dt} \quad и \quad i_{ос} = \frac{U_{вых}}{R}. \qquad (12)$$

Then from latest ratios we will receive

$$U_{вых} = RC \frac{dU_{вх}}{dt}. \qquad (13)$$

Thus, the output voltage in the circuit is proportional to the first derivative of the input voltage.

In order to eliminate the phenomenon of self-excitation of the differentiator, the resistor in the feedback circuit is shunted by a capacitor C_{sh}, the capacitance of which must be less than the capacitance of the working capacitor C.

3. Integrator

Integrating circuits include those whose output voltage is proportional integral input signal in time. Are applied For semi-
linearly varying voltages. Like differentiating ones, they are built on the basis of RC, RL circuits, or operational amplifiers.

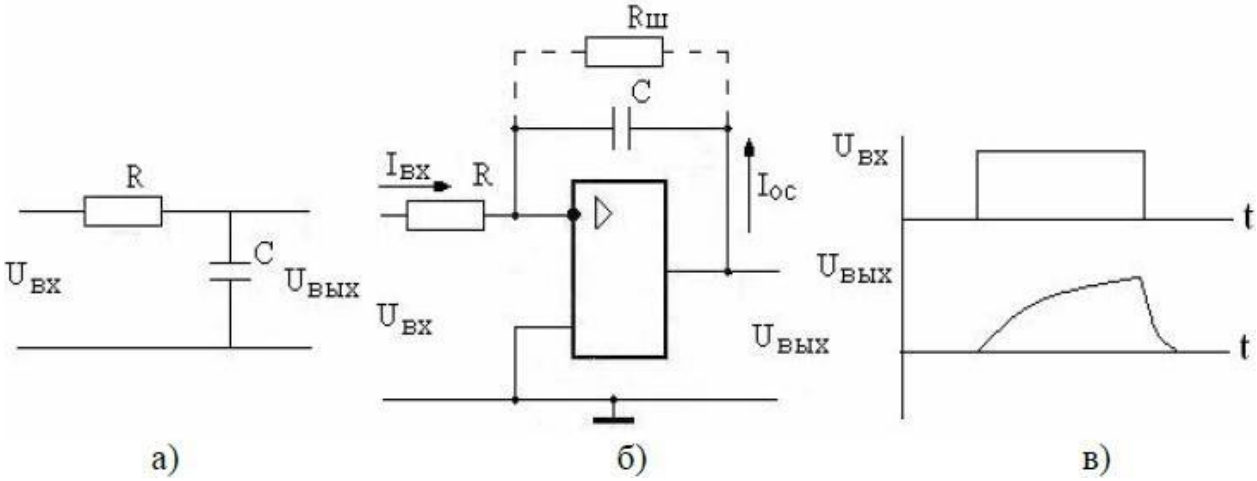


Fig. 3 – Integration scheme

IN integrating chains (rice. 3, A) at admission input impulse
the voltage on the output capacitor increases exponentially, and at the end actions - Also By exponent decreases. For execution operations integration on basis OU V chain reverse connections is being installed capacitor With wasps (rice. 3, b). In this case, for an ideal op amp,

$$i_{вх}=U_{вх}/R = i_{ос}= i_c; \qquad U_{вых} = U_c = \frac{1}{C}\int i_c(t)dt \qquad (14)$$

the following relations are valid:
Then from these ratios we get

$$U_{вых} = -\frac{1}{RC}\int_0^t U_{вх}dt \qquad (15)$$

Thus, the output voltage of the circuit is proportional to the integral of the input voltage. The values of resistance and capacitance determine the constant coefficient of the integration circuit, which can be explained from purely physical considerations. The larger R and C, the lower the current charging the capacitor, and the greater its capacitance. That's why charge capacitor, A, hence, And weekend voltage, will be grow more slowly. When applying a voltage jump to the input of the integrator, a voltage surge will be observed at the output slow height weekend voltage, incline direct graphics is determined by the integration time constant $\tau = RC$ (Fig. 3, c).

Time integration 1 accepted equal pulse duration
input signal or at periodic entrance signal - period following input signal.

Weekend voltage Not depends from coefficient gains OU, A is determined by the time constant $\tau = RC$ and the nature of the input signal. For example, when a rectangular wave is applied to the input impulse (rice. 3, V.) output signal will have view linearly changing voltage

Availability at real OU final values voltage displacements causes on during the circuit,

$$Uвых(t) = -\frac{Um}{\tau}\cdot t \qquad (16)$$

additional voltage appears

$$U_{вых} = -\frac{1}{RC}\int U_{вх} dt \quad (17)$$

In order to eliminate integration errors, the capacitor is shunted by a resistor R_{sh}, through which the capacitor is discharged.

Many physical tasks are described simple differential equations . Such tasks Can decide, implementing original differential equation With using analog integrating circuits and measuring the steady-state output voltage. Conventional differential equation — This addiction functions at And her derivatives from the variable x. For example, a second-order linear differential equation looks like this:

$$y'' + k_1 y' + k_0 y = f(x). \quad (18)$$

For permissions management produce replacement variable X on time t, those. $x = t/\tau$. Then first and the second derivatives are equal to:

$$y' = \frac{1}{x'(t)}\frac{dy}{dt} = \tau\frac{dy}{dt} \text{ и } y'' = \tau^2\frac{d^2y}{dt^2}. \quad (19)$$

By means of such transformations, the differential equation is reduced to a form that can be implemented on the basis of integration schemes:

$$\tau\frac{d^2y}{dt^2} + k_1\frac{dy}{dt} = -\frac{1}{\tau}\left[k_0 y - f(t/\tau)\right] \quad (20)$$

Integrating left And right parts equations, we get:

$$\tau\frac{dy}{dt} + k_1 y = -\frac{1}{\tau}\int\left[k_0 y - f(t/\tau)\right]dt. \quad (21)$$

The expression on the right is implemented using an integrator. Let's denote its output signal by the variable z, then:

$$z = -\frac{1}{\tau}\int\left[k_0 y - f(t/\tau)\right]dt \quad (22)$$

WITH using variable z equation is transformed To view

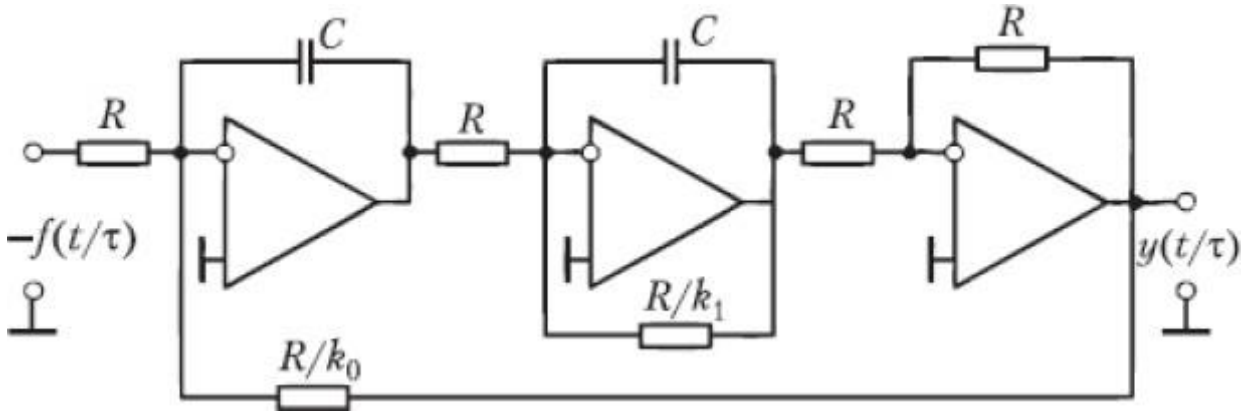
$$-\frac{dy}{dt} = -\frac{1}{\tau}\left[z - k_1 y\right] \quad (23)$$

Having integrated both parts equations, we get:

$$-y = -\frac{1}{\tau}\int\left[z - k_1 y\right]dt \quad (24)$$

The right side of this equation, just like in the previous case, is realized with the help of integrator. His day off signal corresponds functions -y. Signal z comes from the output of the previous integrator, and the signal $–k_1 y$ – through feedback from its own output.

Like this in this way, For implementation differential equations second order required two integrator And one inverting amplifier (rice. 4). Inverting The amplifier is needed to change the sign of the signal from the second integrator, which forms -y. The output signal from this amplifier with a coefficient k0 is fed to the input of the first integrator .



Rice. 4 – Analog circuit solutions of differential equations

Contents of the practical work performed students V in the course classes

Description laboratory equipment:

– PC for each student;

– program editor schematic modeling "ElectronicsWorkbench" (EWB) version no lower than 5.12 or NIMultisim Education version;

– an application for mathematical and engineering calculations, version not lower than 15.0.

Requirements security at execution works:

1) TO conducting laboratory works allowed students, past required safety briefings.

2) Turning on laboratory installations (computers) is being carried out only With once the teacher's decision.

3) When conducting laboratory work, it is not permitted to use devices or equipment that are not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) At occurrence emergency situations necessary immediately turn off equipment from the power supply network, inform the teacher about this and act according to his instructions .

6) At fire equipment his necessary immediately de-energize, report this to the teacher, take measures to eliminate the fire and act according to the teacher's instructions.

7) By ending work With laboratory equipment (computers) his must be switched off in the established order.

Tasks to be completed during practical work Basic level tasks:

1) Study of the operating principles and parameters of an adder and subtractor on an operational amplifier.

2) Study of the operating principles and parameters of a differentiator based on an operational amplifier.

Tasks increased level:

3) Study principles work And parameters integrator on operational amplifier.

Order execution works:

Exercise 1. Study principles work And parameters adder on OU.

Initial data for research

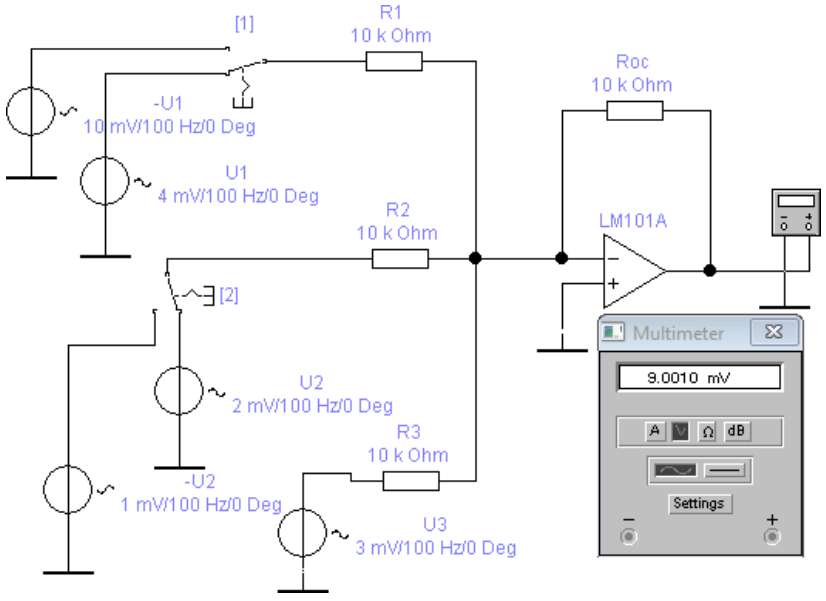
Options tasks For individual modeling schemes auto generators and the research conducted are presented in Table 1.

Table 1 - Options tasks For research.

Option number	In $_1$, mV	In $_2$, mV	At $_3$, mV
1	1	2	3
2	4	5	6
3	7	8	9
4	9	6	3
5	8	5	2
6	7	4	1
7	9	8	7
8	6	5	4
9	3	2	1
10	1	4	7
11	2	5	8
12	3	6	9
13	7	4	1
14	9	8	7
15	3	5	7
16	9	2	1
17	8	5	2
18	7	4	1
19	9	8	7
20	8	6	7
21	7	4	1
22	9	8	2
23	6	5	1
24	2	4	7
25	5	9	1
26	3	8	6

Order execution tasks 1

1.1) Collect V program EWB principled electrical diagram adder on the operational amplifier (Figure 5).



Drawing 5 - Fundamental scheme inverting adder variables voltage on the op amp

1.2) Install V collected scheme quantities parameters elements How shown in Figure 5.

1.3) Calculate the output signal using formula (1) in accordance with the set parameters of power source voltages and resistances (Fig. 5).

1.4) Calculated value of U_{out} Compare with the value obtained on the multimeter . Record the calculation results in the report. Explain why the calculated output voltage has a negative sign.

1.5) Install U_1 , U_2 , U_3 , V in accordance With option (Table 1), A resistances R_1 , R_2 , R_3 and R_{os} calculate using the formula

$$\mathbf{R_1 = R_2 = R_3 = R_{axis} = N * 10^3}$$

where N – option number.

1.6) Key 1 translate V lower position, A key 2 V right. Calculate output voltage U_{out} . Compare with the value obtained on the multimeter. Enter the obtained result in the report.

1.7) Calculate the output voltage U_{out} when changing the input conjugation U_{in1} = -10 – 10 mV. Enter the calculation results into Table 1.

1.8) WITH help multimeter measure size weekend voltage U_{out} at input voltage U_{in1} = -10 – 10 mV. To set a negative input voltage, switch 1 must be turned up. Record the calculation results in Table 2.

1.9) Calculated values compare With experimental.

1.10) Do conclusions By results research.

2.1) Calculate R_1 , R_2 , R_3 And R_{os} according to the formula

$$\mathbf{R_1 = R_2 = R_3 = R_{os} = N * 10^3}$$

where N – option number.

2.2) Calculate the output voltage at the new resistances. Enter the obtained calculation and measurement results into Table 2.

2.3) Calculate the output voltage at $R_{oc} = R_{oc}/2$ and $R_{oc} = R_{oc} * 2$. The resulting The results of calculations and measurements are entered into Table 2.

2.4) Select a resistance such that the weighting factor is equal to 10. Enter the obtained results of calculations and measurements into Table 2.

2.5) Do conclusions By results research. Table 2 – Research results

$U_{вх1}$, mV		- 10	- 8	- 6	- 4	- 2	0	2	3	4	6	8	10
U_{out} , mV	Exp.												
	Calc.												
U_{out} , mV at R_{os} = N*10 Ohm	Exp.												
	Calc.												
U_{out} , mV at $R_{os} = R_{os}/2$ Ohm	Exp.												
	Calc.												
U_{out} , mV at $R_{os} = R_{oc} * 2$ Ohm	Exp.												
	Calc.												
U_{out} , mV at $K_{1,2,3}$ = 10	Exp.												
	Calc.												

3.1) Assemble the basic electrical circuit of a subtractor using an operational amplifier in the EWB program (Figure 6).

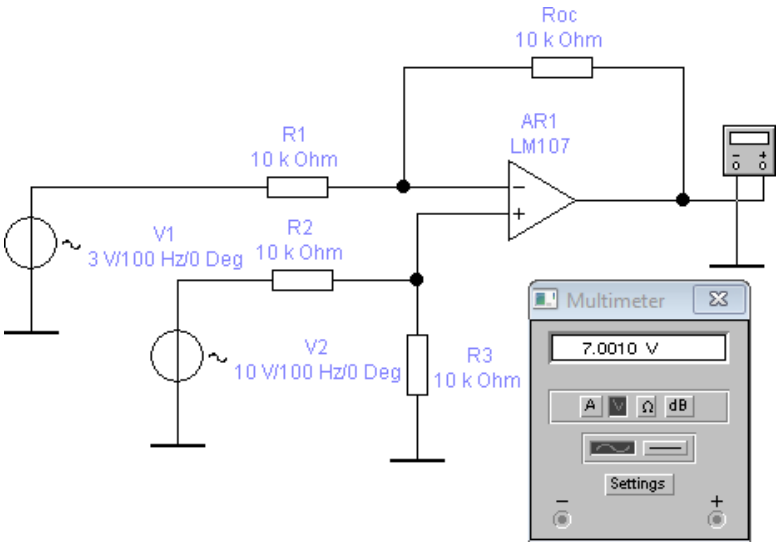
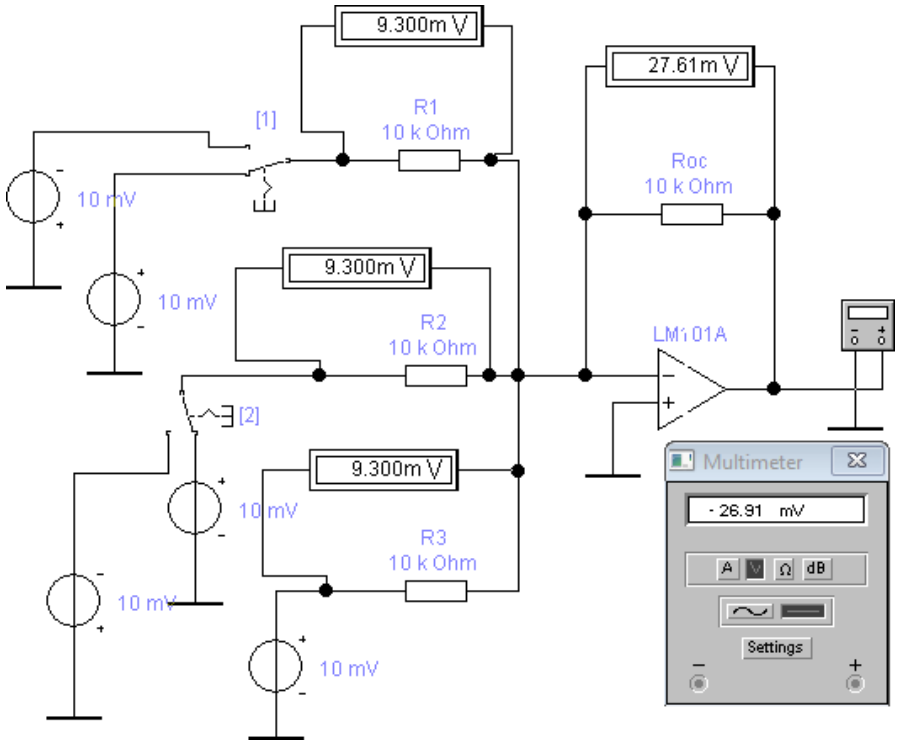


Figure 6 – Schematic diagram subtractor on op amp

3.2) Repeat points 1.2 - 1.5. Results calculations add in the report.

3.3) Do conclusions By results research.

4.1) Assemble the basic electrical circuit of a DC voltage adder on an operational amplifier using the EWB program (Figure 7).



Drawing 7 - Fundamental scheme adder permanent stresses on OU

4.2) Repeat points 1.2 - 1.6. Results calculations add in the report.

4.3) Do conclusions By research results .

<u>Exercise 2.</u> Study principles work And parameters differentiator on OU.

statement :

Necessary on base selected OU analyze principles work differential-ciator, define And conduct study following his parameters:

- coefficient voltage amplification ;

- difference phases between weekend And input voltage;
- amplitude-frequency characteristics (frequency response);

Conduct measurements, calculations and analysis of the values of the RC circuit dependence on the gain and phase difference between the output and input voltage.

Order execution tasks 2

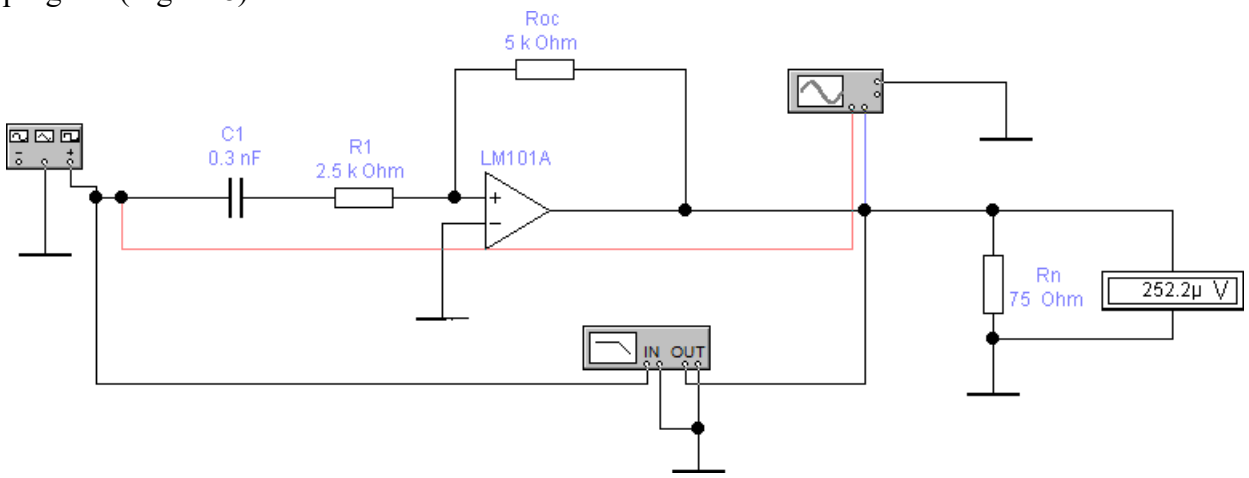
1) Calculate R1 values And C1 according to the formula

$$C1 := \frac{1}{2\pi \cdot R_{oc} \cdot f_{min}}$$

$$R1 := \frac{1}{2\pi \cdot C_1 \cdot f_{max}}$$

Where R_{os} = 5 kOhm, f_{min} = 5 kHz, f_{max} = 10 kHz

2) Assemble the basic electrical circuit of a differential amplifier using the EWB program (Figure 8).



Drawing 8 - Fundamental scheme differentiator at the educational institution

3) In the function generator, set the input signal frequency to 5-10 kHz and amplitude to 1 V.

4) The capacity of the capacitor should be selected so that the oscillogram of rectangular pulses is approximately as in Figure 9-10.

5) Consistently install R1 value = 2R1 And R1 = R1/2.

6) Calculate the voltage gain in times and in dB using the formulas $K_u = R_{oc}/R_1$, $K_u[dB] = 20*\log(K_u)$. Enter the calculation results into Table 3.

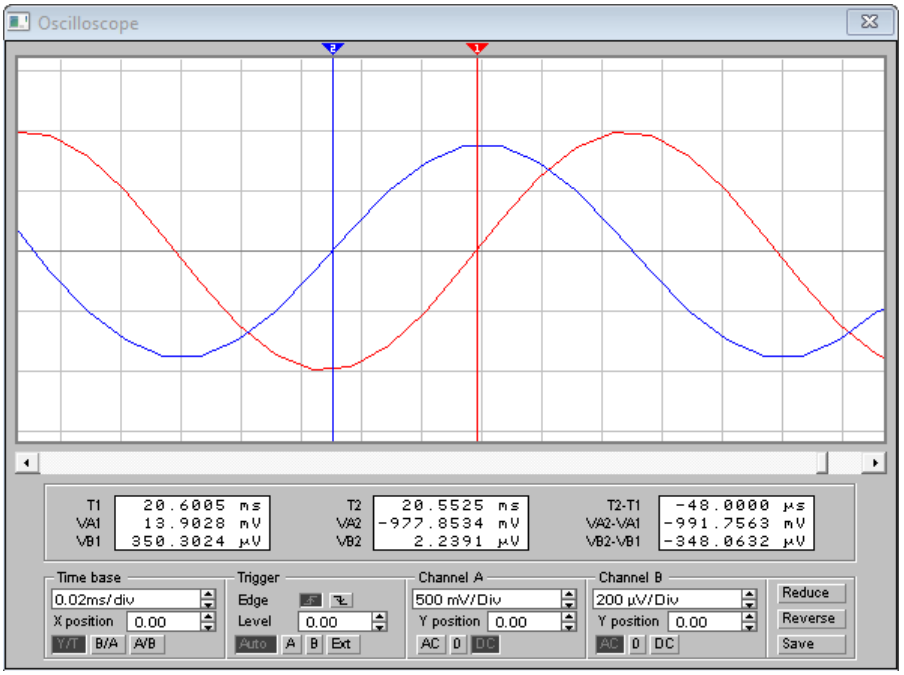
7) Measure the phase difference between the input and output signals and calculate the angle between the signals using the formula φ = 360 f (T1-T2). Record the calculation results and the oscillograms in the report.

8) WITH help Bode Plotter get measured coefficient gains V dB and compare with the calculated ones. Add the resulting frequency responses to the report.

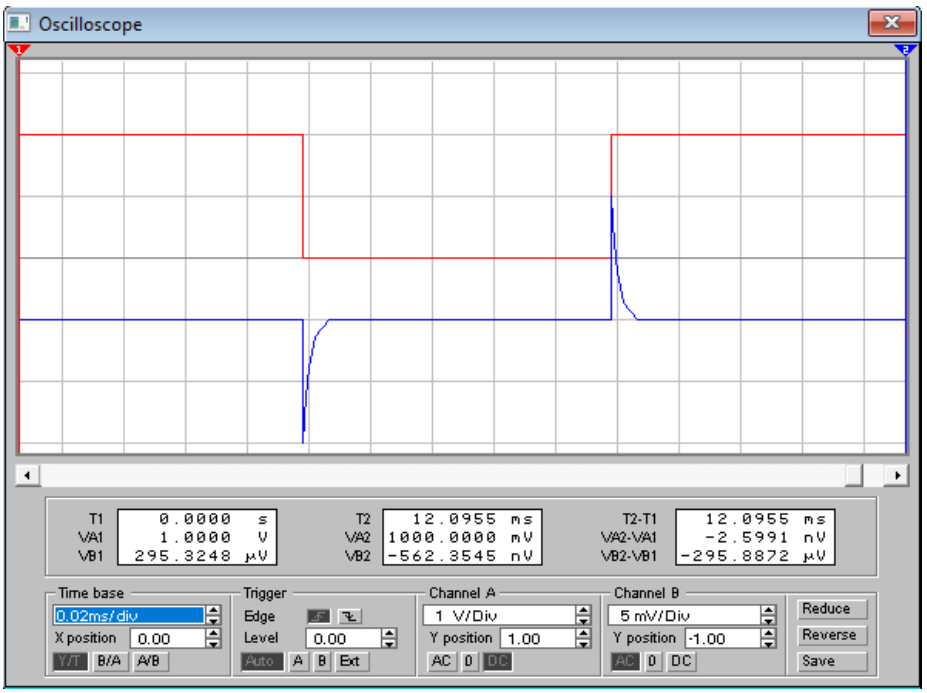
9) Consistently install value of C1 = 2C1 and C1 = C1/2.

10) Repeat points 3- 6.

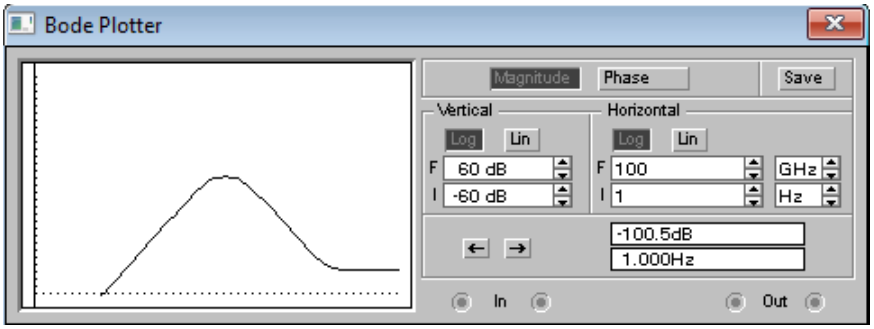
11) Do conclusion By research results .



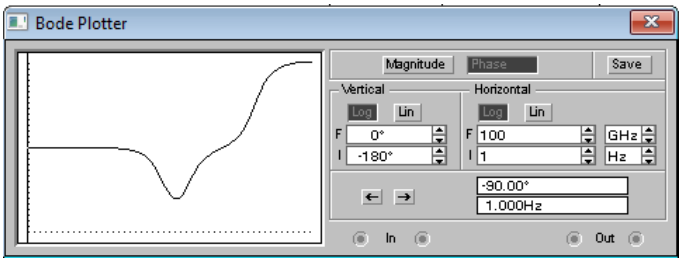
Drawing 9 - Example of an oscillogram of a harmonic signal



Drawing 10 - Example oscillograms rectangular pulses



Drawing 11 – Frequency response example



Drawing 12 - Example Phase

response Table 3 – Results of measurements and calculations

Параметры	K_U, раз	$K_{U.расчит}$, дБ	$K_{U.измер}$, дБ	ϕ, град
0,5R1				
R1				
2R1				
0,5C				
C				
2C				

Exercise 3. ***Study principles work And parameters integrator on OU. Problem statement:***

It is necessary to analyze the operating principles of the integrator on the basis of the selected operational amplifier , determine and conduct a study of its following parameters:

- coefficient voltage amplification ;
- difference phases between weekend And input voltage;
- amplitude-frequency characteristics (frequency response);

Conduct measurements, calculations and analysis of the values of the RC circuit dependence on the gain and phase difference between the output and input voltage.

Order execution tasks 3

1) Calculate R1 values And C1 according to the formula

$$C1 := \frac{1}{2\pi \cdot R_{oc} \cdot f_{min}}$$

$$R1 := \frac{1}{2\pi \cdot C_1 \cdot f_{max}}$$

Where $R_{os} = 5$ kOhm, $f_{min} = 5$ kHz, $f_{max} = 10$ kHz

2) Assemble the basic electrical circuit of the integrator on the operational amplifier in the EWB program (Figure 13).

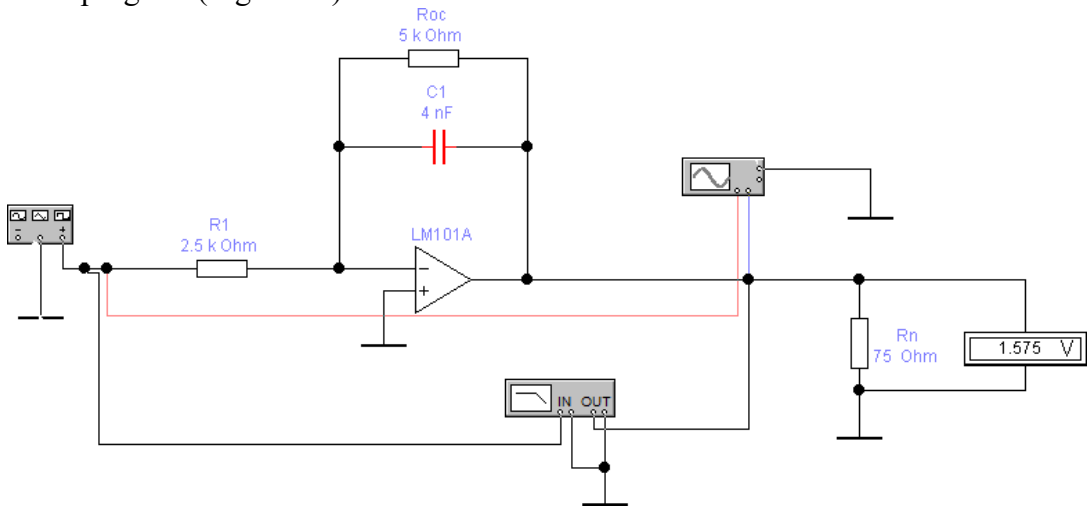


Figure 13 – Schematic diagram of the integrator on the op amp

3) In the function generator, set the input signal frequency to 5-10 kHz and amplitude to 1 V.

4) The capacity of the capacitor should be selected so that the oscillogram of rectangular pulses is approximately as in Figure 15.

5) Consistently install R1 value = 2R1 And R1 = R1/2.

6) Calculate the voltage gain in times and in dB using the formulas $K_u = R_{oc}/R_1$, $K_u[dB] = 20*\log(K_u)$. Enter the calculation results into Table 3.

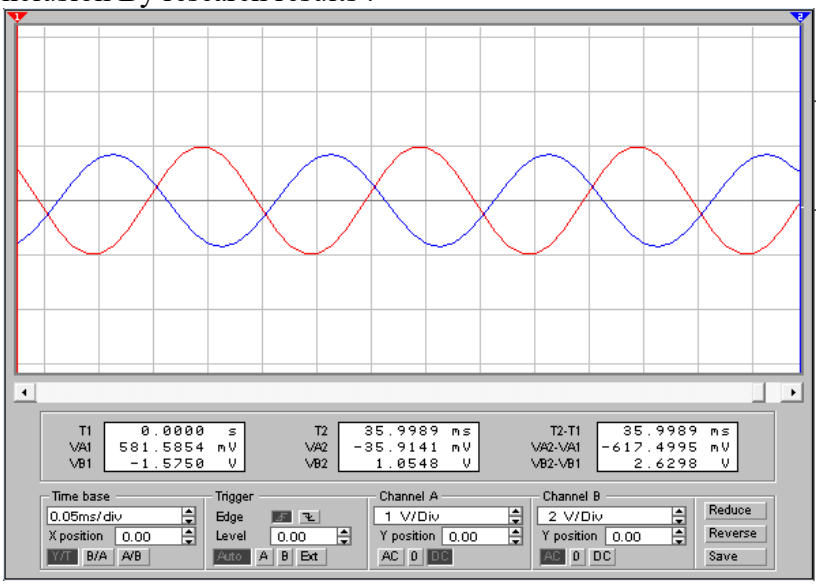
7) Measure the phase difference between the input and output signals and calculate the angle between the signals using the formula $\varphi = 360\ f\ (T1-T2)$. Record the calculation results and the oscillograms in the report.

8) WITH help Bode Plotter get measured coefficient gains V dB and compare with the calculated ones. Add the resulting frequency responses to the report.

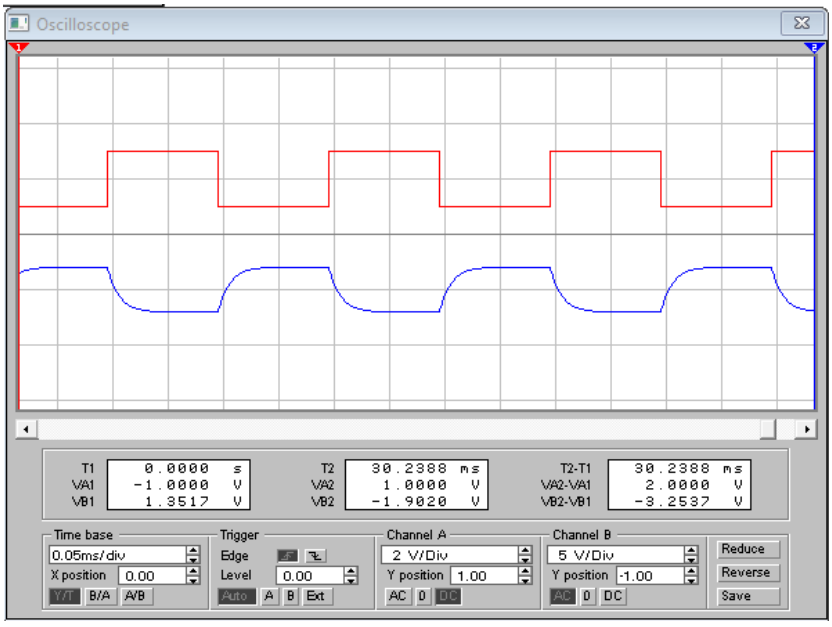
9) Consistently install value of C1 = 2C1 and C1 = C1/2.

10) Repeat points 3- 6.

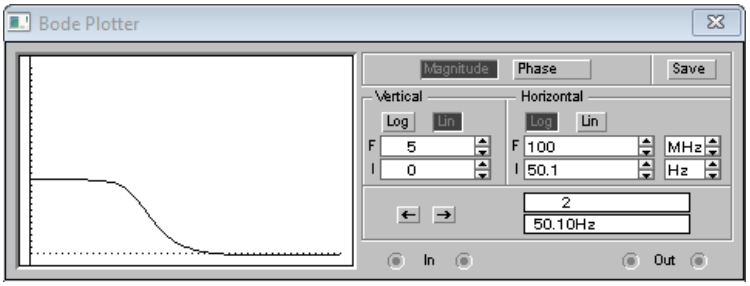
11) Do conclusion By research results .



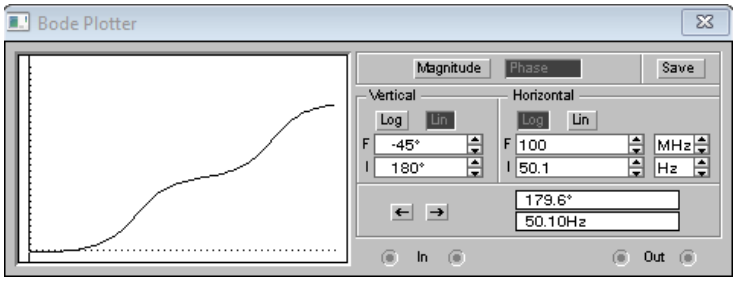
Drawing 14 – Example of an oscillogram of a harmonic signal



Drawing 15 – Example of an oscillogram of rectangular pulses



Drawing 16 – Frequency response example



Drawing 17 - Example Phase

response Table 4 – Results of measurements and calculations

Параметры	**K_U, раз**	**$K_{U.расчит}$, дБ**	**$K_{U.измер}$, дБ**	**ϕ, град**
0,5R1				
R1				
2R1				
0,5C				
C				
2C				

<u>Exercise 4. (For independent work)</u> Design results research in the form of a laboratory report and defend it.

1.1) IN report By laboratory work display:

– topic And target work, tasks For research And brief order their execution;

– the basic electrical circuits of the investigated circuits on the op amp, modeled in the schematic modeling editor;

– oscillograms input and output signals;

– graphs frequency response With results measurements frequency parameters;

– conclusions By results execution tasks And V in general By work done .

5.2) Defend a report on the completed laboratory work, having completed an individual - assignment specified by the teacher, within the framework of the research conducted.

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 8

TOPIC RESEARCH ACTIVE FILTERS ON OPERATIONAL AMPLIFIERS

Time – 4 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– realize circuit design (computer) modeling active filters on operational amplifiers using universal software packages ;

– conduct research into the operating principles, main characteristics and parameters of active filters on operational amplifiers;

– collection and analysis of information to form initial data for the design of active filters on operational amplifiers.

TRAINING AND MATERIAL SUPPORT:

– PC with the electronic circuit simulator "Electronics Workbench – 5.12" and the - computer mathematics system "Mathcad – 15"

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Modeling And study frequency characteristics ARC filters second order.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**65 min**
2. Modeling And study frequency characteristics ARC filters fourth order.	65 min
The final part	**15 min**
Defense of practical work reports	10 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

1. General intelligence about active filters

Active filters are filters that contain an active element that uses an additional power source.

Active filters are implemented on the basis of amplifiers (usually op-amps) and passive ones. RC filters. As the filter order increases, its filtering

Depending on the frequency characteristics, the following types of filters are distinguished: low-pass frequencies (LPF), top frequencies (HPF), striped (FP), striped rejector

(FPR) Sometimes called filter plugs. General at everyone these filters is that their transfer functions are divided into two zones: pass and reject. The boundary between these zones is called the critical frequency or the frequency break frequency. The main parameters resistors are nominal resistance And his acceptable from deviation from denomination. Denominations resistors follows choose V within from 1 to 100 kOhm. Lower limit conditioned by limitation on output currents OU, upper limit 100 kOhm prevents excessive resistor noise.

Basic characteristic filter is his amplitude-frequency frequency response (AFC), i.e. the dependence of the absolute value of the transmission coefficient K or its inverse, the attenuation a = 1/K, on the signal frequency. For ideal filters, there are cutoff frequencies separating the transmission (a = 0) and rejection (a = 1) regions, and the filter attenuation in fits and starts changes at transition from stripes transmission To strip delays . IN real filters stripes transmission And delays are separated transition zone, V which coefficient attenuation changes continuously from maximum allow my to minimally acceptable V strip delays (az). Instead of frequencies cut two cutoff frequencies appear : the passband cutoff frequency and the stopband cutoff frequency. The smaller the difference between ω and ω_3 ,, the higher the quality of the filter.

Note that the active filter circuits do not change depending on the frequency response approximation type, but the ratios between the values of their elements change.

The critical frequency (or -3 dB point) is the frequency at which the filter's gain is -3 dB (or 1/ $\sqrt{2}$ times) lower than the passband frequency response . weakening signal V zone barriers filter is determined his in order. How higher
order the filter, the cooler frequency response in the fenced area.

Among advantages active filters in comparison With passive follows highlighted-pour:

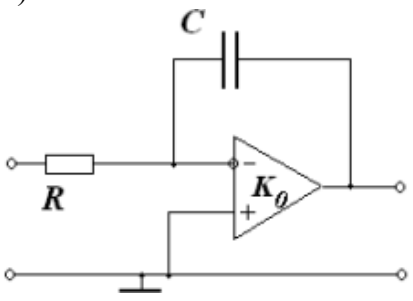
- absence induction coils ;
- the best selectivity;
- compensation attenuation useful signals or even their strengthening;
- suitability To implementation V view

IMS. Active filters have And flaws:

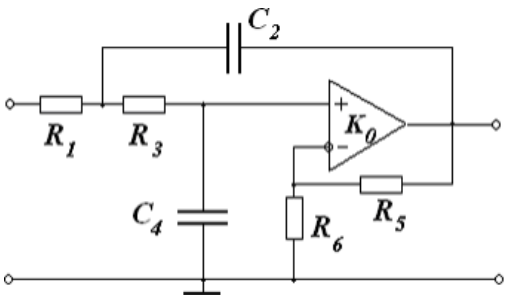
- consumption energy from source nutrition;
- limited dynamic range;
- additional nonlinear distortions signal. The main

parameters ARC filters is:

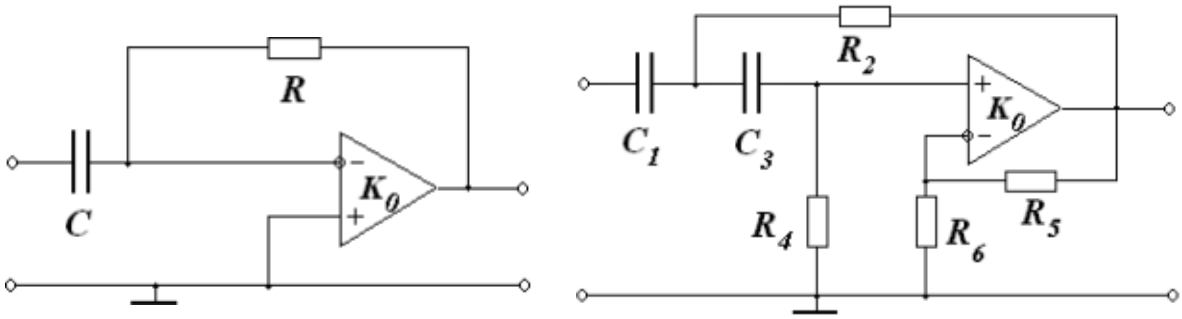
1) *frequency cut f* $_s$ - This frequency, at which *K and* filter falls to level 0.707 from *K and* V strip transmission (i.e. falls on 3 dB);
2) *stripe transmission* — This stripe frequencies, V which signal transmitted without distortion;
3) *stripe suppression* — This stripe frequencies, V which signal is suppressed to for - this level;
4) *quality factor* Q — This value, connecting average frequency bandwidth and its width at the level of 3 dB
5) *order*



A)



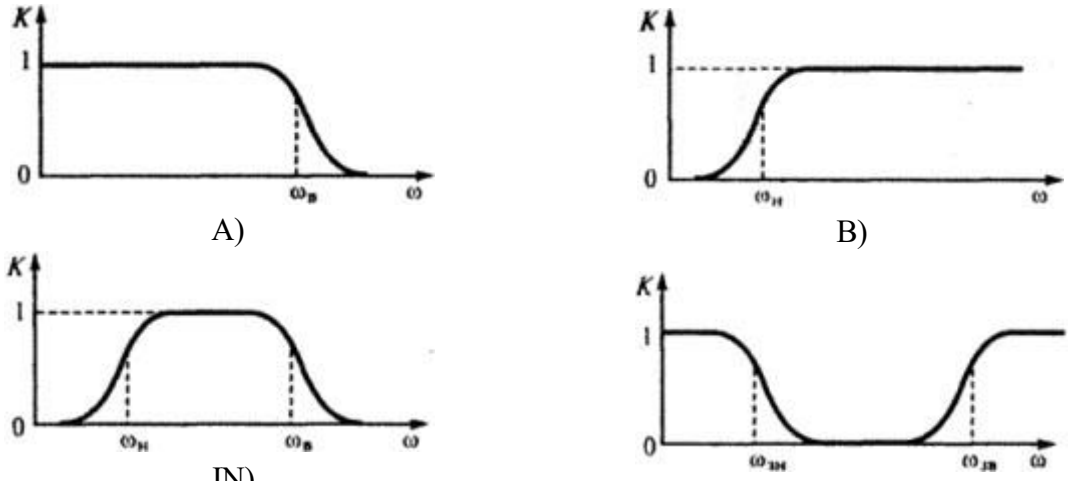
B)



IN) G)

Drawing 1 -Filters low-pass filter And HPF: A) LPF, b) low-pass filter second order, V) HPF, G) HPF second order.

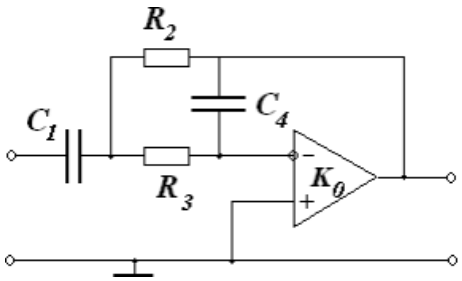
Let us give examples frequency response active filters:



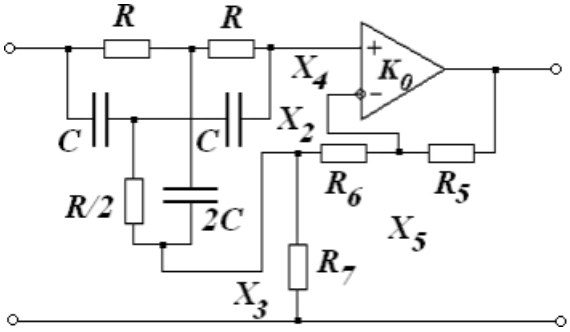
A) B)

IN) G)

Drawing 2 - frequency response filters various types: a) LPF, b) HPF, V) PF, G) Russian Federation.



Drawing 3 - Active striped filter



Drawing 4 - Notch filter

Size capacity C1 is selected close To meaning, determined By formula (1)

$$C_1 = \frac{10}{f_c} \text{мкФ} \quad (1)$$

Size capacity C2 located By formula (2)

$$C_2 \geq C_1 \frac{4b_i(1-K_0)}{a_i^2} \quad (2)$$

Size resistance values R1, R2, R3 is found by the formulas (3), (4), (5).

$$R_2 = \frac{a_1 C_2 - \sqrt{a_1^2 C_2^2 - 4C_1 C_2 b_1 (1-F_0)}}{2 \cdot 2\pi f_c C_1 C_2} \quad (3)$$

$$R_1 = -\frac{R_2}{F_0}$$

$$R_1 = -\frac{R_2}{-1} = R_2 \quad (4)$$

$$R_3 = \frac{1}{(2\pi f_c)^2 C_1 C_2 R_2} \quad (5)$$

Content practical work, performed students **Description of laboratory equipment:**

– PC for each student;

– program editor schematic modeling "ElectronicsWorkbench" (EWB) version no lower than 5.12 or NIMultisim Education version;

– an application for mathematical and engineering calculations, version not lower than 15.0.

Requirements security at execution works:

1) TO conducting laboratory works allowed students, past required safety briefings.

2) Turning on laboratory installations (computers) is being carried out only With once the teacher's decision.

3) When conducting laboratory work, it is not permitted to use devices or equipment that are not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) At occurrence emergency situations necessary immediately turn off equipment from the power supply network, inform the teacher about this and act according to his instructions .

6) At fire equipment his necessary immediately de-energize, report this to the teacher, take measures to eliminate the fire and act according to the teacher’s instructions.

7) By ending work With laboratory equipment (computers) his must be switched off in the established order.

Tasks to be completed during the Basic Level practical work:

1) Simulate And research amplitude-frequency characteristics (frequency response) of the second-order low-pass ARC filter and plot their graphs.

2) Simulate And research amplitude-frequency characteristics (frequency response) of the second-order high-pass ARC filter and plot their graphs.

3) Simulate And research amplitude-frequency characteristics (frequency response) of the fourth-order ARC low-pass filter and plot their graphs.

4) Simulate And research amplitude-frequency characteristics (frequency response) of the fourth-order high-pass ARC filter and plot their graphs.

Advanced level:

5) Simulate And research amplitude-frequency characteristics (frequency response) by - bandpass ARC filter and plot their graphs.

Initial data for modeling and research

Table 1 - Options tasks For modeling and research.

Option	f_s, kHz	a_i	b_i
0	1.2124	1.4142	1
1	1.272	1	1
2	1	1.3617	1
3	1.414	0.9996	0.4772
4	1.797	0.7743	0.389
5	1	1.3614	1.3827
6	1.335	0.6402	1.1931
7	0.538	2.6282	3.44341
8	1.419	0.3548	1.1509
9	1.797	0.7743	0.3890
10	1	1.3614	1.3827
11	1	1.0650	1.9305
12	1.410	0.1964	1.2009

Order execution works:

Task 1. Model and investigate the amplitude-frequency response (AFR) of a second-order low-pass ARC filter.

1) IN application For mathematical And engineering Mathcad calculations Professional calculate the parameters of the circuit elements. To do this, follow these steps:

1.1) Enter formulas And calculate next parameters:

- Positive valid coefficient;

$$a_j := 1.4142 \;;$$

- Positive valid coefficient

$$b_j := 1 \;;$$

- Coefficient

$$F_0 := -1 \;;$$

- Size capacity C1

$$C1 := \frac{10}{f} \cdot 10^{-6} = 8.248 \times 10^{-9} \quad Ф$$

- Size capacity C2

$$C2 := C1 \cdot \frac{4 \cdot b_j \cdot 2}{(a_j)^2} = 32.993 \times 10^{-9} \quad Ф$$

;

- Resistance R2

$$R2 := \frac{a_j \cdot C2 - \sqrt{a_j^2 \cdot C2^2 - 4C1 \cdot C2 \cdot b_j \cdot (1 - F_0)}}{2 \cdot 2\pi \cdot f_N \cdot C1 \cdot C2} = 11.254 \times 10^3 \quad Ом$$

;

- Resistance R1

$$R1 := R2 = 11.254 \times 10^3 \quad Ом$$

- Resistance R3

$$R3 := \frac{1}{(2 \cdot \pi f)^2 \cdot C1 \cdot C2 \cdot R2} = 5.627 \times 10^3 \quad Ом$$

;

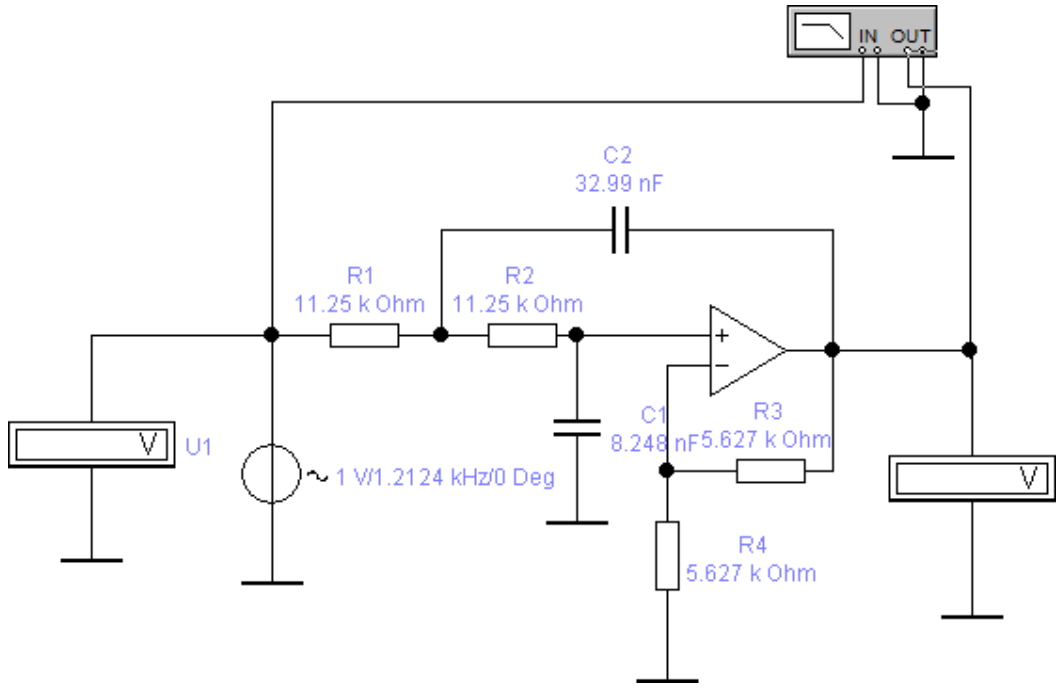
- Resistance R4

$$R4 := R3 = 5.627 \times 10^3 \quad Ом$$

;

1.2) Bring in V report By laboratory work listing dialed programs in Mathcad with calculation results.

2) Assemble the electrical circuit of the second-order low-pass ARC filter in the EWB program (Figure 1).



Drawing 1 - Simulated circuit

3) In the assembled circuit model, check the correctness of the assembly, referring to , before in total, attention on correct compound elements schemes Friend To to a friend, A

also connection of measuring instruments and switching keys, paying special attention to the connection of the power source and grounding.

The procedure for setting up, debugging and checking the performance of the simulated circuit.

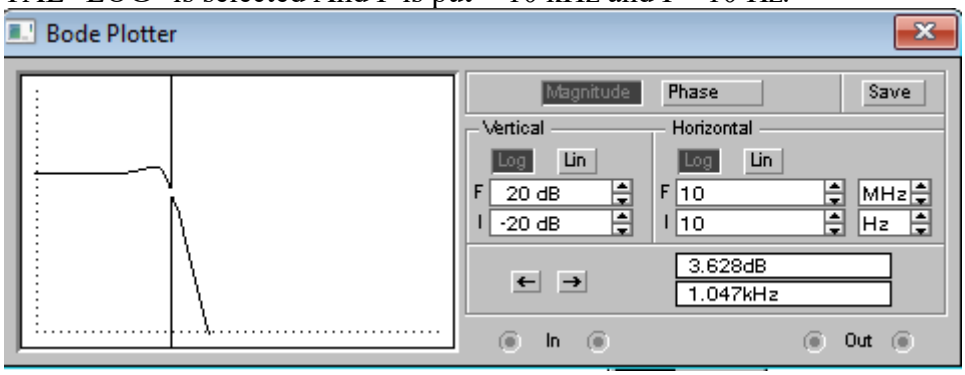
1) Enter V collected diagram given or calculated parameters elements:

- Frequency V source signal (generator EMF) install according to given option, and the voltage is equal to 1 V.
- Resistance R1, R2, R3, R4
- Capacitors C1, C2

2) Tune means measurements, For this execute next operations:

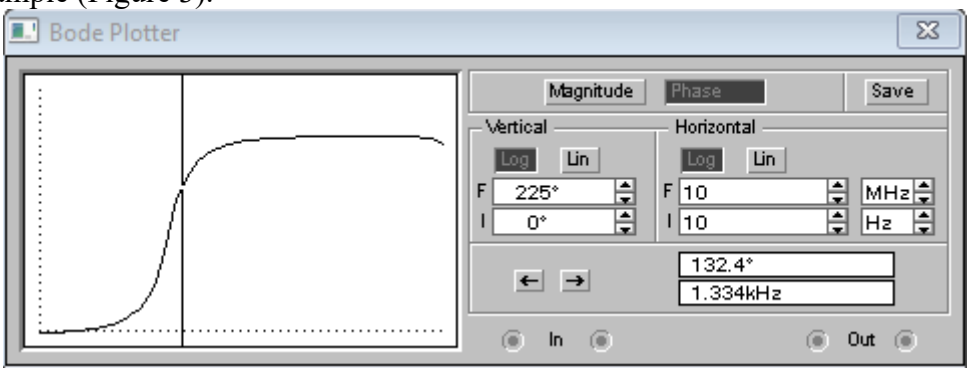
- Voltmeters translate V mode measurements alternating voltage.

3) It is being removed frequency response on bode-plotter. For this is selected V panels "VERTICAL" "LOG", be put F = 20 dB And I = -20 dB (example shown on drawing 2), in tab HORIZONTAL "LOG" is selected And F is put = 10 kHz and I = 10 Hz.



Drawing 2 – frequency response on bode plotter.

By analogies is being done And With phase. It is selected V panels "VERTICAL" is selected «LOG» F = 225 º , I = 0 º . In the «HORIZONTAL» panel «LOG» and set F = 10 MHz and I = 10 Hz. Example (Figure 3).



Drawing 3 – phase response on bode plotter.

Define frequency cut With help frequency response and phase response. 1)For this do next: the frequency response is set to a sight at the -3 dB mark (Figure 2):

$$f_{заданная} := 1.2124 \cdot 10^{3} \ Гц$$

$$f_{снятая} := 1.047 \cdot 10^{3} \ Гц$$

$$A := f_{заданная} - f_{снятая}$$

$$|A| = 165.4$$

$$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 15.798 \ \%$$

Where A - absolute error, δ - relative error in percent.

$f_{заданная} := 1.2124 \cdot 10^3$ Гц

$f_{снятая} := 1.334 \cdot 10^3$ Гц

$A := f_{заданная} - f_{снятая}$

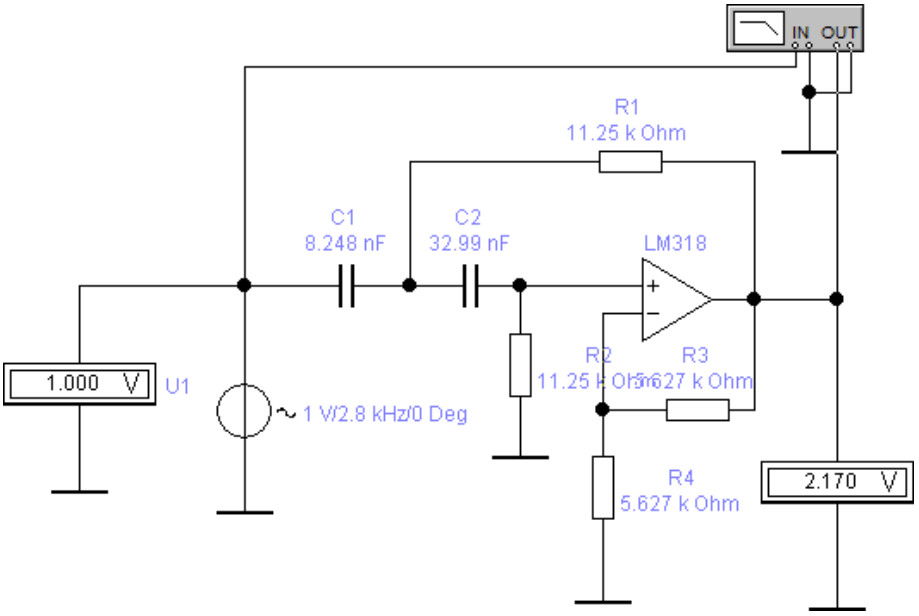
$|A| = 121.6$

$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 9.115$ %

Where A - absolute error, δ - relative error V percent. Draw conclusions based on the laboratory work.

Task 2. Model and investigate the amplitude-frequency response (AFR) of a second-order high-pass ARC filter.

1) Assemble the electrical circuit of a second-order high-pass ARC filter using the EWB program (Figure 4). To assemble the circuit of a second-order high-pass ARC filter, we will swap the resistors and capacitors.



Drawing 4 - Simulated circuit

2) In the assembled circuit model, check the correctness of the assembly, referring to , before in total, attention on correct compound elements schemes Friend To to a friend, as well as connecting measuring instruments and switching keys, paying particular attention to connecting the power source and grounding.

The procedure for setting up, debugging and checking the performance of the simulated circuit.

1) Enter V collected diagram given or calculated parameters elements:

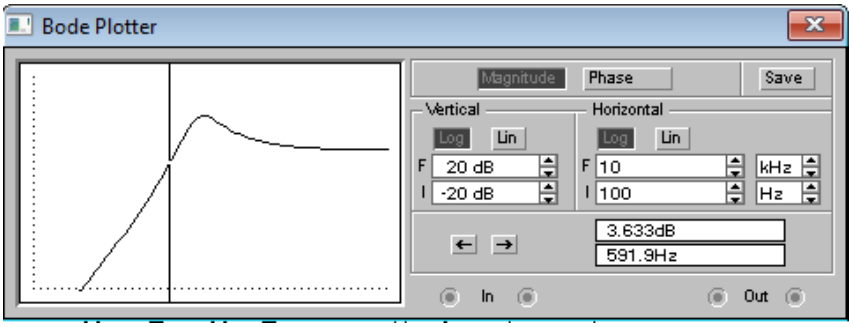
- Frequency V source signal (generator EMF) install according to given option, and the voltage is equal to 1 V.
- Resistance R1, R2, R3, R4
- Capacitors C1, C2

2) Tune means measurements, For this execute next operations:

- Voltmeters translate V mode measurements alternating voltage.

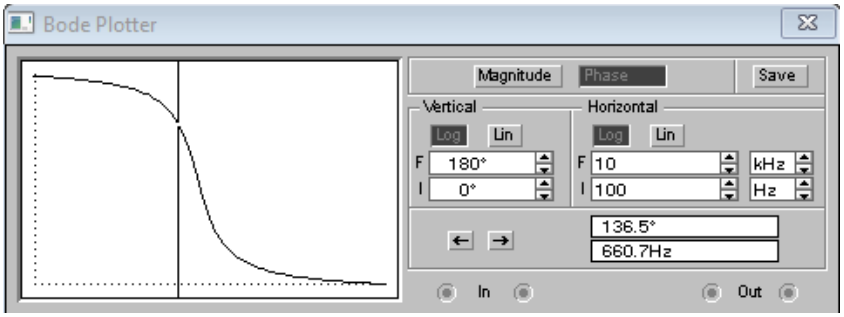
3) It is being removed frequency response on bode-plotter. For this is selected V panels "VERTICAL"

"LOG", be put F = 20 dB And I = -20 dB (example shown on drawing 2), in tab HORIZONTAL "LOG" is selected And F is put = 10 kHz and I = 10 Hz.



Drawing 5 – frequency response on bode plotter.

By analogies is being done And With phase. It is selected V panels "VERTICAL" is selected
«LOG» F = 180 º , I = 0 º . In the «HORIZONTAL» panel «LOG» is set to F = 10 kHz and I = 100 Hz.



Drawing 6 – phase response on bode plotter.

Determine the cutoff frequency using the frequency response and phase response. To do this, follow these steps: set the frequency response sighting target at -3 dB (Figure 5):

$$f_{заданная} := 1.2124 \cdot 10^{3} \ Гц$$

$$f_{снятая} := 591.9 \quad Гц$$

$$A := f_{заданная} - f_{снятая}$$

$$|A| = 620.5$$

$$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 104.83\ \%$$

Where A - absolute error, δ - relative error in percent.
For this case, calculating $f_{calculated}$ By phase response is calculated How:

1) It is being put sight on 135 degrees, frequency is measured

$$f_{заданная} := 1.2124 \cdot 10^{3} \ Гц$$

$$f_{снятая} := 660.7 \quad Гц$$

$$A := f_{заданная} - f_{снятая}$$

$$|A| = 551.7$$

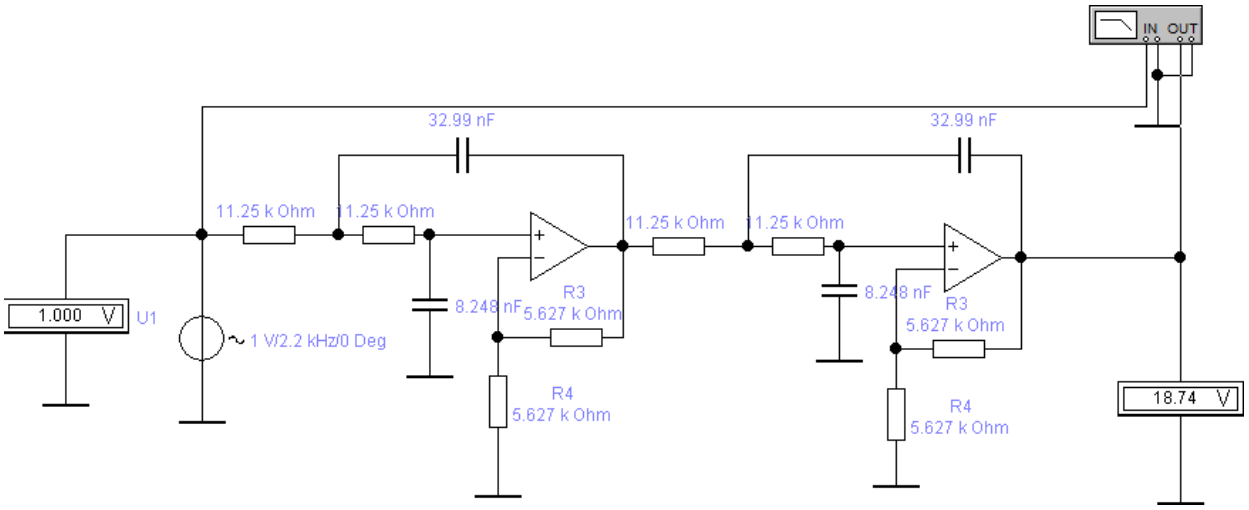
$$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 83.502\ \%$$

Where A - absolute error, δ - relative error in percent.

Do conclusions By laboratory work.

Task 3. Model and investigate the amplitude-frequency response (AFR) of a fourth-order low-pass ARC filter.

1) Assemble the electrical circuit of the ARC low-pass filter in the EWB program fourth order. So How ARC filter Thursday order consists of from two cascades of the second-order low-pass ARC filter, we connect these two cascades (Figure 7).



Drawing 7 - Simulated circuit

2) In the assembled circuit model, check the correctness of the assembly, referring to , before in total, attention on correct compound elements schemes Friend To to a friend, as well as connecting measuring instruments and switching keys, paying particular attention to connecting the power source and grounding.

The procedure for setting up, debugging and checking the performance of the simulated circuit.

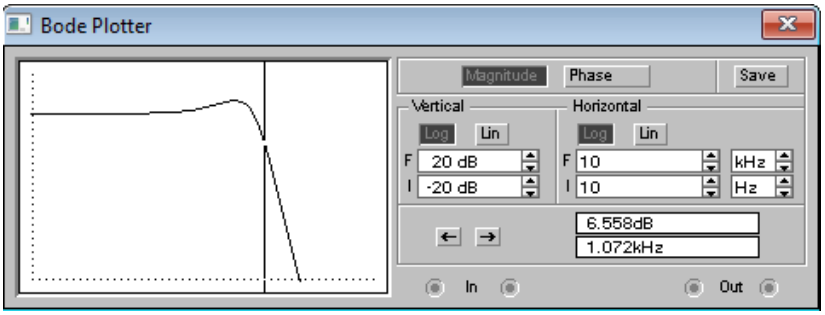
1) Enter V collected diagram given or calculated parameters elements:

- Frequency V source signal (generator EMF) install according to given option, and the voltage is equal to 1 V.
- Resistance R1, R2, R3, R4
- Capacitors C1, C2

2) Tune means measurements, For this execute next operations:

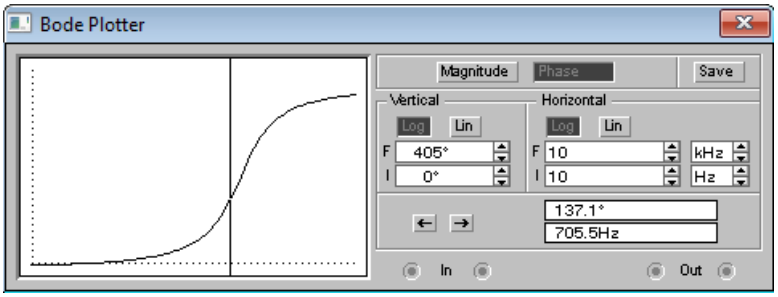
- Voltmeters translate V mode measurements alternating voltage.

3) It is being removed frequency response on bode-plotter. For this is selected V panels VERTICAL
"LOG", be put F = 20 dB And I = -20 dB, in tab HORIZONTAL is selected "LOG" and set F = 10 kHz and I = 10 Hz.



Drawing 8 – frequency response on bode plotter.

By analogies is being done And With phase. It is selected V panels VERTICAL is selected «LOG» F = 405 °, I = 0 °. In the «HORIZONTAL» panel «LOG» is set to F = 10 kHz and I = 100 Hz.



Drawing 9 - phase response on bode plotter.

The cutoff frequency is determined using the frequency response and phase response. For this the cursor is set to the cutoff frequency and the error is determined: $f_{given} - f_{removed}$.
For this case, calculating $f_{calculated}$ By frequency response is calculated How, is put sighting device on cancel V
-3dB (drawing 8):

$$f_{заданная} := 1.2124 \cdot 10^3 \ Гц$$

$$f_{снятая} := 1.072 \cdot 10^3 \ Гц$$

$$A := f_{заданная} - f_{снятая}$$

$$|A| = 140.4$$

$$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 13.097 \ \%$$

Where A - absolute error, δ - relative error V percent. For this case, calculating $f_{calculated}$ is according to the phase response it is calculated as:

1) It is being put sight on 135 degrees, frequency is measured

$$f_{заданная} := 1.2124 \cdot 10^3 \ Гц$$

$$f_{снятая} := 705.5 \ Гц$$

$$A := f_{заданная} - f_{снятая}$$

$$|A| = 506.9$$

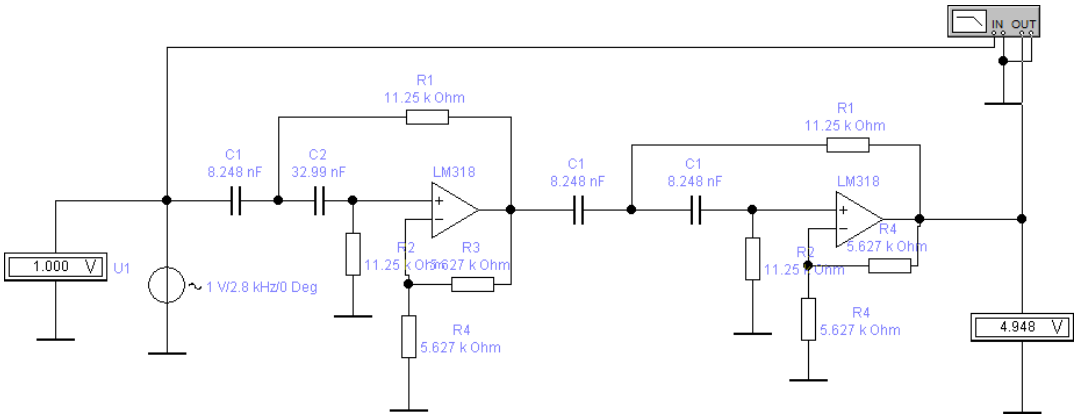
$$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 71.85 \ \%$$

Where A - absolute error, δ - relative error in percent.

Do conclusions By laboratory work.

Task 4. Model and investigate the amplitude-frequency response (AFR) of a fourth-order high-pass ARC filter.

1) Assemble the electrical circuit of the ARC high-pass filter in the EWB program fourth order So How ARC filter fourth order consists of from two ARC filter cascades top frequencies second order, let's connect two these cascade (drawing 10). By analogy with task 1.2, we swap the resistors and capacitors compared to the fourth-order ARC low-pass filter.



Drawing 10 - Simulated circuit

2) In the assembled circuit model, check the correctness of the assembly, referring to , before in total, attention on correct compound elements schemes Friend To to a friend, as well as connecting measuring instruments and switching keys, paying particular attention to connecting the power source and grounding.

The procedure for setting up, debugging and checking the performance of the simulated circuit.

1) Enter V collected diagram given or calculated parameters elements:

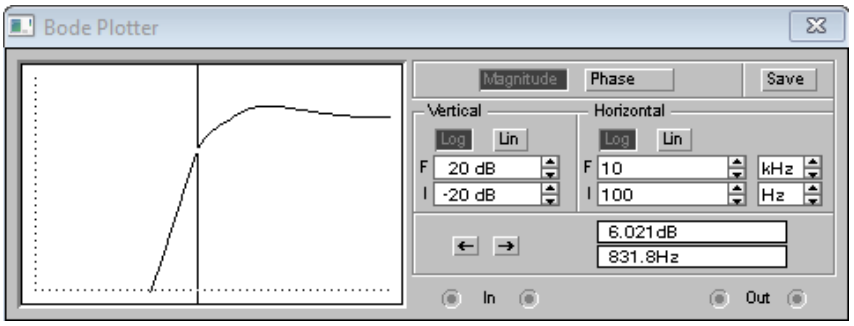
- Frequency V source signal (generator EMF) install according to given option, and the voltage is equal to 1 V.
- Resistance R1, R2, R3, R4
- Capacitors C1, C2

2) Tune means measurements, For this execute next operations:

- Voltmeters translate V mode measurements alternating voltage.

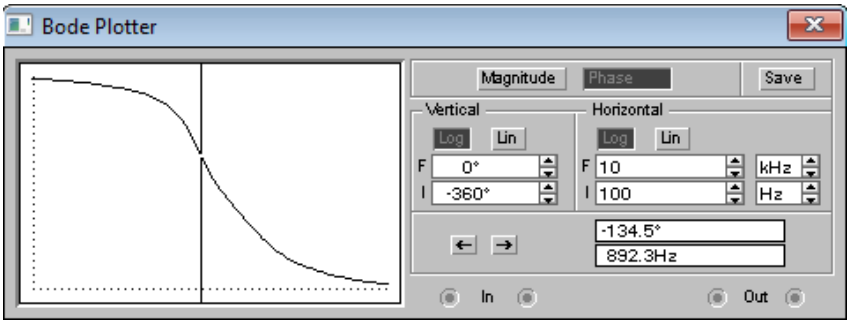
3) It is being removed frequency response on bode-plotter. For this is selected V panels "VERTICAL"

"LOG", be put F = 20 dB And I = -20 dB, in tab HORIZONTAL is selected "LOG" and set F = 10 kHz and I = 100 Hz.



Drawing 11 – Frequency response on bode plotter.

By analogies is being done And With phase. It is selected V panels VERTICAL is selected «LOG» F = 0 °, I = -360 °. In the «HORIZONTAL» panel «LOG» is set to F = 10 kHz and I = 100 Hz.



Drawing 12 – Phase response on bode plotter.

It is being determined frequency cut With help frequency response And Phase-frequency response. For this is being installed the cursor is set to the cutoff frequency and the error is determined: $f_{given} - f_{removed}$.
For this case, calculating $f_{calculated}$ By frequency response is calculated How, is put sighting device on cancel V
-3dB (drawing 11):

$$f_{заданная} := 1.2124 \cdot 10^3 \ Гц$$

$$f_{снятая} := 831.8 \ Гц$$

$$A := f_{заданная} - f_{снятая}$$

$$|A| = 380.6$$

$$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 45.756\ \%$$

Where A - absolute error, δ - relative error V percent. For this case, calculating $f_{is\ calculated}$ according to the phase response it is calculated as:

1) It is being put sight on 135 degrees, frequency is measured

$$f_{заданная} := 1.2124 \cdot 10^3 \ Гц$$

$$f_{снятая} := 892.3 \ Гц$$

$$A := f_{заданная} - f_{снятая}$$

$$|A| = 320.1$$

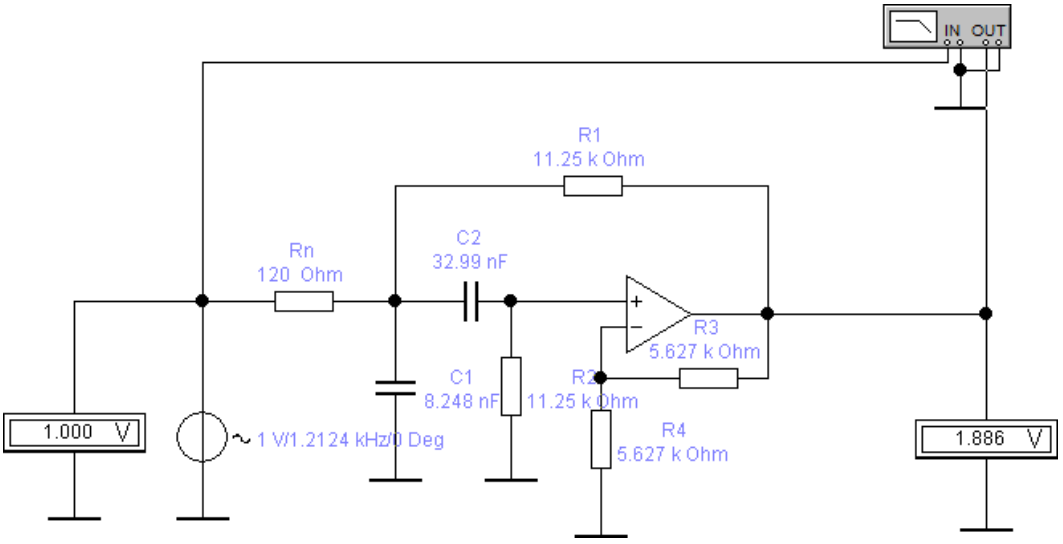
$$\delta := \frac{|A|}{f_{снятая}} \cdot 100 = 35.874\ \%$$

Where A - absolute error, δ - relative error in percent.

Do conclusions By laboratory work.

Task 5. Model and investigate the amplitude-frequency response (AFR) of a bandpass link.

3) Collect V program EWB electrical diagram striped link (drawing 13).



Drawing 13 - Modeled scheme

4) In the assembled circuit model, check the correctness of the assembly, referring to , before in total, attention on correct compound elements schemes Friend To to a friend, as well as connecting measuring instruments and switching keys, paying particular attention to connecting the power source and grounding.

The procedure for setting up, debugging and checking the performance of the simulated circuit.

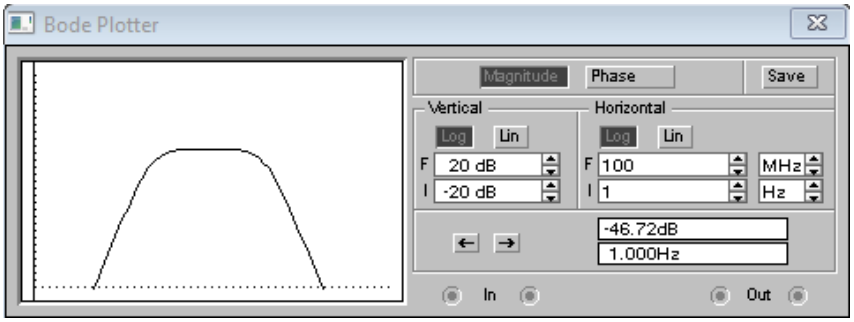
2) Enter V collected diagram given or calculated parameters elements:

- Frequency V source signal (generator EMF) install according to given option, and the voltage is equal to 1 V.
- Resistance R1, R2, R3, R4
- Capacitors C1, C2

2) Tune means measurements, For this execute next operations:

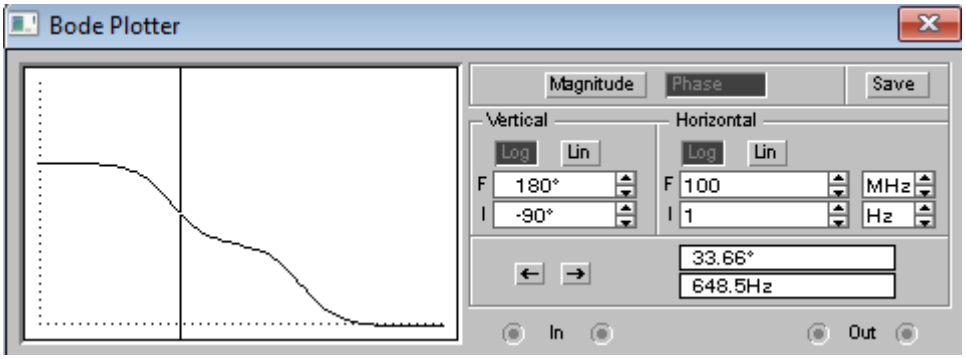
- Voltmeters translate V mode measurements alternating voltage.

3) It is being removed frequency response on bode-plotter. For this is selected V panels VERTICAL "LOG", be put F = 20 dB And I = -20 dB, in tab HORIZONTAL is selected "LOG" and set F = 100 MHz and I = 1 Hz.



Drawing 14 – Frequency response on bode plotter.

By analogies is being done And With phase. It is selected V panels "VERTICAL" is selected "LOG" F = 180 °, I = -90 °. IN panels HORIZONTAL "LOG" And is put F = 100 MHz And I = 1 Hz.



Drawing 15 – Phase response on bode plotter.

Do conclusions By laboratory work.

<u>Exercise 6. (For independent work)</u> Design results research in the form of a laboratory report and defend it.

6.1) IN report By laboratory work display:

– topic And target work, tasks For research And brief order their execution;

– Schematic diagrams of the active filters under study, modeled in a schematic modeling editor;

– oscillograms input and output signals;

– graphs frequency response With results measurements frequency parameters;

– conclusions By results execution tasks And V in general By work done .

6.2) Defend a report on the completed laboratory work by completing an individual - assignment specified by the teacher, within the framework of the research conducted.

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 9

Subject: **STUDY AUTO GENERATORS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of various autogenerators using operational amplifiers using universal packages of applied computer programs;

– conduct research into the operating principles, main characteristics and parameters of various operational amplifier oscillators;

– collection and analysis of information to form initial data for the design of auto-oscillators on operational amplifiers.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling "ElectronicsWorkbench" (EWB), version no lower than 5.12 or NIMultisim Education version;

– MathcadProfessional application for mathematical and engineering calculations, version not lower than 15.0;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study principles work, parameters And characteristics autogen-ratator on op-amp with bridge Guilt.	50 min
2. Study parameters RC generator chains With phase-shifting ce-kidney "R- parallel".	20 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**60 min**
2. Study parameters RC generator chains With phase-shifting ce-kidney "R- parallel".	20 min
3. Study parameters RC generator chains With phase-shifting ce-kidney "WITH - parallel."	40 min
The final part	**20 min**
Defense of practical work reports	15 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

Generators on operating amplifiers are unstable schemes, those. they are specially designed to remain in an unstable or unstable state generation. Generators there are useful For generation standard signals, used as reference for applications in audio-related fields, as function generators, in digital systems and in communication systems.

Generators sinusoidal signal they work without filing on them external signal. Instead this applies combination positive or negative reverse connections that would translate amplifier V unstable state, What leads To cyclical The output signal changes from the minimum to the maximum supply voltage with a constant period. The frequency and amplitude of the oscillations are determined by a set of active and passive components connected to the operational amplifier.

Op-amp oscillators are limited to the low frequency range of the frequency spectrum because they lack the wide bandwidth required for achievements low phase shift on high frequencies. Operating amplifiers with voltage feedback are limited to the kilohertz frequency range, since dominant pole at open chains reverse connections Maybe be on to a fairly low frequency, such as 10 Hz. New current-coupled operational amplifiers have much big strip transmission, But their Very difficult use V generator circuits because they are sensitive to capacitances in the feedback circuits.

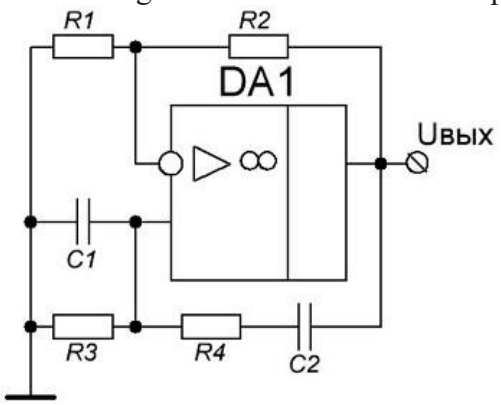
By principle of construction RC generators are divided into:

- generators With frequency-dependent positive reverse communication;
- generators With phase-shifting in chains V chains reverse connections.

Generator sinusoidal fluctuations on basis bridge Guilt

The Wien bridge sine wave generator is one of the most common RC sine wave generators. The circuit diagram of this generator is shown in Figure 1.

Figure 1 – Wien generator circuit based on op-amp.



The Wien oscillator consists of an op-amp, which is covered by negative feedback (NFB) via resistors R1 and R2, and positive feedback (PFC) via the frequency-selective circuit R3C1R4C2.

The frequency-selective circuit R3C1R4C2 is called the Wien bridge, from which And received Name generator this type. This bridge consists of from series -connected differentiating circuit R4C2 and integrating circuit R3C1. As is known For generation signal bridge Guilt must provide null phase signal shift. This provided equality constant time integrating chains R3C1 and the differentiating circuit R4C2:

$$R4C2 = R3C1$$

Then frequency, at which will shift phases equal zero, is determined the following expression:

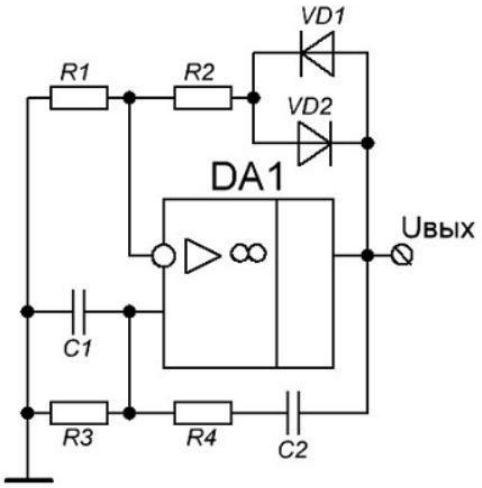
$$f = \frac{1}{2\pi\sqrt{R3C1R4C2}}$$
$$R3 = R4 = R$$
$$C1 = C2 = C$$
$$f = \frac{1}{2\pi RC} \quad (1)$$

At this condition coefficient transmissions chains POS will equal 1/3. That's why for that to compensate given condition coefficient transmissions chains OOS must be equal to 3, that is:

$$\beta_{ooc} = \frac{R1}{R1+R2} = \frac{1}{3}$$
$$R2 = 2 * R1 \quad (2)$$

If β < 1/3 That emerged fluctuations will be with strong distortions, A V case β > 1/3, even if oscillations occur, their amplitude will gradually decrease and eventually become zero. Therefore, various automatic amplitude stabilization systems are used to stabilize the operation of the Wien generator.

This system works So to influence on coefficient transmissions circuits and stabilize oscillations at a given frequency with small distortions. The basis of amplitude stabilization systems is the property of nonlinear elements under the influence of voltage. change your own internally resistance. One from protozoa schemes stabilization contains two semiconductor diodes included in the feedback circuit, see Figure 2



Drawing 2 - Scheme generator Guilt on OU With system automatic stabilization am plitudy

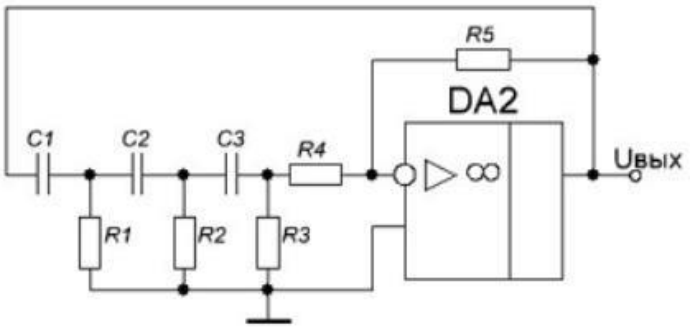
IN this scheme sequentially With resistor reverse connections R2 included two diode - VD1VD2 in an antiparallel circuit, which ensures stabilization of the amplitude of the positive and negative half-waves of the sinusoidal signal.

If V scheme Not provided devices automatic stabilization, stable operation of the generator will be impossible. In this case, after the occurrence of oscillations amplitude weekend voltage will start constantly increase, And This will lead To

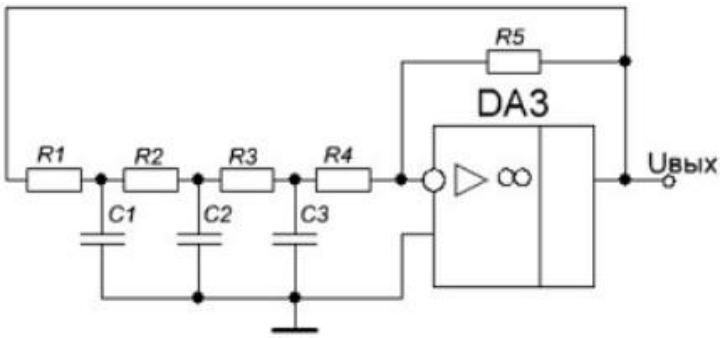
This means that the generator's active element (the operational amplifier) will enter saturation mode . As a result, the output voltage will differ from the harmonic voltage.

Generator sinusoidal fluctuations With phase-shifting RC circuits

More one view generator sinusoidal fluctuations is generator on phase-shifting chains. Schemes generator this type exists some varieties , they are based on ladder RC circuits, which provide a phase shift for the generated frequencies on 180°. WITH taking into account inverting amplifier, which Also provides a 180° signal phase shift, resulting in a total signal phase shift of 0°. The number of ladder chain links can be any, but not less than three.



Drawing 3 - RC generator chains With phase-shifting chain R- parallel



Drawing 4 - RC generator chains With phase-shifting chain "C- parallel"

Just like with the Wien bridge, ladder networks attenuate the signal, so the gain gains OU must compensate given weakening. To Not delve into conclusion calculated formulas I'll bring it main ratios V various types generators with sliding ladder chains.

Formulas For schemes on Figure 3:

$$R1 = R2 = R3 = R4 = R$$

$$C1 = C2 = C3 = C$$

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

$$\frac{R5}{R4} \geq 29$$

Formulas For schemes on Figure 4:

$$R1 = R2 = R3 = R4 = R$$

$$C1 = C2 = C3 = C$$

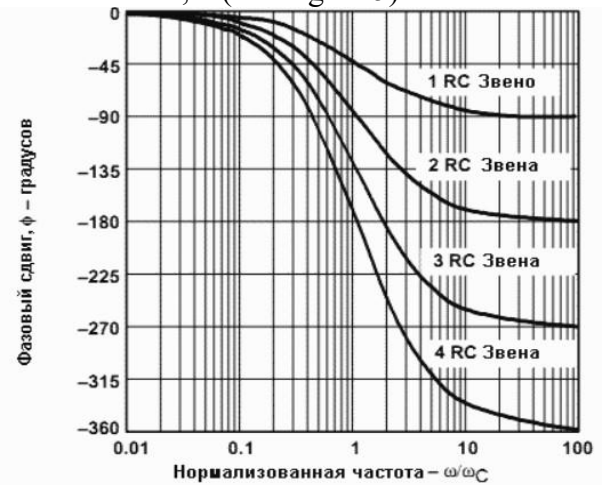
$$f = \frac{\sqrt{6}}{2\pi RC}$$

$$\frac{R5}{R4} \geq 29$$

So same How And V generator Guilt basic problem is security Amplitude stability . The solution to this problem is to use an automatic amplitude stabilization circuit by introducing nonlinear resistances into the feedback circuit of the op amp. The simplest such amplitude stabilizer is an assembly of two antiparallel semiconductor diodes.

Oscillators are dependent on the phase shift introduced by passive components because this phase shift accurate And almost without drift. Phase shift, introduced active components, reduced To minimum, because He depends from temperatures, has wide initial tolerance, and depends on the types of active elements. The amplifiers are selected in such a way in this way, What would They contributed minimum phase shift on frequency fluctuations. These factors limit the operating range of operational amplifier oscillators to relatively low frequencies.

The phase shift determines working oscillation frequency, since the circuit will generate oscillations at any frequency at which a phase shift of 180° accumulates. Sensitivity phases To frequency, dφ/dω, defines stability frequencies. When buffered RC links (the buffer on the operational amplifier provides high input and low weekend resistance) included cascading, That phase shift multiplies on number of links, n (see Figure 5).



Drawing 5 - Shift phases RC links

In the region where the phase shift is 180°, the generation frequency is very sensitive To shift phases. Like this in this way, because of tough requirements To frequency It is necessary that the phase shift dφ be varied within extremely narrow limits so that the changes in frequency dφ are insignificant with a phase shift of 180°.

From drawing 5 it is visible, What Although two sequentially united RC link V of - course in the end provide phase shift almost 180°, magnitude dφ/dω on frequency generation unacceptable small. Hence, generator on basis two sequentially with connected RC circuits will have poor frequency stability.

Three identical RC filter, included consistently, have much a larger dφ/dω ratio (see Figure 5), which results in improved frequency stability generator. Addition fourth RC link allows create generator With

excellent dφ/dω ratio (see Figure 5), thus providing the most frequency stable RC oscillator circuit.

Four-link RC chains contain maximum number links, which use , That's why What V one body microcircuits contains four OU, And four-stage generator gives four sinusoids, shifted By phase Friend relatively each other at 45°.

Content practical work, performed students **Description of laboratory equipment:**

– PC for each student;

– program editor schematic modeling "ElectronicsWorkbench" (EWB) version no lower than 5.12 or NIMultisim Education version;

– an application for mathematical and engineering calculations, version not lower than 15.0.

Requirements security at execution works:

1) TO conducting laboratory works allowed students, past required safety briefings.

2) Turning on laboratory installations (computers) is being carried out only With once the teacher's decision.

3) When conducting laboratory work, it is not permitted to use devices or equipment that are not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) At occurrence emergency situations necessary immediately turn off equipment from the power supply network, inform the teacher about this and act according to his instructions .

6) At fire equipment his necessary immediately de-energize, report this to the teacher, take measures to eliminate the fire and act according to the teacher's instructions.

7) By ending work With laboratory equipment (computers) his must be switched off in the established order.

Initial data for research

Options tasks For individual modeling schemes auto generators and the research conducted are presented in Tables 1 and 2.

Table 1 - Options tasks for research.

Option number	f, Hz	Variant No.	f, Hz
1	100	11	300
2	120	12	320
3	140	13	340
4	160	14	360
5	180	15	380
6	200	16	400
7	220	17	420
8	240	18	440
9	260	19	460
10	280	20	480

Table 2 - Options tasks for research.

Option number	C, nF	Option number	C, nF
1	15	11	20
2	15.5	12	20,5
3	16	13	21
4	16,5	14	21,5
5	17	15	22

6	17,5	16	22,5
7	18	17	23
8	18,5	18	23,5
9	19	19	24
10	19,5	20	24,5

Tasks to be completed during practical work

Tasks basic level:

1) Conduct study principles work, parameters And characteristics autogenator on an op-amp with a Wien bridge.

2) Conduct study parameters RC generator chains With phase-shifting chain “R-parallel”.

Tasks increased level:

3) Conduct study parameters RC generator chains With phase-shifting chain “C-parallel”.

Order execution work

Exercise 1. Conduct study principles work, parameters And characteristics of an op-amp oscillator with a Wien bridge.

statement :

Perform mathematical and circuit simulation of the Wien bridge generator on an op amp for a given frequency (see Table 1).

IN task necessary define next parameters autogenerator Wien bridge on an operational amplifier:

– resistance And capacity elements chains, on which Maybe self-excitation;
– relative And absolute error quasi-resonant frequencies;
– time offensive established process;
– quality factor chains By expected appearance frequency response And Phase-frequency response.

For conducting research scheme should have measuring instruments :

– oscilloscope For analysis forms weekend voltage And measurements time its establishment;
– Bode plotter for plotting amplitude-frequency and phase-frequency characteristics (AFC and PFC).

Order execution tasks

1) Calculate values of the elements of a given circuit and simulate the circuit. To do this, perform the following procedures:

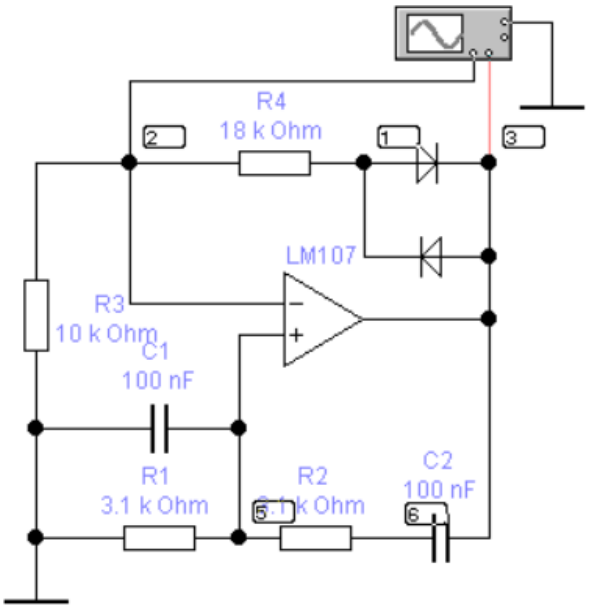
1.1) Calculate meaning denominations resistance And capacity V striped filter, using formula (1), the frequency is set according to the option in table 1.

$$R1=R2=R$$
$$C1=C2=C$$
$$f := \frac{1}{2\pi R \cdot C}$$

1.2) Define meaning denomination resistance V chains reverse negative relationship, taking into account formula (2).

$$\beta_{ooc} := \frac{R3}{R3 + R4} = \frac{1}{3}$$
$$R4 := 2 \cdot R3$$

1.3) Assemble the basic electrical circuit diagram of the Wien bridge generator using an op-amp in the EWB program, as shown in Fig. 1. Set the capacitor and resistance values calculated in paragraphs 1.1 and 1.2 on the diagram.

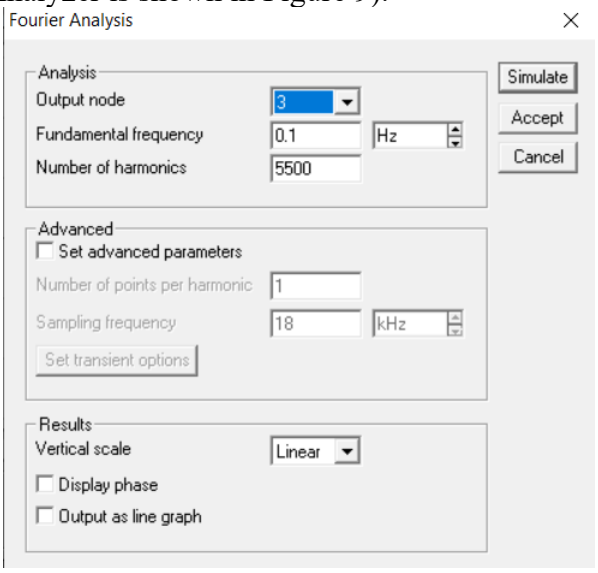


Drawing 6 - Scheme For research parameters And characteristics bridge generator Wines at the OU

1.4) Check performance schemes, using oscillogram weekend signal and Fourier analyzer, make sure that the obtained frequency practically coincides with the frequency specified in the option:

A) WITH help oscillograms define period weekend signal, And calculate its frequency (an example of operation is shown in Figure 8);

B) Using a Fourier analyzer, find out what the frequency of the output signal is (for this necessary find out number node, connected To exit oscillograms: Cir-curt - SchematicOptions - Shownodes; then execute: Analysis - Fourier - choose required node – pulse repetition step – number of harmonics – Simulate) An example of the setup is shown in Figure 7. (An example of the operation of the Fourier Analyzer is shown in Figure 9).



Drawing 7 – Using a Fourier Analyzer

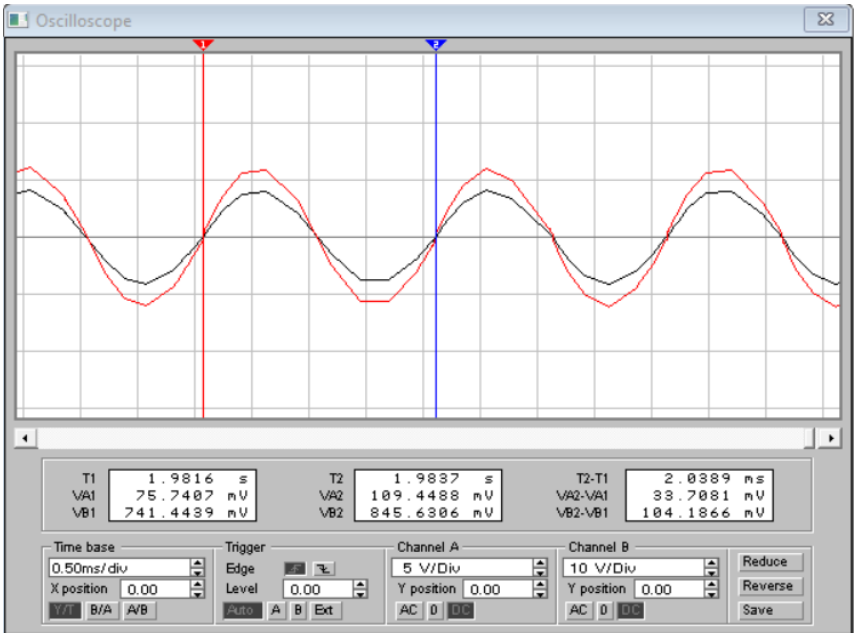
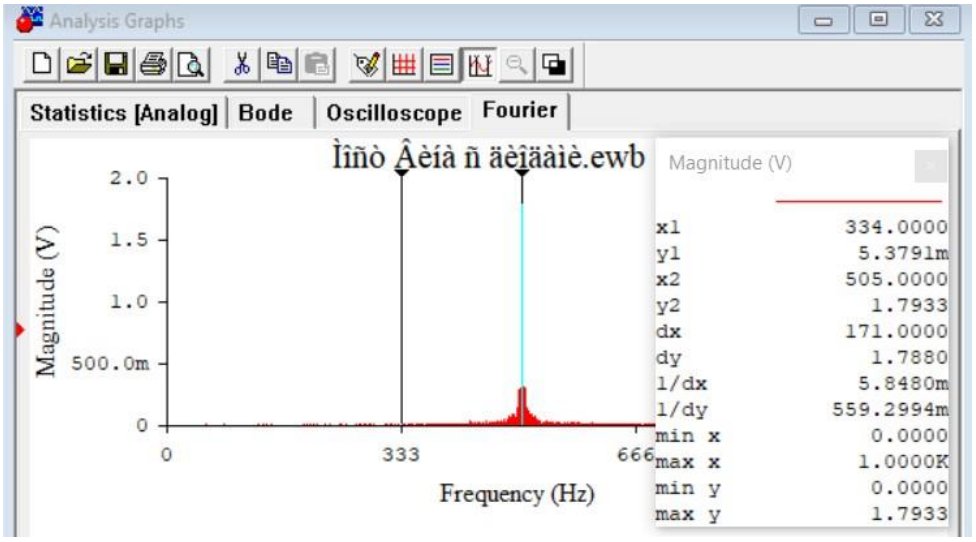


Figure 8 – Oscillogram schemes



Drawing 9 - Using a Fourier Analyzer

1.5) Calculate the relative and absolute error of the difference in the error obtained using a Fourier analyzer and an oscilloscope relative to a given frequency using the formulas:

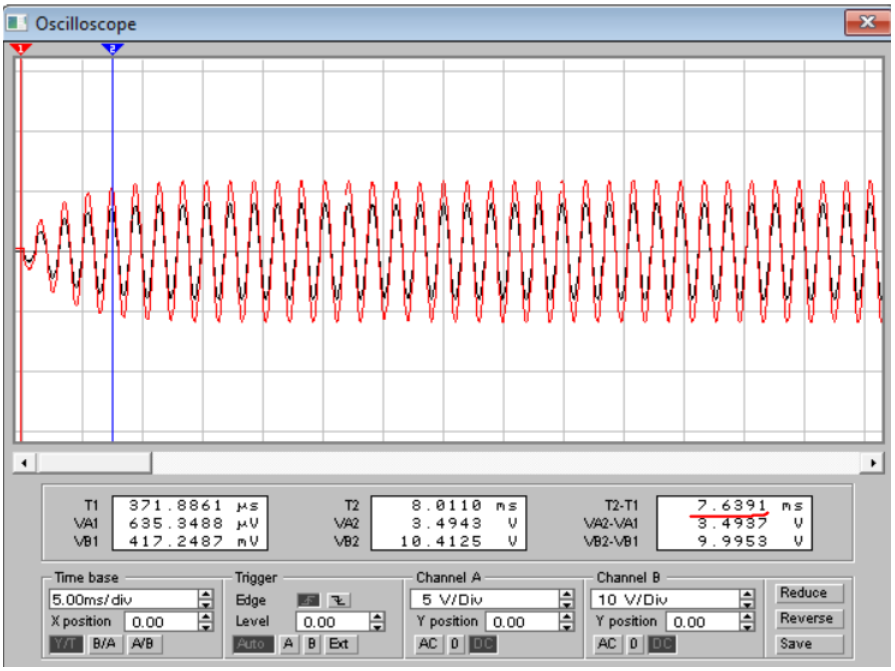
Absolute error:

$$\Delta f := f_{изм} - f_{зад}$$

Relative error:

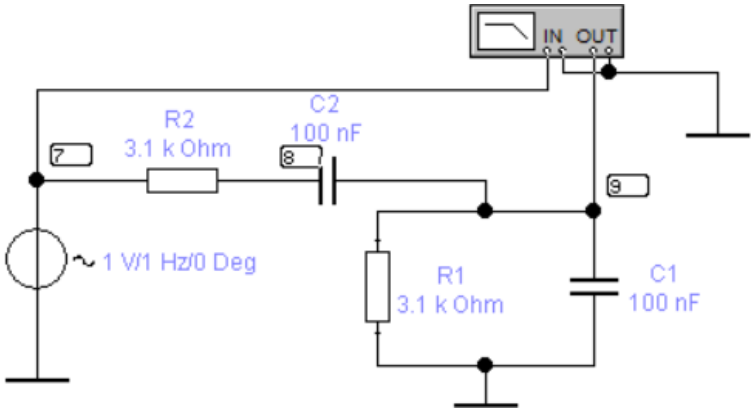
$$\delta F := \frac{\Delta f}{f_{зад}}$$

1.6) Determine the duration of the steady-state process using the circuit oscilloscope trace. To do this, set the first cursor of the oscilloscope to approximately **0.1U** $_{out}$, and the second cursor to approximately size, equal to **0.9U** $_{out}$. C using the oscilloscope's measuring window, determine **the set** $_{point}$ = T2 – T1. An example is shown in Figure 10.



Drawing 10 - Duration steady-state process

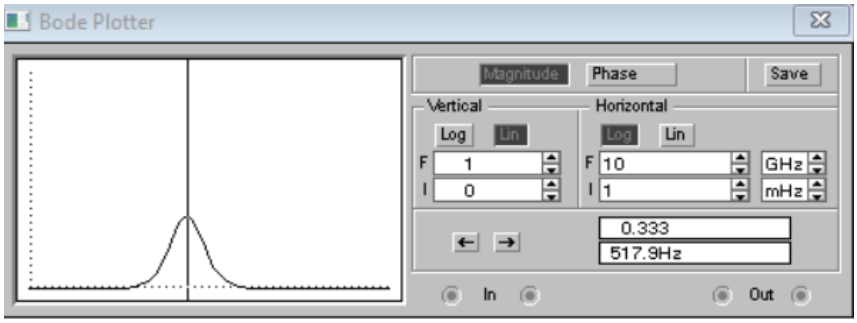
1.7) To investigate the frequency response and phase response at a quasi-resonant frequency, for this it is necessary to collect chain presented on drawing 11. Install on scheme values capacitors and resistances calculated in paragraph 1.1.



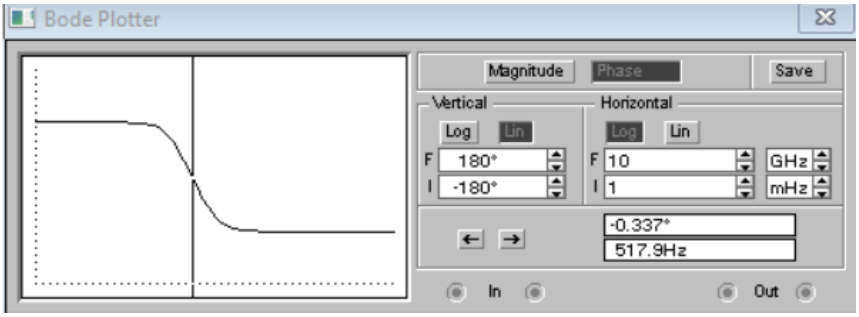
Drawing 11 - Scheme autogenerator Guilt For research frequency response and phase response

1.8) Set up the graph plotter (Bode plotter) in the frequency response meter mode, to do this, turn on button Magnitude, V frame Vertical choose linear scale By axes amplitudes, and set the upper and lower threshold values F=0.5 or 1, I=0, in the Horizontal frame you select logarithmic scale By axes frequencies, And install values top And lower threshold F=10 GHz, I=1 mHz. An example is shown in Figure 12.

1.9) Set up the graph plotter (Bode plotter) in the phase response meter mode, to do this, turn on the Phase button, in the Vertical frame, select the linear scale along the amplitude axis, and set the upper and lower threshold values F=180, I=-180, in In the Horizontal frame, select logarithmic scale By axes frequencies, And install values top And lower threshold F=10 GHz, I=1 mHz. An example is shown in Figure 13.



Drawing 12 - frequency response schemes



Drawing 13 - phase response schemes

1.10) Received oscillograms And graphs at research analyzer Present the Fourier transform in the report. Draw conclusions based on the results of the study.

2) Research stability weekend signal autogenerator at changing the circuit parameters. To do this, perform the following procedures:

2.1) Return To scheme For research, presented on rice. 6

2.2) At first increase, A then decrease resistance resistor V OOS (resistor) R4) on 5% from original values. Get oscillograms input and output signals.

2.3) At first increase, A then decrease resistance resistor R3 on 5% from the original value. Obtain oscillograms of the input and output signals.

2.4) At first increase, A then decrease resistance resistors bridge Wines (resistors) R1 And R2) on 0.5 COM from original values. Get oscillograms input and output signals.

2.5) First, increase and then decrease the capacitance of the Wien bridge capacitors (capacitors C1 and C2) by 20 nF from the original value. Obtain oscillograms of the input and output signals.

2.6) Received oscillograms introduce in the report.

2.7) Do conclusions By results conducted research.

<u>Exercise 2.</u> Conduct study parameters RC generator chains With phase -shifting chain "R-parallel".

statement :

Perform mathematical and circuit simulation of the RC generator circuit With phase-shifting chain R-parallel For given frequencies (cm. table 1).

The task requires determining the following parameters of the RC generator circuit with the phase-shifting circuit “R-parallel”:

– resistance And capacity elements chains, on which Maybe self-excitation;

– relative And absolute error quasi-resonant frequencies;

– time offensive established process;

– shift phases, which carries out phase-shifting chain.

For conducting research scheme should have measuring instruments :

– oscilloscope For analysis forms weekend voltage And measurements time its establishment;

– Bode plotter for plotting amplitude-frequency and phase-frequency characteristics (AFC and PFC).

Order execution tasks 2

1) Calculate values of the elements of a given circuit and simulate the circuit. To do this, perform the following procedures:

1.1) Calculate the value of the resistance and capacitance for the phase-shifting circuit using formula (1), the frequency is specified according to the option in Table 1.

$$R1=R2=R3=R4=R$$

$$C1=C2=C3=C$$

$$f := \frac{1}{2\pi\sqrt{6}\cdot R\cdot C}$$

1.2) Define meaning denomination resistance V chains reverse negative relationship, taking into account formula (2).

$$\frac{R5}{R4} \geq 29$$

1.3) Assemble the basic electrical circuit of the RC generator in the EWB program chains With phase-shifting chain "R-parallel" How shown on rice. 14. Set the values of capacitors and resistances calculated in points 1.1 and 1.2 on the diagram.

1.4) Connect V chain resistance loads, How shown on drawing 14, with a nominal value equal to the output resistance of the operational amplifier.

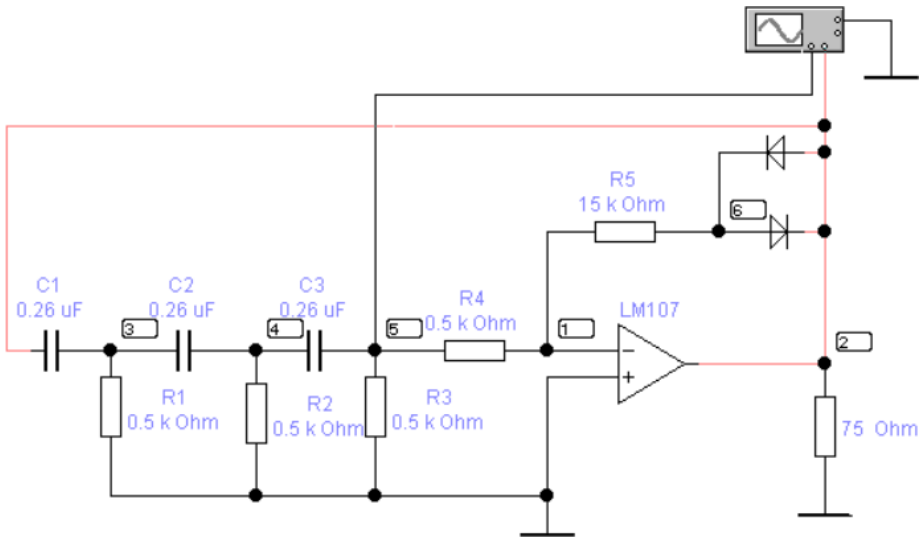
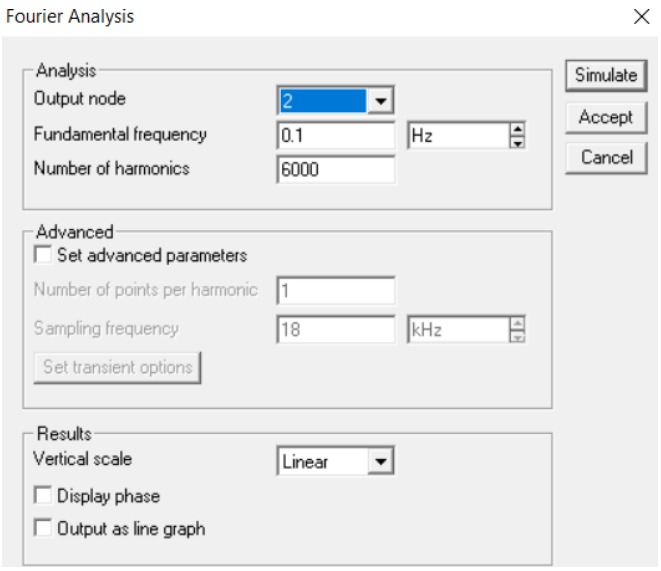


Figure 14 – Schematic diagram for studying the parameters and characteristics of an RC generator chains With phase-shifting chain R-parallel

1.5) Check performance schemes, using oscillogram weekend signal and Fourier analyzer, make sure that the obtained frequency practically coincides with the frequency specified in the option:

A) WITH help oscillograms define period weekend signal, And calculate its frequency (an example of operation is shown in Figure 16);

B) Using a Fourier analyzer, find out what the frequency of the output signal is (for this necessary find out number node, connected To exit oscillograms: Cir-curt - SchematicOptions - Shownodes; then execute: Analysis - Fourier - choose required node – pulse sequence step – number of harmonics – Simulate) An example of the setup is shown in Figure 15. (An example of the operation of the Fourier Analyzer is shown in Figure 17).



Drawing 15 - Usage Fourier analyzer

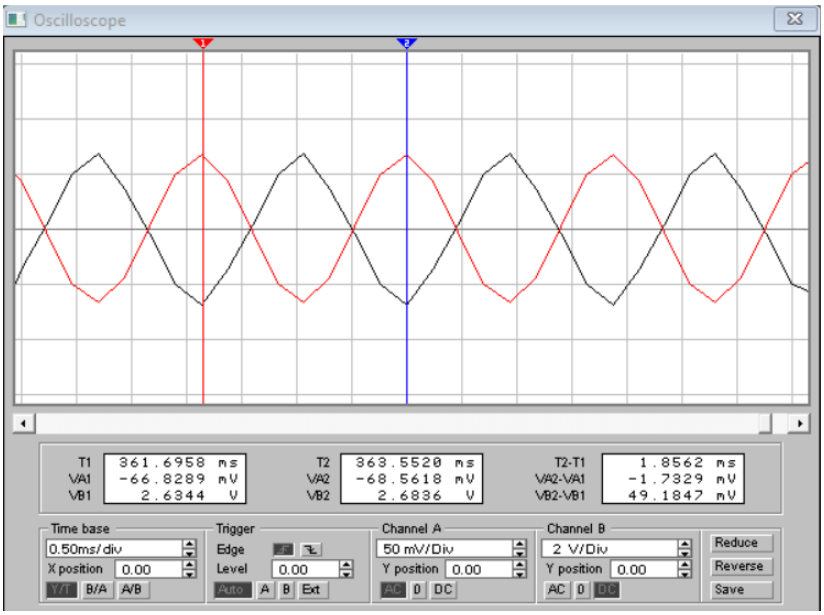
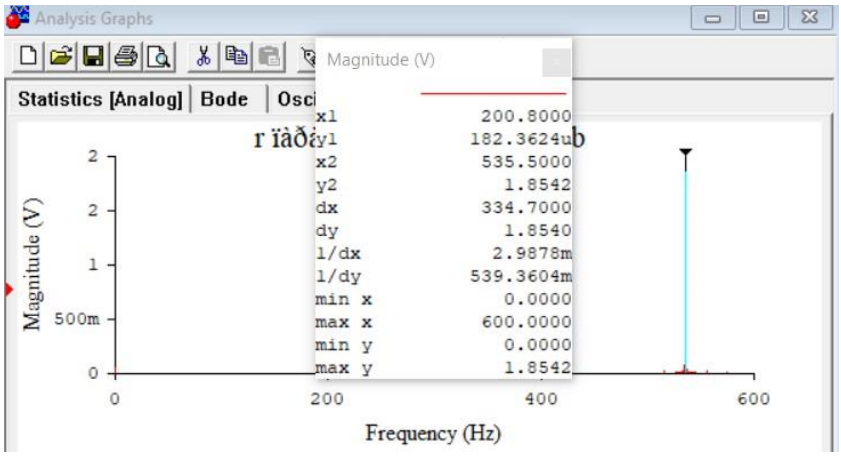


Figure 16 – Oscillogram schemes



Drawing 17 - Usage Fourier analyzer

1.6) Calculate the relative and absolute error of the difference in the error obtained using a Fourier analyzer and an oscilloscope relative to a given frequency using the formulas:

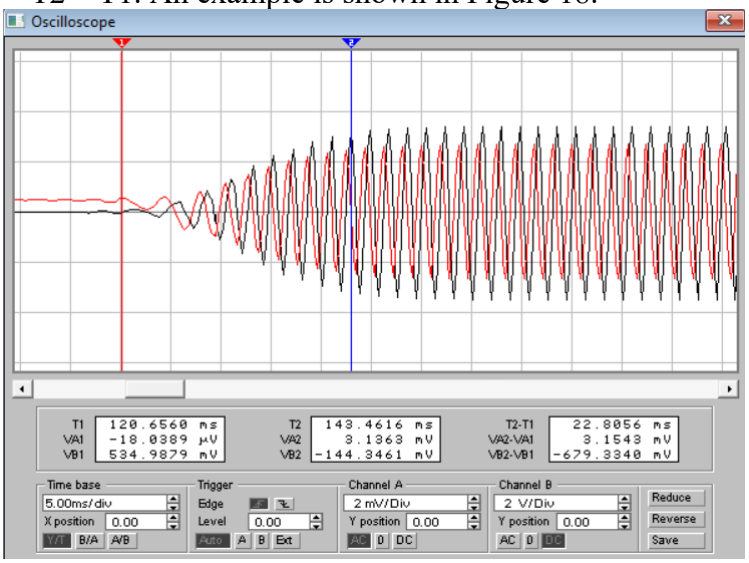
Absolute error:

$$\Delta f := f_{изм} - f_{зад}$$

Relative error:

$$\delta F := \frac{\Delta f}{f_{зад}}$$

1.7) Define duration established process, using oscillogram of the circuit. To do this, set the first cursor of the oscilloscope to a value approximately equal to **0.1U** $_{out}$, A second cursor approximately on size, equal **0.9U** $_{out}$. WITH help windows determine the **t** $_{setting\ of\ the\ oscilloscope}$ measuring window = T2 – T1. An example is shown in Figure 18.



Drawing 18 - Duration steady-state process

1.8) To investigate the frequency response and phase response at a quasi-resonant frequency, for this it is necessary to collect chain presented on drawing 19. Install on scheme values capacitors and resistances calculated in paragraph 1.1.

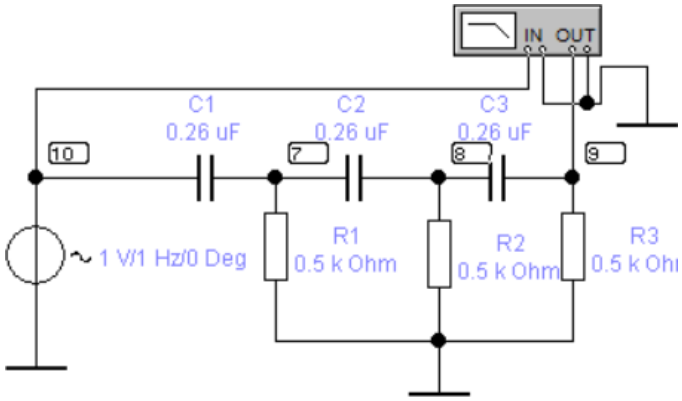
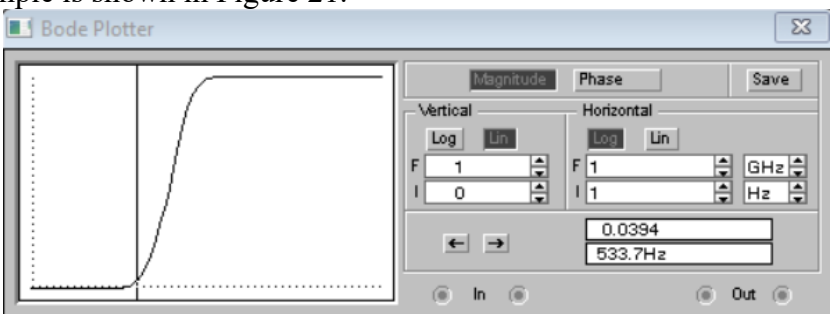


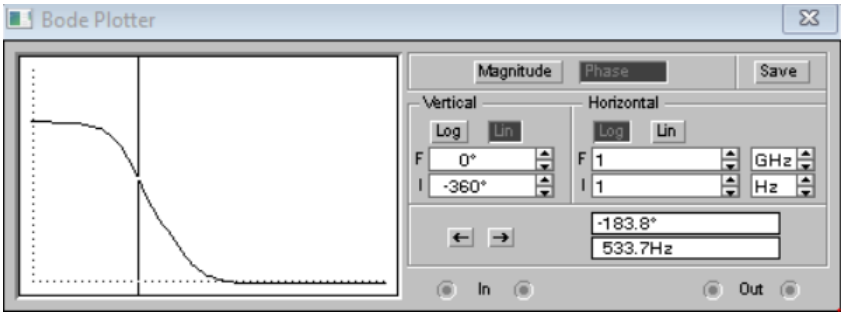
Figure 19 – Schematic diagram of an RC generator circuit with a phase-shifting circuit "R-parallel" for studying the frequency response and phase response

1.9) Set up the graph plotter (Bode plotter) in the frequency response meter mode, to do this, turn on button Magnitude, V frame Vertical choose linear scale By axes amplitudes, and set the upper and lower threshold values F=0.5 or 1, I=0, in the Horizontal frame you select logarithmic scale By axes frequencies, And install values top And lower threshold F=1 MHz, I=1 Hz. An example is shown in Figure 20.

1.10) Set up the graph plotter (Bode plotter) in the phase response meter mode, to do this, turn on the Phase button, in the Vertical frame, select the linear scale along the amplitude axis, and set the upper and lower threshold values F=0, I=-360, in the Horizontal frame, select the logarithmic scale scale By axes frequencies, And install values top And lower threshold F=1 MHz, I=1 Hz. An example is shown in Figure 21.



Drawing 20 - frequency response schemes



Drawing 21 - phase response schemes

1.11) Bring cursor Bode plotter V mode phase response on phase, equal -180 degrees, and determine the frequency

1.12) Translate Bode plotter V mode frequency response And measure on this frequency transfer coefficient, for this you need to use the formula:

$$\beta_{ooc} := \frac{1}{A}$$

Where A - amplitude at received frequency

1.13) Define With help cursors oscilloscope difference phases between output and input signals, for example, as in Figure 22, measure the time shift between the signals □ τ = T2 – T1, and then determine the phase shift using the formula: $\Delta\varphi = \Delta \mathbf{t} \cdot \mathbf{f} \cdot \mathbf{360}$ [Deg].

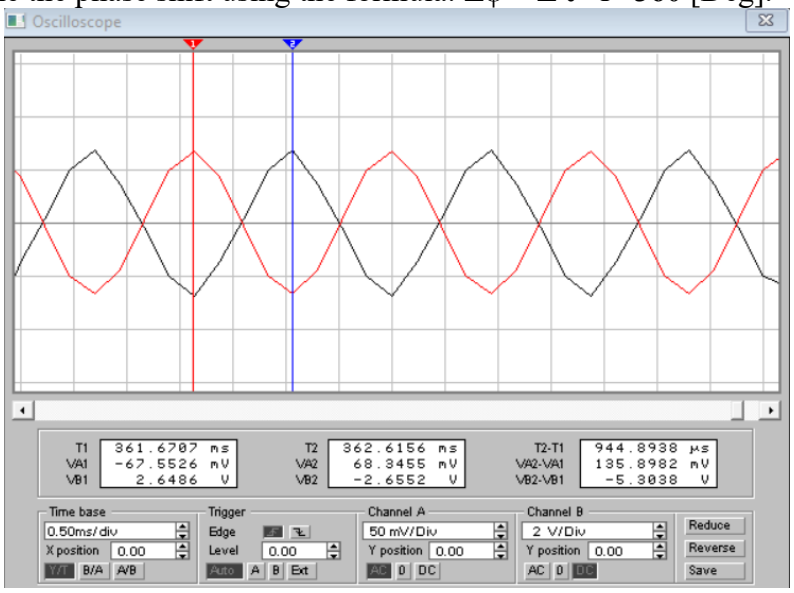


Figure 22 – Oscillogram schemes

1.14) Disable from chains resistance loads. Find out what way the oscillogram of the circuit changes .

1.15) Received oscillograms And graphs at research analyzer Present the Fourier transform in the report. Draw conclusions based on the results of the study.

2) Research stability weekend signal, at change circuit parameters. To do this, perform the following procedures:

2.1) Return To scheme For research, presented on rice. 14

2.2) At first increase, A then decrease resistance resistor V OOS (resistor R5) on 15% from original values. Get oscillograms input And output signals.

2.3) First, increase and then decrease the resistance of resistor R4 by half its original value. Obtain oscillograms of the input and output signals.

2.4) First increase and then decrease the resistance of the phase- shifting resistors. chains (resistors R1, R2 And R3) V 2 times from original values. Get oscillograms of input and output signals.

2.5) At first increase, A then decrease capacity capacitors phase-shifting circuit (capacitors C1, C2 and C3) by 5 times the original value. Obtain oscillograms of the input and output signals.

2.6) Received oscillograms introduce in the report.

2.7) Do conclusions By results conducted research.

<u>Task 3 (advanced level).</u> Conduct a study of the parameters of an RC generator circuit with a phase-shifting "C-parallel" circuit.

statement :

Produce circuit design modeling RC generator chains With phase- shifting circuit "C-parallel" for a given capacitance of capacitors (see Table 2).

The task requires determining the following parameters of the RC generator circuit with the phase-shifting circuit “R-parallel”:

– quasi-resonant frequency, on which self-excitation occurs ;

– relative And absolute error quasi-resonant frequencies;

– time offensive established process;

– shift phases, which carries out phase-shifting chain.

For conducting research scheme should have measuring instruments :

– oscilloscope For analysis forms weekend voltage And measurements time its establishment;

– Bode plotter for plotting amplitude-frequency and phase-frequency characteristics (AFC and PFC).

Order execution tasks 3

1) Simulation of an RC generator circuit with a C-parallel phase-shifting circuit. To do this, perform the following procedures:

1.1) Assemble the basic electrical circuit of the RC generator circuit with the “C-parallel” phase-shifting circuit in the EWB program, as shown in Fig. 23. In this case, set the resistance values as in Fig. 23, and the capacitance for the phase-shifting circuit is specified according to the option in Table 2.

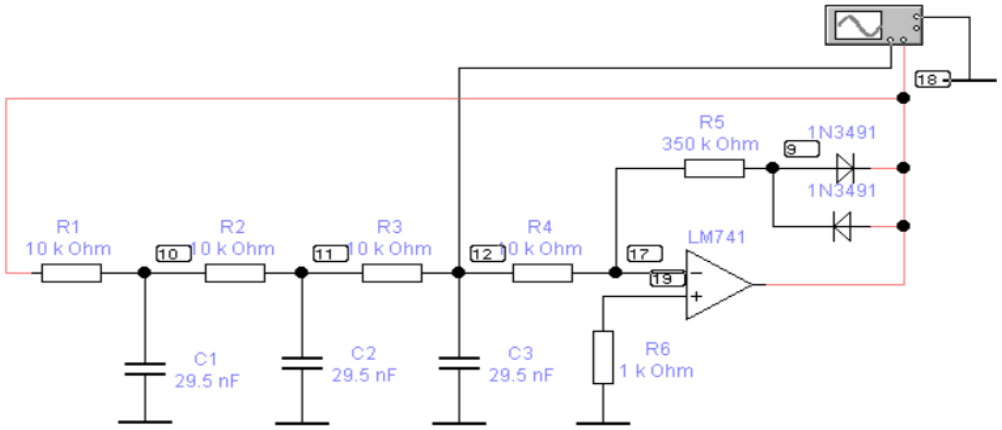


Figure 23 – Schematic diagram for studying the parameters and characteristics of an RC generator circuit with a phase-shifting "C-parallel" circuit

1.2) Calculate the value of the quasi-resonant frequency at which self-excitation will occur:

$$R1=R2=R3=R4=R$$

$$C1=C2=C3=C$$

$$f := \frac{\sqrt{6}}{2\pi \cdot R \cdot C}$$

1.3) Check performance schemes, using oscillogram weekend signal and Fourier analyzer, make sure that the obtained frequency is almost the same as the frequency calculated in point 1.2.

1.4) Calculate the relative and absolute error of the difference in the obtained error using a Fourier analyzer and an oscilloscope relative to the calculated frequency.

1.5) Determine the duration of the steady-state process using the oscillogram of the circuit.

1.6) To investigate the frequency response and phase response at a quasi-resonant frequency, for this it is necessary to collect chain presented on drawing 24. Install on scheme values capacitors and resistors that were used in the previous circuit.

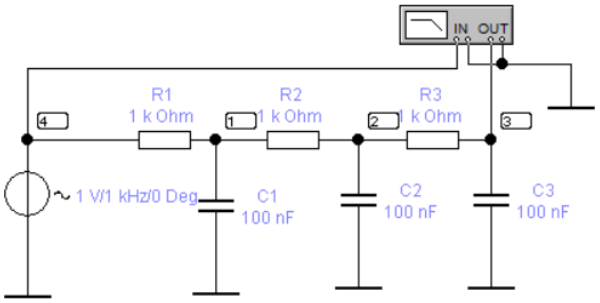


Figure 24 – Schematic diagram of an RC generator circuit with a phase-shifting circuit "C-parallel" for studying the frequency response and phase response

1.7) Using frequency response schemes, calculate coefficient autogenerator transmission

1.8) Define With help oscillogram difference phases between weekends And input signal.

1.9) The obtained oscillograms and Present the graphs obtained from the Fourier analyzer analysis in the report. Draw conclusions based on the results of the study.

2) Research stability weekend signal, at change circuit parameters. To do this, perform the following procedures:

2.1) Return To scheme For research, presented on rice. 23

2.2) At first increase, A then decrease capacity capacitors phase- shifting chains (capacitors C1, C2 And C3) V on 1 nF from original values. Get Oscillograms of the input and output signals and calculate the resulting frequency. Study the frequency spectrum using a Fourier analyzer.

2.3) At first increase, A then decrease capacity capacitors phase- shifting chains (capacitors C1, C2 And C3) V on 5 nF from original values. Get Oscillograms of the input and output signals and calculate the resulting frequency. Study the frequency spectrum using a Fourier analyzer.

2.4) Present the resulting oscillograms and graphs from the Fourier analyzer in a report. Draw conclusions based on the results of the study.

<u>Exercise 4. (For independent work)</u> Design results research in the form of a laboratory report and defend it.

1.1) IN report By laboratory work display:

– topic And target work, tasks For research And brief order their execution;

– the basic electrical circuits of the studied autogenerators on the op amp, modeled in the schematic modeling editor;

– oscillograms input and output signals;

– graphs frequency response With results measurements frequency parameters;

– conclusions By results execution tasks And V in general By work done .

1.2) Defend a report on the completed laboratory work by completing an individual - assignment specified by the teacher, within the framework of the research conducted.

Control questions For preparation To protection:

1. Please specify from what kind parts must consist generator sinusoidal fluctuations
2. List conditions of self-excitation of autogenerators
3. For what are used diodes V chains OOS of autogenerators?
4. How are phase balance conditions met in auto-oscillators with phase-shifting circuits and a Wien bridge?
5. On what kind frequencies found applications auto generators sinusoidal oscillation-niy
6. What by yourself represent frequency and phase characteristics of autogenerators
7. Please explain appointments reverse connections V auto generators

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 10

Subject: **STUDY BASICS BOOLEAN LOGIC. MINIMIZATION LOGICAL FUNCTIONS**

Time – 2 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– to conduct research into the fundamentals of Boolean algebra and basic logic elements based on their circuit models,

– realize synthesis logical devices With using universal packages of computer applications;

– collection and analysis of information to generate initial data for the design of digital devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program schematic editor Electronics Workbench (EWB) simulation , version 5.12 or later, or NI Multisim Education version;

– application for mathematical and engineering calculations Mathcad Professional version not lower than 15.0;

– electronic methodological development By laboratory work.

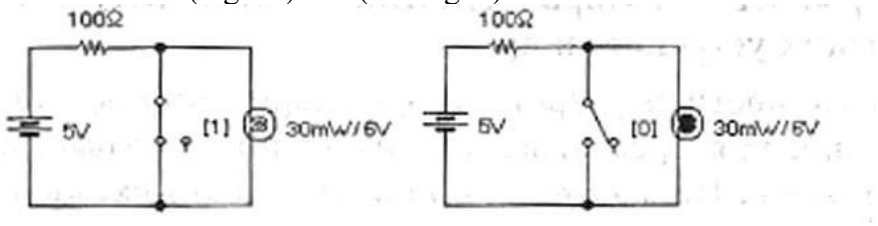
STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study basics Boolean algebra With help circuit design fashion-lei.	50 min
2. Minimization logical functions.	25 min
Final Part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

It is known, What ***mathematical basis digital computing devices is binary arithmetic*** , which uses only two numbers - 0 and 1. The choice of binary systems numeration was dictated requirements simplicity technical implementation the most difficult tasks With using total one basic element – ***electronic key, which has two conditions*** : included (closed) or turned off (open). IN computer the first closed state of the key is taken as a conditional (logical) zero, then the second open state will reflect a conditional (logical) one (see Fig. 1).



a) *b)*

Rice. 1 - Electromechanical imitators: A) logical units, b) zero in inverse mode

When key 1 is pressed, the indicator goes out, recording the state 0, and, conversely, when the key is released, the indicator lights up, recording – 1. The circuits shown in Fig. 1, according to the output signal (the state of the indicator lamps), are the opposite or inverse of the state of the key, therefore such keys are called inverters.

Because digital systems contain a huge number of keys (in just one microprocessor their some millions) And They Not can report Friend to a friend O In their state, the lights flash, and ***electrical voltage signals are used to exchange information*** . In this case, the switches are usually used in inverse mode.

The theoretical basis for the use of logical elements in the creation of various combinational digital devices (adders, multiplexers and demultiplexers , encoders and decoders, digital comparators etc.) ***is Boolean an algebra*** that operates on binary variables, the actions on which are performed according to the rules of logical operations.

Protozoa logical there are three operations :

1) ***Negation*** (inversion, operation NOT). Operation denials is being carried out over one variable and is characterized by the following properties: function Y = 1 with argument X – 0 and Y = 0, If X = 1. It is designated negation feature over variable, With which the operation is performed: $Y = \overline{X}$ (y is not equal to x). In the Elec tronics circuit simulation program Workbench (EWB) negation (inversion) is designated How Y = X ' (further inversion will be designated in exactly this way).

2) ***Logical multiplication*** (conjunction, AND operation). The operation of logical multiplication (conjunction) $Y = X_1 \cdot X_2$ for two variables is expressed as follows: 0 0 = 0; $0 \cdot 1 = 0$; $1 \cdot 0 = 0$; $1 \cdot 1 = 1$, i.e., a zero value of at least one of the arguments ensures zero result operations. Operation Maybe be widespread And on more number variables .

3) ***Logical addition*** (disjunction, operation OR). Operation logical additions (disjunctions) $Y = X_1 \vee X_2$ or $Y = X_1 + X_2$ two variables characterized by the following properties: 0+0 = 0; 0+1 = 1; 1+0 = 1: 1+1 = 1, i.e. the unit value of at least one of the arguments ensures a single result of the operation. Disjunction, like conjunction, can be performed with many variables.

More complex logical transformations Can bring together To specified operations .

Totality various values variables they call set . Boolean a function ***of n*** arguments can have up to $N = 2^n$ sets. Since the function takes only two values , the total number Boolean functions ***of n*** arguments equals $2^N = 2^k$, where $k = 2^n$. Thus, the function one argument can have four values: Y = X ; Y = X ' ;Y = 1 (constant 1); Y = 0 (constant 0).

Two arguments already give 16 function values, of which, in addition to the three mentioned above, five more are used in practice:

1) ***EXCLUSIVE OR*** , those. $Y = X_1 \oplus X_2$ (0+0 = 0; 0+1 = 1; 1+0 = 1; 1+1 = 0), By to another Can name function disparity.

2) ***OR-NOT*** $Y = (X_1 + X_2)'$, this operation otherwise called Pierce arrow (0+0 = 1; 0+1 = 0; 1+0 = 0; 1+1 = 0), i.e. a unit value of at least one of the arguments ensures a zero result of the operation.

3) ***AND-NOT*** $Y = (X_1 \cdot X_2)'$, this operation otherwise it's called hatch Schaeffer ($0 \cdot 0 = 1$; $0 \cdot 1 = 1$; $1 \cdot 0 = 1$; $1 \cdot 1 = 0$), i.e. single value though would one from arguments provides zero result of the operation.

4) ***Ban By*** X_2 , those. $Y = X_1 \cdot X_2'$ ($0 \cdot 0 = 0$; $0 \cdot 1 = 0$; $1 \cdot 0 = 1$; $1 \cdot 1 = 0$), those. only at zero value of the argument X_2 and a single value of the argument X_1 ensures a single result of the operation.

5) ***Ban By X 1*** , those. $Y = X_1' \cdot X_2$ (0 0 = 0; 0 · 1 = 1; 1 · 0 = 0; 1 · 1 = 0), Here vice versa only when zero meaning argument X_1 And single meaning argument X_2 provided single result of the operation.

Boolean algebra is based on several axioms from which the basic laws are derived. For transformations With binary variables. Justification choice these the axioms are confirmed tables truth For considered operations. ***Each one axiom presented V two types*** , What flows out ***from principle duality (duality) logical operations*** , according to which the operations of conjunction and disjunction allow mutual substitution , If simultaneously change logical 1 on logical 0, A 0 on 1, sign "V" (or "+") to the " · " sign, and the " · " sign to "V" (or "+").

Axioms operations denials : 0 = 1; 1 = 0.

Axioms operations conjunctions And disjunctions :

1) $0 \cdot 1 = 1$;	(a);	$1 + 1 = 1$;	(b)
2) $1 \cdot 0 = 0 \cdot 1 = 0$;	(a);	$0+1=1+0=1$;	(b)
3) $1 \cdot 1 = 1$;	(a);	$0 + 0 = 0$.	(b)

Axiom 1b has no analogue in binary arithmetic, which 1+1=10 (here the numbers and signs have the usual arithmetic meaning).

Laws Boolean algebra flow out from axioms And Also have two forms expressions : for conjunction and disjunction . They are given here without proof. Their correctness easily check By tables truth or by way substitutions 0 And 1 instead of corresponding values of variables.

1) Commutative law:

$X_1 \cdot X_2 = X_2 \cdot X_1$; (a); $X_1 + X_2 = X_2 + X_1$. (b)

2) Associative law:

$X_1 (X_2 X_3) = (X_1 X_2) X_3 = X_1 X_2 X_3$; (a) $X_1 + (X_2 + X_3) = (X_1 + X_2) + X_3 = X_1 + X_2 + X_3$. (b)

3) Law repetitions (tautologies):

$XX = X$; (A) $X + X = X$. (b)

4) Law appeals:

If $X_1 = X_2$, That $X_1' = X_2'$.

5) Law of Double Inversion: Law $(X')' = X$.

6) zero sets:

$X\,0 = 0$; (A) $X + 0 = X$. (b)

7) Law universal sets:

$X\,1 = X$; (a) $X + 1 = 1$. (b)

8) Law additionality:

$X X' =$ 0; (a) $X + X' = 1$. (b)

9) Distribution law:

$X_1 + X_2 X_3 = (X_1 + X_2)(X_1 + X_3)$. (b)

10) Law absorption:

$X_1 (X_2 + X_3) = X_1 X_2$ (a) $X_1 X_2 + X_1 X_2' =$ (b)

11) X_1.

$+ X_1 X_3$; $X_1 + X_1 X_2 = X$ ***Law gluing:*** (b)

12) (a) $X_1 X_2 + X_1 X_2' =$

$_1$; X_1. (b)

Law inversions (law De Morgana):

$(X_1 + X_2)(X_1 + X_2') =$ (a) $(X_1 + X_2)' = X_1' X$

X_1; $_2'$

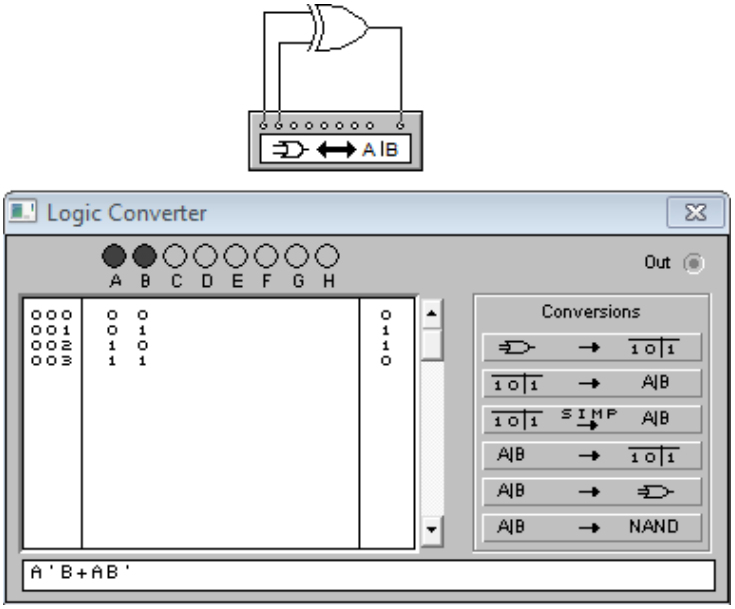
$(X_1 X_2)' = X_1' + X_2'$;

It is advisable to model logical circuits in the EWB program using logical converter (Logic Converter) . IN quality example on rice. 3, A when introduced scheme For research element EXCLUSIVE OR. Order connections of the studied element to the logical converter is obvious from

Fig. 3. It is also obvious that What at availability two entrances possible only four combinations input signals, What

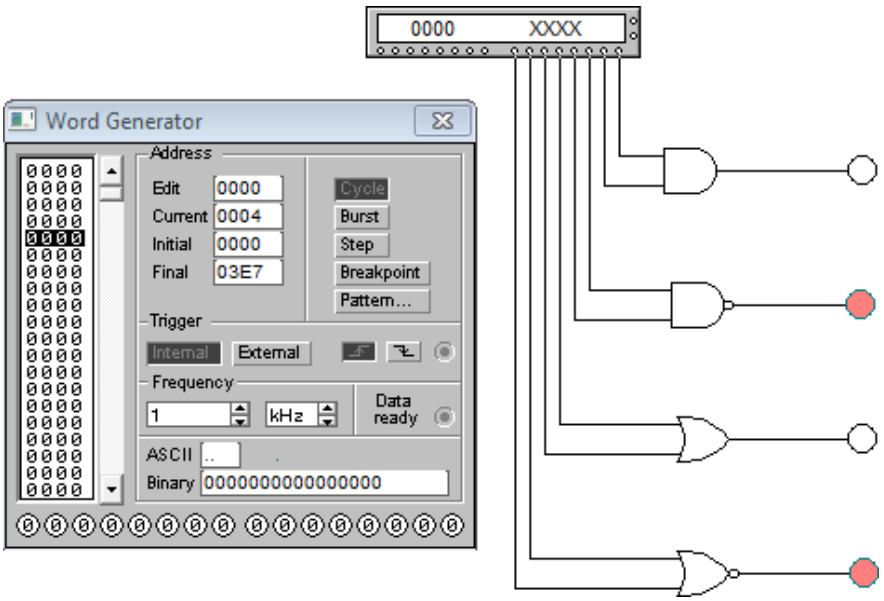
is displayed on the converter screen in the form of a truth table, which is generated after pressing the button  .

To obtain a Boolean expression for the element being studied, press the button  . This expression is shown on the additional display located V lower parts facial panels, V view two terms, corresponding output signal TRUE (signal logical units on exit OUT). Comparison The comparison of the obtained expression with the truth table convinces us that there are actually two such combinations, A ' B and AB ' , therefore the Boolean function has the form: A ' B + AB ' , where the + sign corresponds to the logical operation OR.



Rice. 3 - Study logical elements With help logical converter

IN quality example use generator words (Word Generator) for research of logical elements in Fig. 4 shows a circuit in which the corresponding binary combination is fed to the inputs of the AND, NAND, OR, NOR elements, A reaction elements indicated included on their exits logical probes .



Rice. 4 - Study logical elements With help generator words

With the help of a logic converter it is possible to carry out not only the analysis of logical devices, But And their synthesis . Let's say, What us required make up diagram And Boolean expression For logical element, at whom day off combination V table the truth value is not 0110, as in Fig. 3, but 1101. To make the necessary changes, we mark the symbol to be changed with the cursor in the OUT column, change it using the keyboard and then, moving along the column with the keys cursor control, change symbols as needed V others lines. After contributions everyone changes sequentially press on buttons given on rice. 5 (V right lower corner), And we get result, presented on Fig. 5.

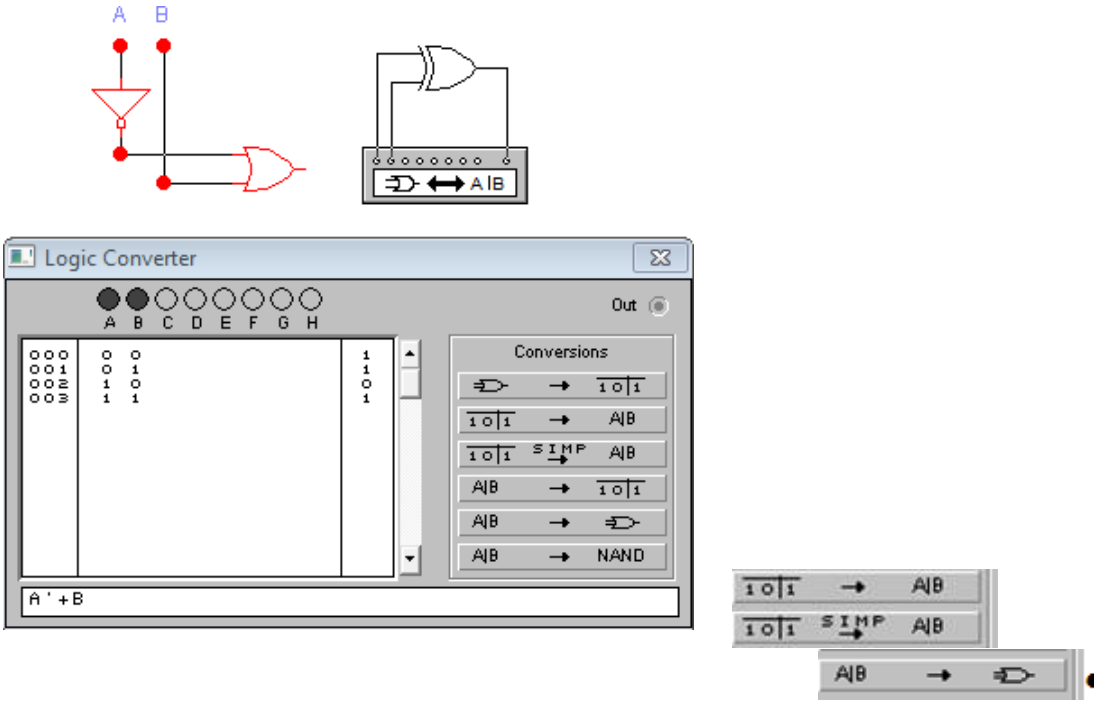
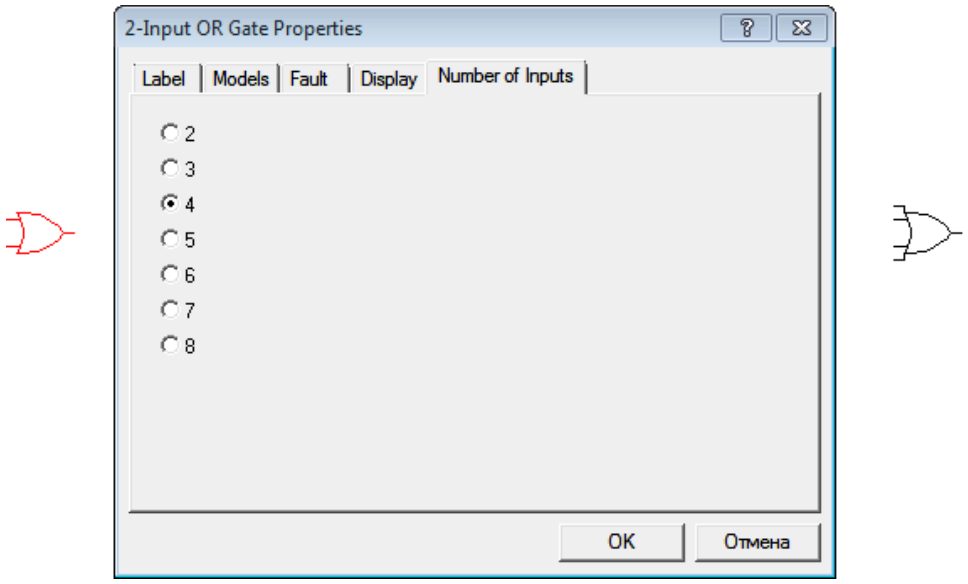


Fig. 5 – The result of synthesizing a logical device according to a given truth table Synthesized

logical device shown V top left corner rice. 5, A his
Boolean expression A ' +B presented on additional display V lower parts ***Logic Converter*** .

In general, to perform synthesis, it is advisable to proceed as follows . Click the cursor on the logical converter icon directly on the ruler devices we reveal it facial panel. Let's activate cursor of the button terminal A, B, ..., H (starting with A), the number of which is equal to the number of inputs of the synthesized device . We make the necessary changes in the OUT column and after pressing on the converter panel specified higher buttons management we get result V view schemes on working program field and Boolean expression in the additional display.

Finally, note that for the two-input elements shown in Fig. 2, the number of inputs can be increased to eight by double-clicking on the component icon. dialogic window (cm. rice. 6). By default V this window indicated minimally possible number inputs equal to two. Note also that when optimizing logical devices with the purpose of receipt most simple schemes are used various methods minimization boo left expressions (cards Carnot, diagrams Veicha And etc.), however at number entrances more five this process becomes extremely labor-intensive.



Rice. 6 - Window installations quantities entrances logical element

Contents of the practical work performed students V in the course classes

1. Description laboratory equipment:

– PC for each student;

– Electronics Workbench (EWB) schematic modeling software editor, version 5.12 or later, or NI Multisim Education version;

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) In case of emergency situations, it is necessary to immediately disconnect the equipment from the power supply, inform the teacher about this and act according to his instructions .

6) If equipment catches fire, it must be immediately de-energized, the teacher must be informed, measures must be taken to eliminate the fire, and the teacher must act as instructed.

7) By ending work With laboratory equipment (computers) his must be switched off in the established order.

Tasks to be completed during practical work

Tasks basic level:

1) Confirmation laws Boolean algebra With help programs Electronics Workbench circuit simulation.

Tasks increased level:

2) Synthesize By minimized Boolean functions logical devices With using the Electronics Workbench circuit simulation program.

Order execution work

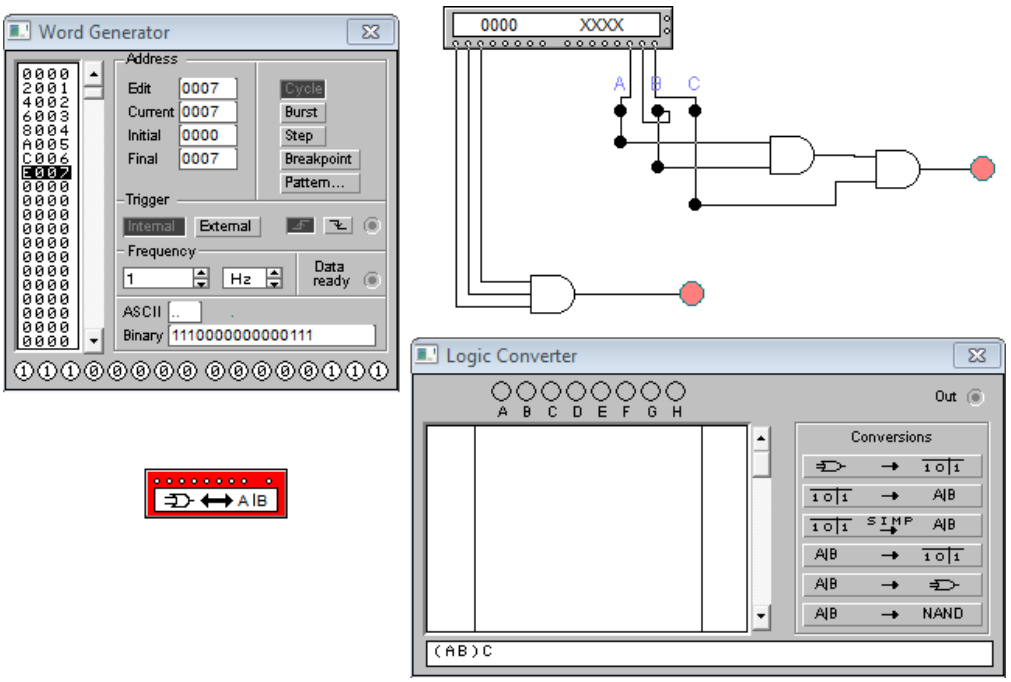
Task 1. Confirmation of the laws of Boolean algebra using the Electronics Workbench circuit simulation program.

Task 1.1. Confirm the commutative law. To do this, perform the following operations:

1) WITH help logical converter analyze tables truth elements AND, OR.

2) Do it conclusions By results of the analysis.

Task 1.2. Confirm associative law. To do this , perform the following operations shown in Fig. 11:



Rice. 11 - Study design For confirmation associative law

1) In the logic converter screen-line, write the Boolean function for the associative law (see Fig. 11):

A(BC) or (AB)C or A+(B+C) or (A+B)+C.

2) Click synthesis button logical devices 

.

3) Connect the synthesized device to the three left outputs of the word generator, as in Fig. 11, and connect a logic probe to the output of the device.

4) From the Logical Elements component, drag and drop either the AND or OR element onto the workspace, depending on which Boolean function is being analyzed.

5) Install For selected element quantity entrances, equal three. For this Right -click on the logic element and in the context-sensitive menu that opens, select the Component Properties... command. In the dialog box, open the Number of inputs tab and set the option next to the number 3.

6) Connect 3-x entrance logical element left To first 3rd exits word generator , and connect a logic probe to the output of the element as shown in Fig. 11.

7) IN generator words write it down V below cells next codes:

Cell	Code word
0000	**0000**
0001	**2001**
0002	**4002**
0003	**6003**
0004	**8004**
0005	**A005**
0006	**C006**
0007	**E007**

8) In the word generator, set the cycle start address to 0000 and the final address to 0007. Set the clock frequency to 1 Hz.

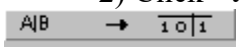
9) Launch generator, by clicking button Cycle.

10) Analyze the state of the generator outputs and the operation of the elements connected to it .

11) Do it conclusions By results analysis.

Exercise 1.3. Confirm law repetitions. For this complete next operations:

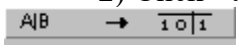
1) IN screen-line logical converter write it down Boolean function this forhorse AA or A+A.

2) Click the button to display the truth table corresponding to this expression  .

3) Analyze received table truth, And draw conclusions.

Task 1.4. Confirm the law of double inversion. To do this, perform the following operations:

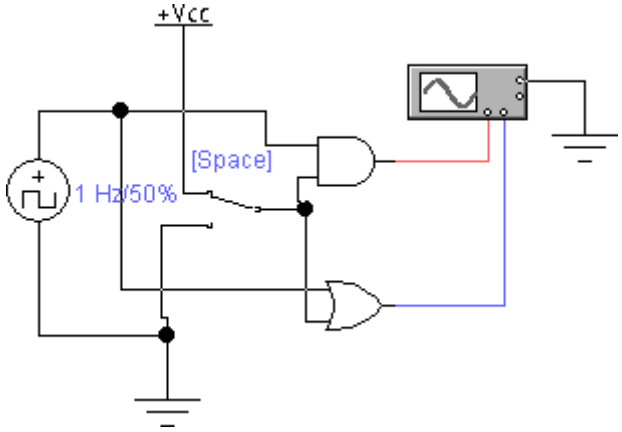
1) In the screen-line of the logical converter, write the Boolean function of this law A".

2) Click the button to display the truth table corresponding to this expression  .

3) Analyze received table truth, And draw conclusions.

Exercise 1.5. Confirm laws of the universal And zero sets. For this you perform the following operations:

1) Collect diagram research, given on rice. 12. IN original condition To The inputs of the elements are connected to the potential of a logical unit.



Rice. 12 - Scheme research For confirmation laws zero And universal sets

2) On generator of such impulses install frequency 1 Hz And voltage 5 V.

3) On the oscilloscope, set the horizontal (time) sweep to 0.50 s/div, and the vertical (amplitude) sweep to 5 V/div for both channels.

4) Launch operation of the circuit, by clicking on the switch.

5) Display diagrams voltage With screen oscilloscope V report.

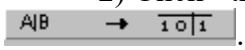
6) By clicking key Space, connect To entrances elements AND, OR potential logical zero.

7) Repeat points 5 And 6.

8) Conduct analysis And do conclusions.

Task 1.6. Confirm the distributive law of Boolean algebra. To do this, perform the following operations:

1) In the screen-line of the logical converter, write the Boolean function of this law A+BC.

2) Click the button to display the truth table corresponding to this expression  . Record the truth table in the report.

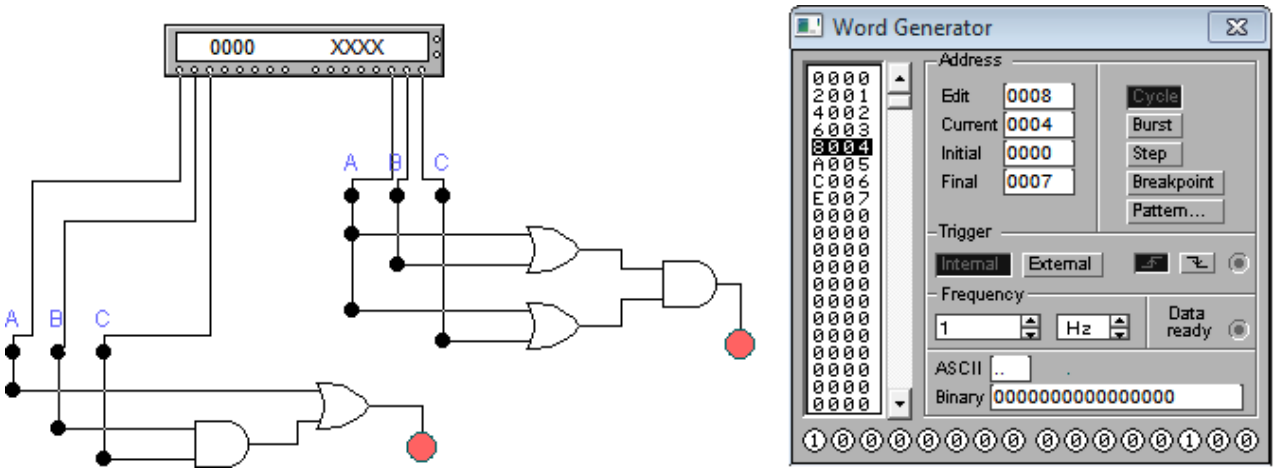
3) Click button synthesis logical devices By this Boolean functions  .

4) IN screen-line logical converter write it down identical Boolean function (A+B)(A+C).

5) Determine And write it down V report table truth this functions. Compare With the truth table previously obtained in point 2.

6) Use a logic converter to synthesize a logic device based on the given function.

7) Connect the synthesized devices to the three left and three right outputs of the word generator, as in Fig. 13, and connect logic probes to the outputs of the devices.



Rice. 13 - Scheme research For confirmation distribution law

8) IN word generator write in below cells the following codes:

Cell	Code word
0000	0000
0001	2001
0002	4002
0003	6003
0004	8004
0005	A005
0006	C006
0007	E007

9) In the word generator, set the cycle start address to 0000 and the final address to 0007. Set the clock frequency to 1 Hz.

10) Launch generator, by clicking button Cycle.

11) Analyze the state of the generator outputs and the operation of the elements connected to it .

12) Do it conclusions By results conducted analysis.

Exercise 1.7. Confirm law De Morgana. For this complete next operations
:

1) Conduct procedure research similar previous point.

2) IN report reflect tables truth And research schemes .

3) Do it conclusions By results conducted analysis.

Exercise 1.8. Confirm law additionality. For this complete next operations:

1) In the screen-line of the logical converter, write the Boolean function of this law AA' or A+A'.

2) Click on button  displays tables truth, corresponding to these expressions. Write the truth tables in your report and analyze them.

3) Do it conclusions By results conducted analysis.

Exercise 8.1. Confirm laws absorption And gluing. For this complete the following operations:

1) Conduct algebraic transformations Boolean expressions And using the axioms of Boolean algebra to confirm these laws.

2) Reflect these transformations in the report and draw conclusions based on the results of - the analysis.

Exercise 2. Synthesize By minimized Boolean functions logical devices using the Electronics Workbench circuit simulation program.

To do this, follow these steps: operations:

1) Write down V report given By number options Boolean function from tables 1.

Table 1 – Table of task options

Option number	Function
1.	F1=A'B'C+A'BC'+A'BC+AB'C'; F2 = A'BC' + AB'C' + AB'C + ABC' + ABC
2.	F1=A’B’C+A’BC’+AB’C’+AB’C; F2=A’BC+AB’C’+AB’C+ABC’+ABC
3.	F1=A’B’C+A’BC’+AB’C+ ABC’; F2=A’B’C+A’BC+AB’C+ABC’+ABC
4.	F1=A’B’C+A’BC’+ABC’+ABC; F2=A’B’C+A’BC+ AB’C’+ABC’+ABC
5.	F1=A’B’C’+A’BC’+AB’C’+ABC’; F2=A’B’C+A’BC’+AB’C’+AB’C+ABC
6.	F1=A’B’C’+A’BC+AB’C+ABC’; F2=A’B’C’+A’B’C+A’BC’+ABC’+ABC
7.	F1=A’B’C+A’BC’+AB’C+ABC; F2=A’B’C’+A’BC+AB’C’+AB’C+ABC
8.	F1=A’B’C’+AB’C’+AB’C+ABC; F2=A’B’C+A’BC’+A’BC+ABC’+ABC
9.	F1=A’B’C’+A’B’C+A’BC’+AB’C’; F2=A’BC+AB’C’+AB’C+ABC’+ABC
10.	F1=A’BC’+A’BC+AB’C’+AB’C; F2=A’B’C’+A’B’C+A’BC+ABC’+ABC
11.	F1=A’BC’+AB’C’+AB’C+ABC’+ABC F2=A’B’C+A’BC’+A’BC+AB’C’
12.	F1=A’BC+AB’C’+AB’C+ABC’+ABC F2=A’B’C+A’BC’+AB’C’+AB’C
13.	F1=A’B’C’+A’B’C+A’BC+ABC’+ABC F2=A’B’C+A’BC’+AB’C+ ABC’
14.	F1=A’BC+AB’C’+AB’C+ABC’+ABC F2=A’B’C+A’BC’+ABC’+ABC
15.	F1=A’B’C+A’BC’+A’BC+ABC’+ABC F2=A’B’C’+A’BC’+AB’C’+ABC’
16.	F1=A’B’C’+A’BC+AB’C’+AB’C+ABC F2=A’B’C’+A’BC+AB’C+ABC’
17.	F1=A’B’C’+A’B’C+A’BC’+ABC’+ABC F2=A’B’C+A’BC’+AB’C+ABC
18.	F1=A’B’C+A’BC+AB’C+ABC’+ABC F2=A’B’C’+AB’C’+AB’C+ABC
19.	F1=A’B’C+A’BC+ AB’C’+ABC’+ABC F2=A’B’C’+A’B’C+A’BC’+AB’C’
20.	F1 = A'B'C + A'BC' + AB'C' + AB'C + ABC F2 = A'BC' + A'BC + AB'C' + AB'C

2) Write down function F1 V screen-line of the logical converter.

3) Display the truth table of the device by pressing the button  and check the correctness of the function set.

4) Click button  synthesis logical devices By this Boolean function.

5) Display synthesized device V report.

6) Minimize given function, by clicking button  .

7) Synthesize a minimized logic device by pressing the button  .

8) Display minimized synthesized device V report, compare his with a previously synthesized device.

9) Repeat points 2–8 For synthesis devices By Boolean functions F2.

10) WITH help generator words check work synthesized devices.

11) Do it conclusions By results conducted synthesis.

4. Content report about work

IN In the report, please provide:

– topic And target work work ,

– practical tasks;

– designs ;

– results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, voltage diagrams, etc.;

– conclusions O done work.

5. Control questions For preparation To protection report:

1) Axioms And laws Boolean algebra.

2) Brief characteristic And order modeling schemes With help programs Electronics Workbench circuit simulation .

3) Characteristic And order work With logical converter program Electronics Workbench circuit simulation .

4) Characteristics and operating procedure of the word generator of the Electronics Workbench circuit simulation program.

5) Characteristic And order work With logical analyzer program Electronics Workbench circuit simulation .

6) Methodology confirmation laws Boolean algebra With help programs Electronics Workbench technical simulation circuit .

7) Order synthesis logical devices With help programs Electronics Workbench circuit simulation.

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 11

Subject: STUDY BASIC LOGICAL ELEMENTS

Time – 2 academic hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– realize circuit design (computer) modeling basic logical elements using universal software packages ;

– conduct research on basic logic elements based on their circuit models,

– realize synthesis logical devices With using universal packages of computer applications;

– collection and analysis of information to generate initial data for the design of digital devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program schematic editor Electronics Workbench (EWB) simulation , version 5.12 or later, or NI Multisim Education version;

– application for mathematical and engineering calculations Mathcad Professional version not lower than 15.0;

– electronic methodological development By laboratory work.

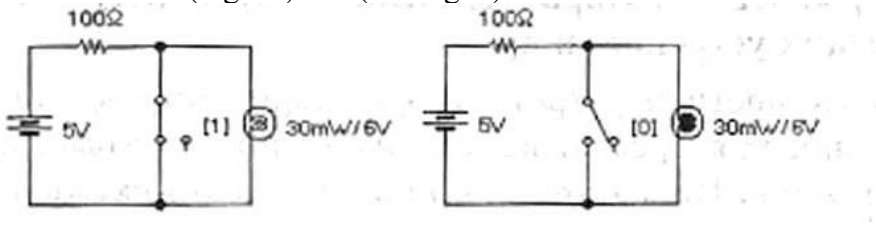
STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study basic logical elements on basis their circuit design skii models.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

It is known, What ***mathematical basis digital computing devices is binary arithmetic*** , which uses only two numbers – 0 and 1. The choice of binary systems numeration was dictated requirements simplicity technical implementation the most difficult tasks With using total one basic element – ***electronic key, which has two conditions*** : included (closed) or turned off (open). IN computer the first closed state of the key is taken as a conditional (logical) zero, then the second open state will reflect a conditional (logical) one (see Fig. 1).



a) *b)*

Rice. 1 - Electromechanical imitators: A) logical units, b) zero in inverse mode

When key 1 is pressed, the indicator goes out, recording the state 0, and, conversely, when the key is released, the indicator lights up, recording – 1. The circuits shown in Fig. 1, according to the output signal (the state of the indicator lamps), are the opposite or inverse of the state of the key, therefore such keys are called inverters.

Because digital systems contain a huge number of keys (in just one microprocessor their some millions) And They Not can report Friend to a friend O In their state, the lights flash, and ***electrical voltage signals are used to exchange information*** . In this case, the switches are usually used in inverse mode.

In digital technology, practical analogs of the circuits discussed are commonly called - logic **elements .** They differ in the nature of the functions they implement, the number of inputs (based on the number of simultaneously active variables), the number of outputs, and other characteristics. Their performance is assessed solely from a logical standpoint, without regard to practical implementation (technical base, power supply method, etc.).

Entrances And exits logical elements V dependencies from level signal, at which a certain value of a binary variable is perceived or generated are ***divided into*** **direct** ***and*** **inverse** . At the direct input (output), the binary variable has the value logical 1, When signal on this at the entrance (exit) has meaning, accepted for 1. At an inverse input (output), a binary variable has the value 1 when the signal level at this input (output) corresponds to the state taken as 0.

To logical inputs You can supply constant logical values levels 1 and 0 (constant 1 And constant 0) according to laws universal And zero sets. Entrances, equivalent in logical relation (which Can change in some places without damage For performed functions), allow unification according to the law of repetition: in this case they act as one input.

In domestic literature and documentation, ***logical elements according to GOST 2.743-82*** “Conventional graphic symbols in circuits. Elements of digital technology” ***are depicted rectangle*** (So called main field), V top parts whom indicate symbol functions: & For AND, 1 For OR. Entrances show With left sides rectangle , exits - With right. Allowed other orientation rectangle, at which the entrances are located above, A exits from below. ***Inverse entrances And exits stand out indicator of the logical relationship with a small circle at the pin*** . The power and common (ground) pins are usually Not are shown. IN case necessity tires, Not load-bearing logical information (in volume number nutrition And general), let down To left or right side rectangle And are marked with an asterisk.

In digital devices, ***logical states are represented by two voltage levels*** (potentials): ***high*** , close ones To voltage source nutrition, ***And low*** , close To zero. This So called potential system performances information, for which characteristic direct connection between separate elements schemes. The duration of potential signals is determined by the frequency of information change, and switching pulses are voltage drops from one level to another.

Two level voltage , characterizing logical states, ***are determined simply as a higher H*** (High) ***and a lower L*** (Low). These two values are called logical levels. There are two genus So called logical conventions depending on what voltage level encodes a logical 1 (and, accordingly, a logical 0). In the positive logic convention, a higher voltage level (H) corresponds to a logical 1, and a lower one to a logical 0. In the negative logic convention, it is vice versa.

Element, performing logical functions, Can evaluate With positions How both positive and negative logic. Its functional role in both cases will be different. This important position, which often use on practice, flows out from laws

De Morgan. For example, according to the rules of positive logic (H = 1), the element performs the AND operation, and in negative logic (H = 0), it acts as an OR element, which follows from De Morgan's laws.

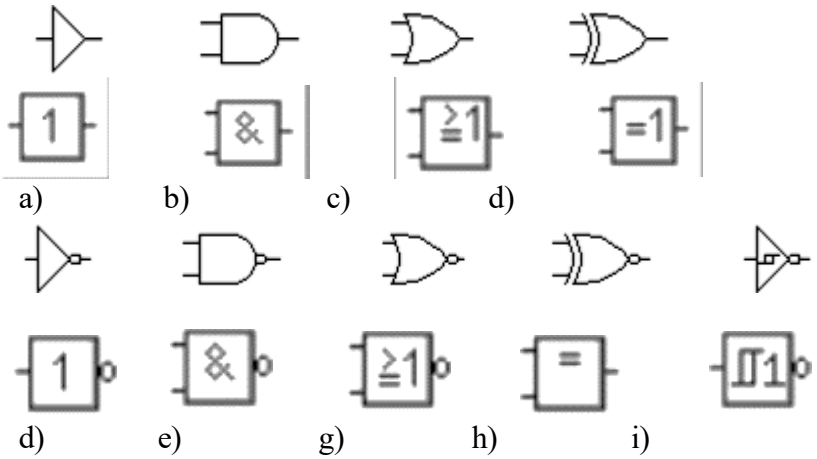
WITH taking into account said elements, performing logical operations, allowed depicted on diagrams in two logically equivalent forms. Given an image of a logical element, its equivalent form can be obtained by performing the following transformations:

a) in the main field of the element image, replace the operation symbol & with the symbol 1 or vice versa;

b) All straight entrances replace inverse, A inverse straight;

V) all direct exits replace inverse, and inverse - direct.

Fig. 2 shows ***the designations of basic logical elements adopted in the EWB program*** , according to foreign (American) standards, and below, European (Russian) standards.



Rice. 2 - Graphic designations logical elements in EWB

Fig. 2 shows:

A) buffer logical element; b) AND element;

V) element OR (OR);

G) element EXCLUSIVE OR (XOR);

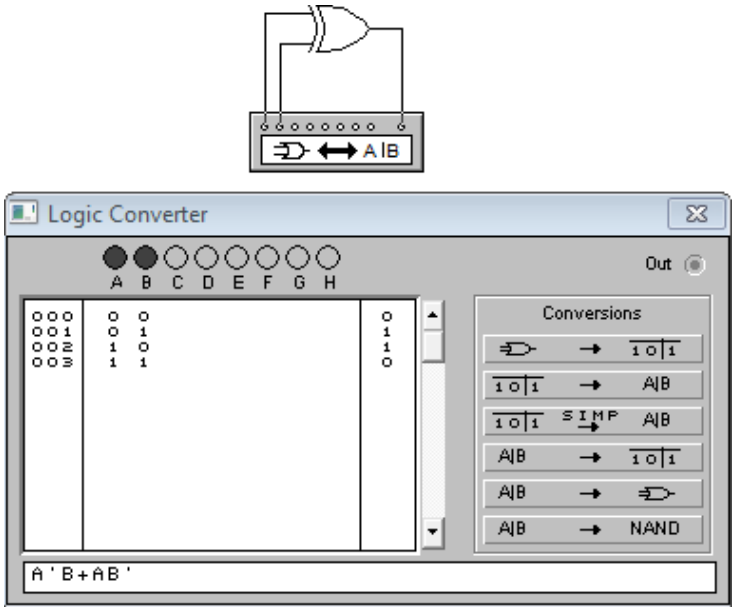
d) inverter (NOT);

e) NAND gate; g) element OR-NOT (NOR);

c) element EXCLUSIVE OR-NOT (XNOR), otherwise equivalence; i) Schmitt trigger.

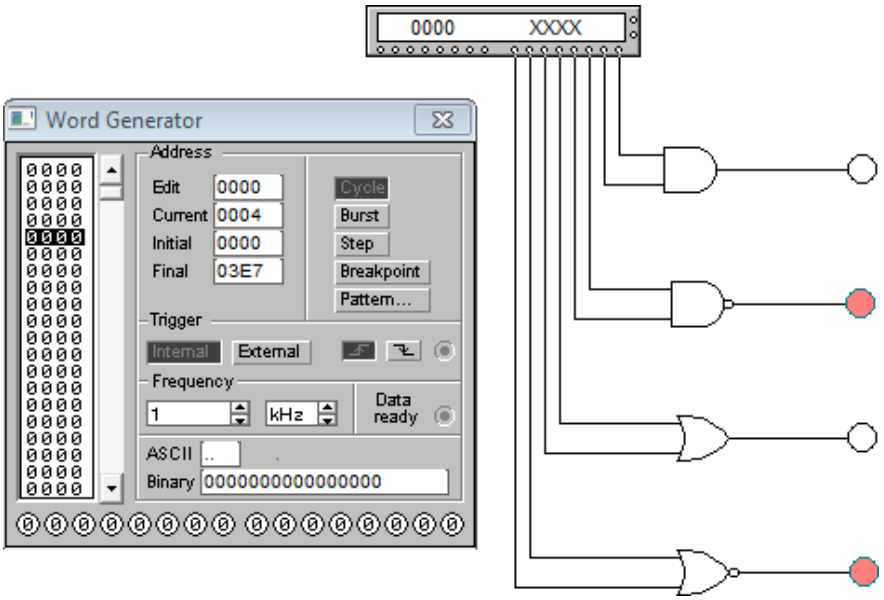
It is advisable to model logical circuits in the EWB program using logical converter (Logic Converter) . IN quality example on rice. 3, A when introduced scheme For research element EXCLUSIVE OR. Order connections of the studied element to the logical converter is obvious from Fig. 3. It is also obvious that What at availability two entrances possible only four combinations input signals, which is displayed on the converter screen in the form of a truth table, which is generated after pressing the button  .

To obtain a Boolean expression for the element being studied, press the button  . This expression is shown on the additional display located V lower parts facial panels, V view two terms, corresponding output signal TRUE (signal logical units on exit OUT). Comparison The comparison of the obtained expression with the truth table convinces us that there are actually two such combinations, A ' B and AB ' , therefore the Boolean function has the form: A ' B + AB ' , where the + sign corresponds to the logical operation OR.



Rice. 3 - Study logical elements With help logical converter

IN quality example use generator words (Word Generator) for research of logical elements in Fig. 4 shows a circuit in which the corresponding binary combination is fed to the inputs of the AND, NAND, OR, NOR elements, A reaction elements indicated included on their exits logical samples by nicknames.



Rice. 4 - Study logical elements With help generator words

With the help of a logic converter it is possible to carry out not only the analysis of logical devices, But And their synthesis . Let's say, What us required make up diagram And Boolean expression For logical element, at whom day off combination V table the truth value is not 0110, as in Fig. 3, but 1101. To make the necessary changes, we mark the symbol to be changed with the cursor in the OUT column, change it using the keyboard and then, moving along the column with the keys cursor control, change symbols as needed V others lines. After contributions everyone changes sequentially press on buttons given on rice. 5 (V right lower corner), And we get result, presented on Fig. 5.

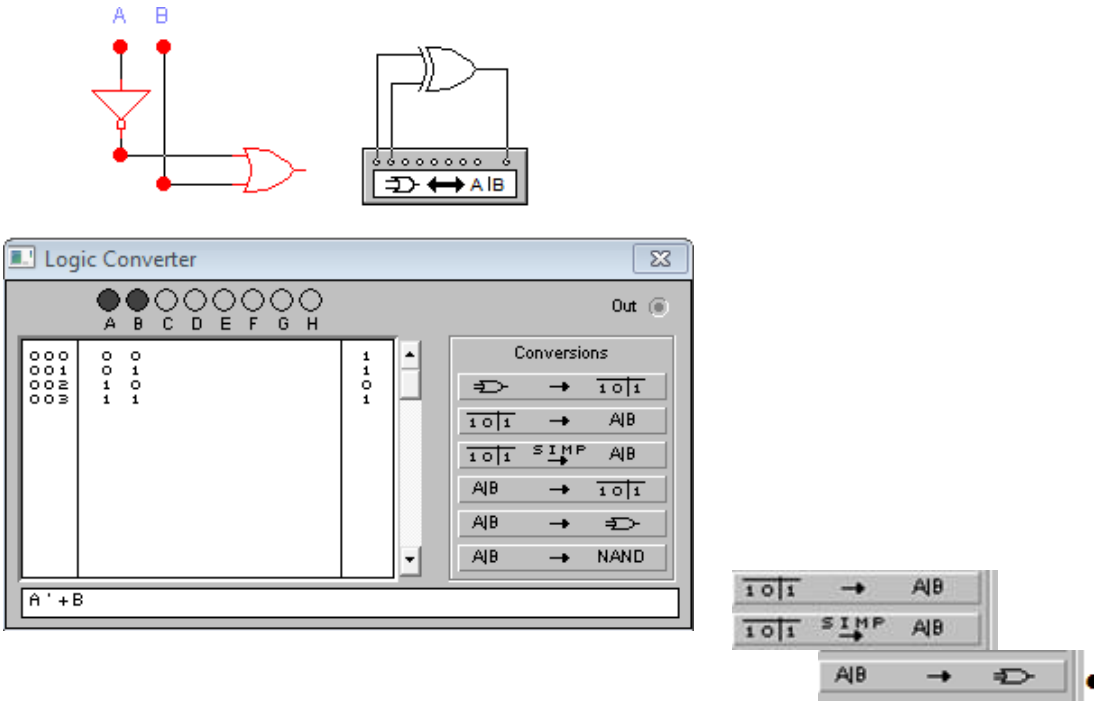
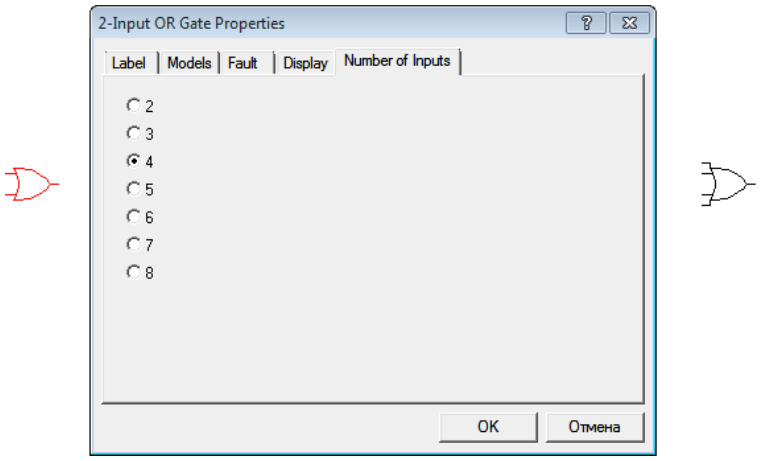


Fig. 5 – The result of synthesizing a logical device according to a given truth table Synthesized

logical device shown V top left corner rice. 5, A his Boolean expression A ' +B presented on additional display V lower parts ***Logic Converter*** .

In general, to perform synthesis, it is advisable to proceed as follows . Click the cursor on the logical converter icon directly on the ruler devices we reveal it facial panel. Let's activate cursor of the button terminal A, B, ..., H (starting with A), the number of which is equal to the number of inputs of the synthesized device . We make the necessary changes in the OUT column and after pressing on the converter panel specified higher buttons management we get result V view schemes on working program field and Boolean expression in the additional display.

Finally, note that for the two-input elements shown in Fig. 2, the number of inputs can be increased to eight by double-clicking on the component icon. dialogic window (cm. rice. 6). By default V this window indicated minimally possible number inputs equal to two. Note also that when optimizing logical devices with the purpose of receipt most simple schemes are used various methods minimization boo left expressions (cards Carnot, diagrams Veicha And etc.), however at number entrances more five this process becomes extremely labor-intensive.



Rice. 6 - Window installations quantities entrances logical element

Contents of the practical work performed students V in the course classes

1. Description laboratory equipment:

– PC for each student;

– Electronics Workbench (EWB) schematic modeling software editor, version 5.12 or later, or NI Multisim Education version;

Requirements security at execution works:

1) Students who have completed the required occupational safety training are allowed to conduct laboratory work.

2) Turning on laboratory installations (computers) is being carried out only With permission of the teacher.

3) At conducting laboratory work Not allowed usage devices, equipment not provided for in the lesson plan.

4) Not allowed at included equipment switch cables nutrition, connecting cables of blocks and components of laboratory installations (computers).

5) In case of emergency situations, it is necessary to immediately disconnect the equipment from the power supply, inform the teacher about this and act according to his instructions .

6) If equipment catches fire, it must be immediately de-energized, the teacher must be informed, measures must be taken to eliminate the fire, and the teacher must act as instructed.

7) By ending work With laboratory equipment (computers) his must be switched off in the established order.

Tasks to be completed during practical work

Tasks basic level:

1) Conduct study logical ventilator.

2) Conduct analysis logical element NOT (inverter).

3) Conduct analysis buffer element.

4) Conduct analysis features work buffer element on three states.

Tasks increased level:

5) Conduct analysis logical elements AND, AND- NOT.

6) Conduct analysis logical elements OR And OR- NOT.

7) Conduct analysis logical elements exclusive OR And equivalence.

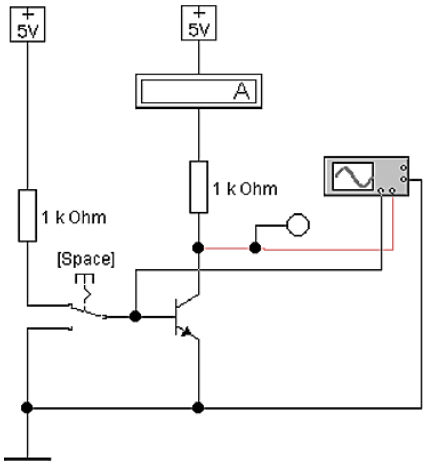
Order execution work

Exercise 1. Conduct study logical ventilator . To do this, follow these steps:

1) IN working field programs Electronics Workbench collect diagram research, shown in Fig. 7.

2) Modeling And research are being carried out student on one's own, based based on the knowledge, skills and abilities acquired during laboratory work in the section "Analog circuit design".

3) Do it conclusions By results work done .



Rice. 7 - Scheme research ventilator

Exercise 2. Conduct analysis logical element NOT (inverter).

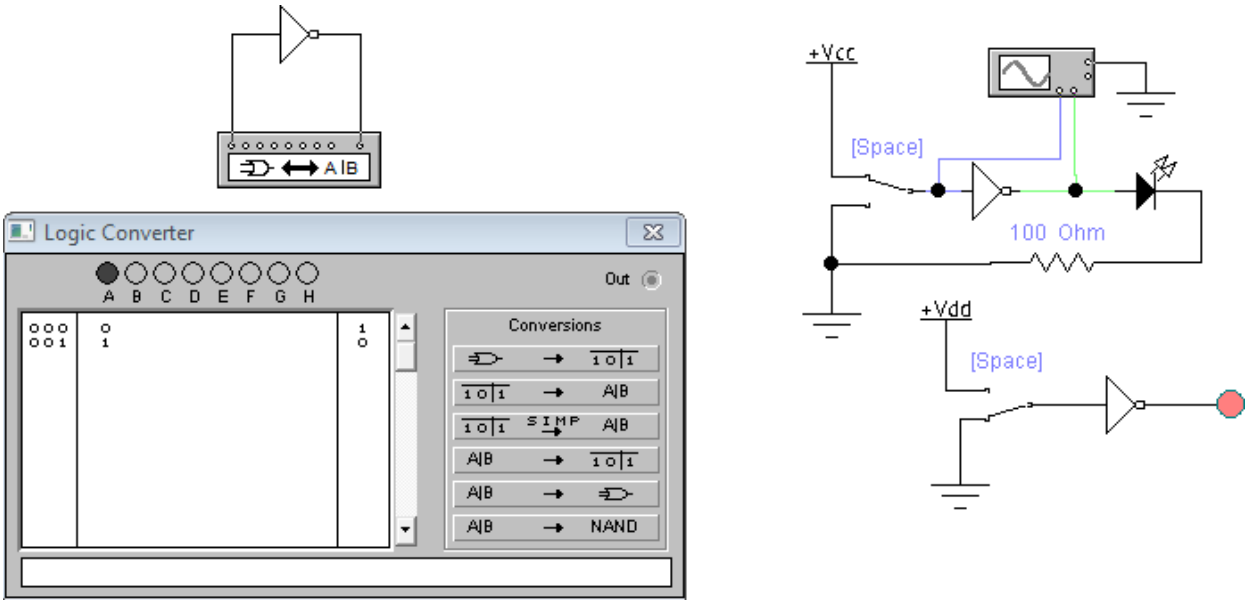
To do this, follow these steps: operations:

1) IN working field programs Electronics Workbench collect schemes research, given on Fig. 8. On the left parts drawing given logical scheme research With using a logic converter, in the upper right part is the electrical circuit diagram, V which study is being carried out With help oscilloscope, V right lower parts - an equivalent electrical circuit in which the study is carried out in a more simplified manner using a logic probe.

2) Double click open logic converter.

3) Display table truth inverter, by clicking on button  .

4) Write down V report table truth inverter.



Rice. 8 – Inverter Research Schemes

5) Double-click to open the oscilloscope, then expand it fully by clicking Expand button.

6) Tune oscilloscope, having installed temporary development (Time base) on 0.10 ms/div, a vertical (amplitude) developments By both of them channels (Channel A, Channel B) on 2V/div.

7) Turn on diagram V work, by clicking switch V right top corner windows about - programs.

8) Switching switch, by pressing keys "Space", With help measure the oscilloscope And display V report logical levels voltage on at the entrance And exit inverter. Compare these logical levels With table truth, received With help logical converter.

9) Investigate the operation of an inverter using a logic probe on a simplified circuit diagram substitutions, connecting By queues To his entrance logical unit (source power supply) and logical zero (zero bus or ground bus). Analyze the state of the probe from the logical voltage level at the inverter output.

10) Do it conclusions By results work done .

Exercise 3. Conduct analysis buffer element.

To do this, follow these steps: operations:

1) IN schemes, given on rice. 7, replace inverter buffer element, For What to delete inverter team Cut V context-sensitive menu, called by pressing Right-click on the element's UCG. Open the Logical Elements panel, select the buffer element, and connect it to the circuit.

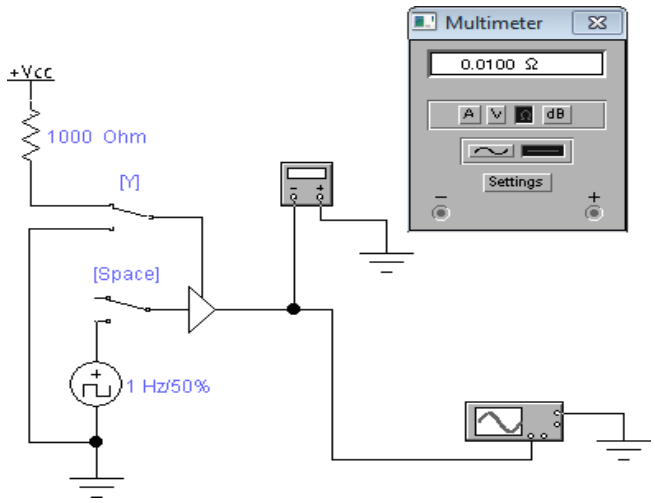
2) For collected schemes research buffer element repeat procedure research given in points 2–9 of the previous task.

3) Do it conclusions By results work done .

Task 4. Conduct an analysis of the operating features of a three-state buffer element .

To do this, follow these steps: operations:

1) IN working field programs Electronics Workbench collect diagram research, shown in Fig. 9.



Rice. 9 - Scheme research buffer element on three states

2) Set up the clock generator by setting the voltage to 5 V, the frequency to 1 Hz, and the duty cycle to 50%.

3) Tune multimeter (tester), by clicking button resistance (Ω) And permanent current (--), as shown in Fig. 15.

4) Set up the oscilloscope by opening double-click it and having installed temporary time - base at 0.50 s/div, and vertical (amplitude) sweeps on both channels (Channel A, Channel B) at 5V/div.

5) Press the switch to start the circuit and measure the resistance of the circuit at the output of the buffer element using a multimeter.

6) Connect the clock generator to the buffer input by pressing the spacebar. Display the voltage waveforms from the oscilloscope screen in the report.

7) Disable work schemes, return switches V initial state.

8) Change the logic voltage level at the control input of the buffer element ; to do this, press the "Y" key. Measure the resistance of the circuit at the output of the buffer element using a multimeter.

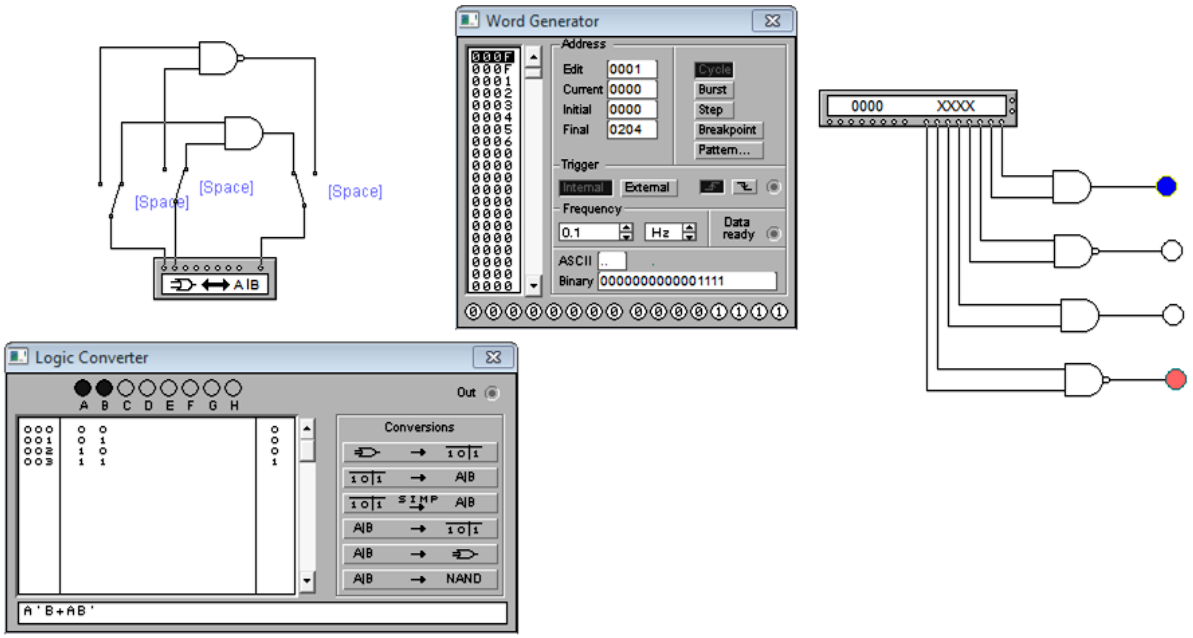
9) Connect the clock generator to the buffer input by pressing the spacebar. Display the voltage waveforms from the oscilloscope screen in the report.

10) Do it conclusions By results work done .

Exercise 5. Conduct analysis logical elements AND, AND- NOT.

To do this, follow these steps: operations:

1) IN working field programs Electronics Workbench collect schemes research, shown in Fig. 10



Rice. 10 – Research schemes logical elements AND, AND- NOT

2) IN logical converter press button displays truth tables .

3) Bring in V report table truth element AND.

4) By pressing keys "Space" connect To logical converter another NAND gate, then click the truth table display button and enter it into the report.

5) IN generator words V first (upper) cells write down code words 0000 (V cell with address 0000), 0055 (into the cell with address 0001), 00AA (into the cell with address 0002) and 00FF (into the cell with address 0003), as a result of accessing these cells, logical values will be formed at the generator output potentials respectively 0000 0000 0000 0000, 0000 0000 0101 0101, 0000 0000 1010 1010 and 0000 0000 1111 1111.

6) In the Initial window (the initial address for starting the generator), enter the zero cell code -0000. Start the generator by pressing the Step button.

7) Analyze addiction levels logical voltage on exit AND, NAND elements from the levels at their input.

8) Changing elementary address sequentially on 0001, 0002 And 0003, launching press generator buttons Step, conduct analysis dependencies levels logical voltage on in the course of AND, NAND elements from the levels at their input.

9) Do it conclusions By results work done .

Exercise 6. Conduct analysis logical elements OR And OR- NOT.

To do this, follow these steps: operations:

1) In the research schemes shown in Fig. 16, replace the existing elements logical elements OR And OR-NOT, changing element AND element OR, A AND-NOT – OR-NOT element.

2) Execute points 2 - 8 previous task For elements OR And OR- NOT.

9) Do it conclusions By results work done .

Exercise 7. Conduct analysis logical elements exclusive OR And equivalence .

To do this, follow these steps: operations:

1) In the research circuits shown in Fig. 16, replace the existing elements with the logical elements Exclusive OR and Exclusive NOR-NOT (equivalence element), changing the OR element to an Exclusive OR element, and the NOR-NOT element to an Exclusive NOR-NOT.

2) Execute points 2 - 8 previous tasks For elements Exclusive OR and Exclusive OR-NOT (element of equivalence).

9) Do it conclusions By results work done .

Content report about work

IN In the report, please provide:

- topic And target work work ,
- practical tasks;
- designs ;
- results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, voltage diagrams, etc.;
- conclusions O done work.

5. Control questions For preparation To protection report:

1) Principle work electronic key (valve).
2) Characteristic protozoa logical operations.
3) Conventional graphic notation and truth tables basic logical elements .
4) Brief characteristic And order modeling seven With help programs Electronics Workbench circuit simulation .
5) Characteristic And order work With logical converter program Electronics Workbench circuit simulation .
6) Characteristics and operating procedure of the word generator of the Electronics Workbench circuit simulation program.
7) Characteristic And order work With logical analyzer program Electronics Workbench circuit simulation .
8) Order analysis main logical elements With help programs Electronics Workbench circuit simulation .

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 12

Subject: **STUDY COMBINATIONAL DIGITAL DEVICES: ADDERS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of combinational digital devices using universal packages of applied computer programs;

– conduct research combinational digital devices based on their schematic models,

– synthesis of combinational digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study of adders.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study adders.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

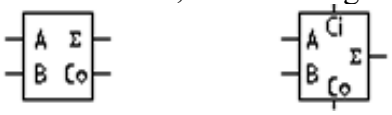
Brief theoretical or reference and information materials

Under ***combinational digital device*** *(KCU)* understood digital A device that converts a set of *N* input digital signals into *M* output signals, where the state of the output signals at a given moment in time is determined by the state of the input signals at the same moment. In other words, a digital control unit (DCU) "does not remember" the history of signals arriving at its inputs. The operating rules of a DCU are determined by the Boolean functions they implement.

Implementing a control logic unit (CLU) involves selecting specific logic elements from a given set and connecting them in such a way as to ensure the dependence of digital output signals on input signals according to specified operating rules. Low-integration integrated combinational logic circuits (ILCs), which form the basis of digital electronics, are widely used in the implementation of CLUs.

Arithmetic adders

Arithmetic adders are composite part So called arithmetic logic units (ALU) of microprocessors (MP). They are also used to form the physical address of memory cells in MP with a segmented memory organization. In the EWB program, arithmetic adders are represented in the Digital component library by two basic devices, shown in Fig. 1: a half adder and a full adder .

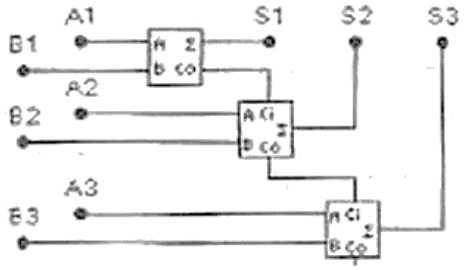


a) b)

Rice. 1 - Schemes half adder (A) And complete adder (b)

They have the following pin assignments : A, B are the inputs of the operands being summed, Σ – result summation, So - exit transfer, Ci - entrance transfer. Multi-bit The sum of the torus is created on the basis of one half adder and ***n*** full adders.

IN quality example on rice. 2 given structure three-digit adder. On the first and second terms are fed to the inputs Al, A2, A3 and Bl, B2, B3, respectively, and the result of the summation is removed from the outputs SI, S2, S3.



Rice. 2 - Three-digit adder

To study the internal structure and operating logic of adders, a logic converter is used.

Content practical work, performed students during the lesson

Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

– program circuit design modeling Electronics Workbench EWB 5.12.

Tasks For execution laboratory work:

Base level:

1) Explore the internal structure and logic operation of a half adder using a logic converter and a word generator.

2) Explore the internal structure and logic operation of a full sum torus using a logic converter and a word generator.

3) To investigate the operating logic of a 4-bit adder using a word generator.

Increased level:

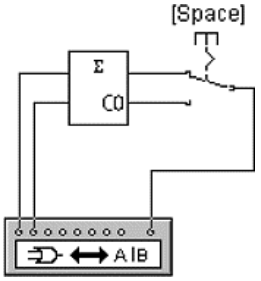
4) Synthesize given adder-subtractor And conduct his study.

Order execution works:

1. Study arithmetic adders

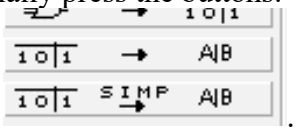
Task 1.1. Explore the internal structure and operating logic of the half adder, using logical converter And generator words. For this perform the following operations:

1) , the output of the summation result Σ in the half adder is connected to the OUT terminal of the logic converter .



Rice. 3 - Scheme research half adder

2) IN logical converter sequentially press the buttons:



.

IN result get And write down V report table truth half adder And his logical expression for the result of the summation.

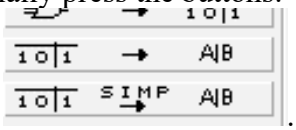
3) Compare received data with tables truth of basic logical elements and draw a conclusion about which element implements the obtained Boolean function when connecting the Σ ουτπυτ of the half adder to the OUT terminal of the converter (as shown in Fig. 3).

4) Synthesize this element in a fully functional AND, OR, NOT basis by pressing the button 

.

5) WITH help switch, by clicking key "Space", connect terminal OUT pre converter to the carry output of the half adder.

6) IN logical converter sequentially press the buttons:



.

IN result get And write down V report table truth half adder And his logical expression for the result of the carry.

7) Define, Which logical element implements function transfer half-sum of a torus, synthesize it using a logical converter.

8) Display in the laboratory report the circuit of the synthesized half- adder in the AND, OR, NOT basis.

9) Conduct study logic functioning synthesized half-sum of a torus. To do this, perform the following operations:

— connect the inputs of the synthesized half adder to the low-order outputs of the generator words, A To entrances And exits half adder connect logical samples For indication of input data and results of summation and transfer;

— write down V first 4 cells generator words respectively codes 0000, 0001, 0002 and 0003, which form the values of operands A and B at the input of the half adder;

— set the word generator to step-by-step operation mode by pressing the generator's "Step" button, check the logic of the half adder's operation;

— include in the laboratory report the results obtained as a result of the research truth table of the half adder (table 1).

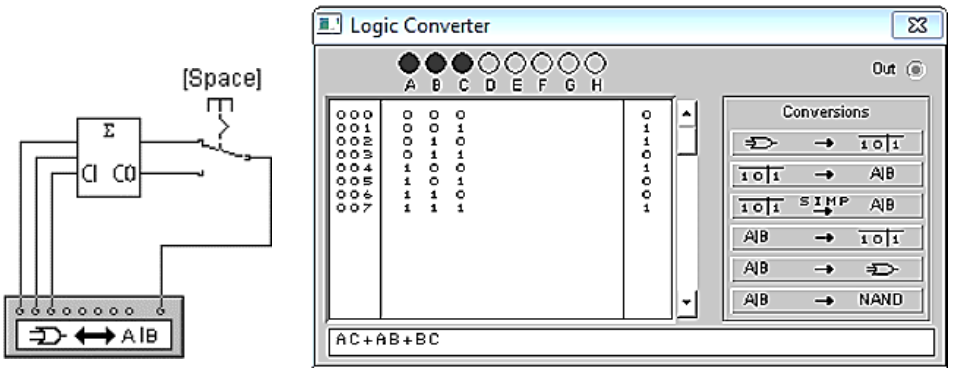
Table 1 - Table truth value of the adder

Inputs			Outputs	
A	B	Ci	S	C0

10) Draw conclusions based on the results of the analysis and synthesis about the internal structure and operating logic of the half adder.

Exercise 1.2. Research internal structure And logic functioning full adder using a logic converter and a word generator. To do this, perform the following operations:

1) Collect diagram full research adder, given on Fig. 4. At this The output of the summation result Σ in the adder is connected to the OUT terminal of the logic converter .



Rice. 4 - Scheme research complete adder

2) Repeat points 2 - 9 of the previous task.

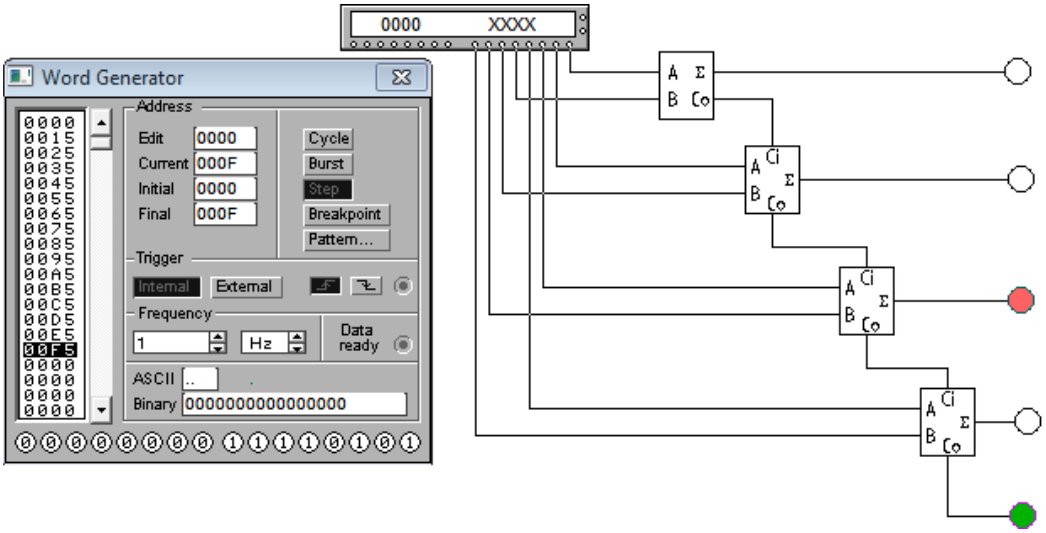
3) Based on the results of completing the listed points in the laboratory work report introduce logical expressions For synthesis adder, synthesized diagram half a leg adder V basis AND, OR, NOT, A Also received V result research truth table of a full adder.

4) Additional task: to design a full adder circuit based on half adders and to confirm its functionality using a word generator and logic probes .

5) Do it conclusions By results conducted analysis And synthesis O the internal structure and operating logic of the full adder.

Exercise 1.3. Research logic functioning 4-x discharge adder With using a word generator . To do this, follow these steps:

1) Collect diagram research 4-x discharge adder, given on rice 5.



Rice. 5 - Scheme research 4-x discharge adder

2) Program the cells of the word generator so that at some inputs of the adder the values of operand ***B*** would change from 0000 to 1111, and at the other input the code of operand ***A*** would remain unchanged, equal variant number code By module 10. IN given scheme research operand code A – 0101.

3) Set the word generator to step-by-step operation. Repeatedly press the generator's "Step" button to test the adder's logic and record all its calculation results in report table 2.

Table 2.

Code operand A	Code operand IN	Amount code	overflow

4) Do it conclusions By results conducted research principles construction and operating logic of a 4-bit adder.

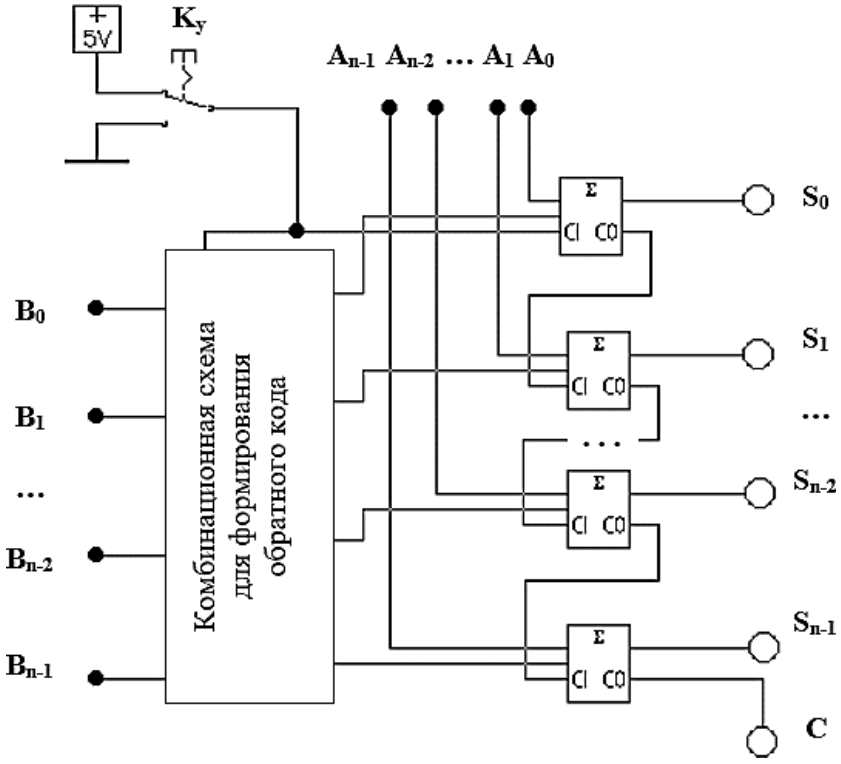
Exercise 1.4. Synthesize given adder-subtractor And conduct his research (high level).

Statement of the synthesis problem . Based on a 4-bit adder, the study of which was conducted V previous task, on one's own synthesize adder-subtractor with the capacity specified by the variant (see Table 3).

Table 3 - Options tasks For synthesis And research adder- subtractor.

Option number	Bit depth torus-subtractor sum	Second operand IN	Option number	Bit depth torus-subtractor sum	Second operand IN
1	4	5	11	4	4
2	5	10	12	5	9
3	6	25	13	6	24
4	7	49	14	7	54
5	8	105	15	8	109
6	4	3	16	4	6
7	5	11	17	5	13
8	6	27	18	6	26
9	7	56	19	7	51
10	8	117	20	8	111

Functional scheme n-bit adder-subtractor is given on rice. 6.



Rice. 6 - Functional scheme n-bit adder- subtractor

IN basis this schemes (cm. rice. 6) lies typical n-bit adder, built on basis full single-digit adders. For implementation operations subtractions With With the help of this adder, the device must contain a combinational circuit for converting the subtrahend n-bit number (negative operand) into the inverse code.

The transfer of the adder to the subtractor mode must be done by the switch Sy, which connects the logical 1 level to the input of the combinational circuit to invert the subtrahend operand And on entrance transfer Ci V younger discharge For receipt complement code of the second (subtrahend) operand. To perform the summation operation, the switch Sy connects the logic 0 level to the specified inputs, as a result, the code of the second (addend) operand does not change.

Thus, the task is synthesis consists in synthesis of a combinational circuit, forming the inverse code of the subtrahend number (operand B) and connecting it to an n-bit adder .

To display the results of summation or subtraction, connect logic probes to the outputs of the adders.

The order of synthesis and research:

1) Collect diagram given n-bit adder.

2) Determine a logical 2-way element that will ensure that when a logical 1 is applied to one of its inputs, the output will generate the inverse code for the operand supplied to the other input of this logical element.

3) Using the selected logic element, synthesize a combinational circuit that ensures the formation of the inverse code for the second (subtracted) n-bit operand arriving at its inputs.

4) Connect exits combinational schemes To informational entrances sumato-
ditch.

5) For formations operands informational entrances ***A*** And ***IN*** connect the adder-subtractor To generator words, V memory whom V hexadecimal code V younger byte to enter the values of operand ***A*** from 0 to 7 for a 4-bit adder or from $\mathbf{2^{n-2}}$ up to $\mathbf{2^{n-2}+7}$ for adders of other bit depths, and in the most significant byte the value of the second operand ***B*** , specified in table 3.

6) Check the performance of the synthesized adder-subtractor by confirming correctness logic his functioning. For this installing the device in the mode of first addition and then subtraction, and by starting the word generator in step-by-step mode, perform computational operations on operands A and B.

7) Results operations summation And subtractions bring in V table 4 V binary code.

Table 5 - Results research

Operand code A in binary view	**Operand code B in binary view**	**Amount code V in binary form**	**Difference code V binary view**

8) Do it conclusions By results conducted synthesis And research O principles of construction and logic of operation of an n-bit adder-subtractor.

Content report about work

IN In the report, please provide:

- topic And target work work ,
- practical tasks;
- designs ;
- results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, timing diagrams, etc.;
- conclusions O done work.

Control questions For preparation To report protection :

1) Scroll And characteristic combinational digital devices.
2) Characteristic principles constructions And work arithmetic adders.
3) Order research internal structures And logic functioning half-sum of the mator And complete adder With help logical converter And generator words.
4) Order research internal structures And logic functioning 4-x once in a row adder With help logical converter And generator words.

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 3

Subject: **STUDY COMBINATIONAL DIGITAL DEVICES: SCRAMBLERS AND DECODERS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of combinational digital devices using universal packages of applied computer programs;

– conduct research combinational digital devices based on their schematic models,

– synthesis of combinational digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study encoders And decoders.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study encoders And decoders.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

Under ***combinational digital device*** *(KCU)* understood digital A device that converts a set of *N* input digital signals into *M* output signals, where the state of the output signals at a given moment in time is determined by the state of the input signals at the same moment. In other words, a digital control unit (DCU) "does not remember" the history of signals arriving at its inputs. The operating rules of a DCU are determined by the Boolean functions they implement.

Implementing a control logic unit (CLU) involves selecting specific logic elements from a given set and connecting them in such a way as to ensure the dependence of digital output signals on input signals according to specified operating rules. Low-integration integrated combinational logic circuits (ILCs) are widely used in the implementation of CLUs.

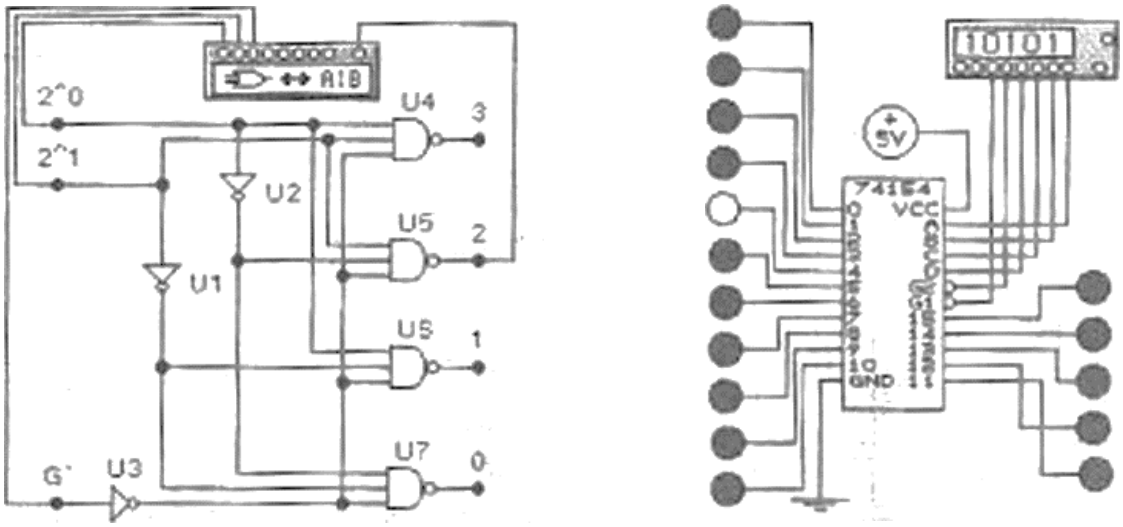
Decoders and encoders

Decoder (decoder) - combinational device With several entrances And outputs, in which certain combinations of input signals correspond to the active state of one of the outputs. A decoder is an input-inverted demultiplexer, in which the address inputs have become information inputs, and the former information input has become an enable input. Therefore, decoders are often called decoder-demultiplexers and vice versa.

Decoders in the form of serial ICs of medium integration level are widely used in information-measuring equipment and microprocessor control systems, in in particular, V quality distribution switches informational signals And synchronization pulses, for demultiplexing data and address logic in storage devices, as well as for converting binary-decimal code to decimal for the purpose of controlling indicator and printing devices.

Decoders, as standalone electronic devices, have 4, 8, or 16 outputs. If more outputs are required, decoders can be integrated into the system.

Scheme decoder 2x4 (rice. 1, A) contains three inverter U1 ... U3 And four element ZI-NE U4 ... U7; entrances $2^{\wedge 0}$, $2^{\wedge 1}$ - address, G' - entrance permissions (active level - logical zero signal); outputs 0...3 are inverse.



a) b)

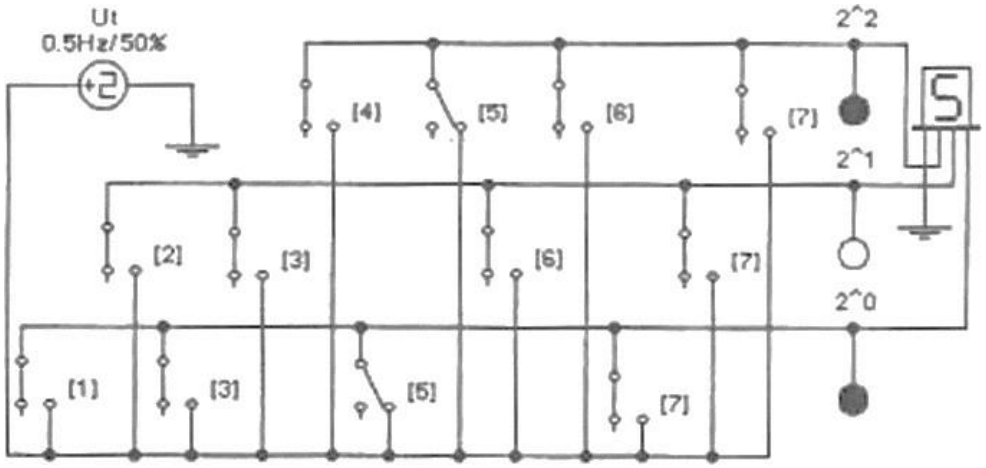
Rice. 1 - Decoder 2x4 (a) And scheme inclusion of the integrated circuit 74154 (b)

Note, What V serial IMS decoders universal type exits Always inverse , i.e. in the initial state, the signal at its outputs is a logical one. This is due to the fact that they are most often used in address selectors to select a particular device (for example, a RAM chip), in which the selection signal, as a rule, must have short level. IN quality example on rice. 1, b) given scheme inclusions torus decipherer 74154 (domestic analogue K155IDZ). This IMS has four address entrance A, IN, C, D, two entrance permissions Gl, G2 And sixteen outputs 0...15 (outputs Not straight, How designated in EWB, and inverse). In the decoder mode, 0 is supplied from the word generator to the G1, G2 inputs, and a code in the range 0000 ... 1111 is supplied to the address inputs. ***In the demultiplexer mode, one from permitting entrances, For example G1, is used V quality informational***

entrance . Informational signal V view logical 0 With this exit is distributed By I'll give you a way - out 0 ... 15 V in accordance With condition address entrances, those. modes decoder And The demul tiplexor is difficult to distinguish.

Encoders are used to encode unitary code into binary code, and also very often to convert decimal numbers into binary or binary-coded decimal code, for example, in microcalculators, in which pressing the decimal key corresponds to the generation of the corresponding binary code.

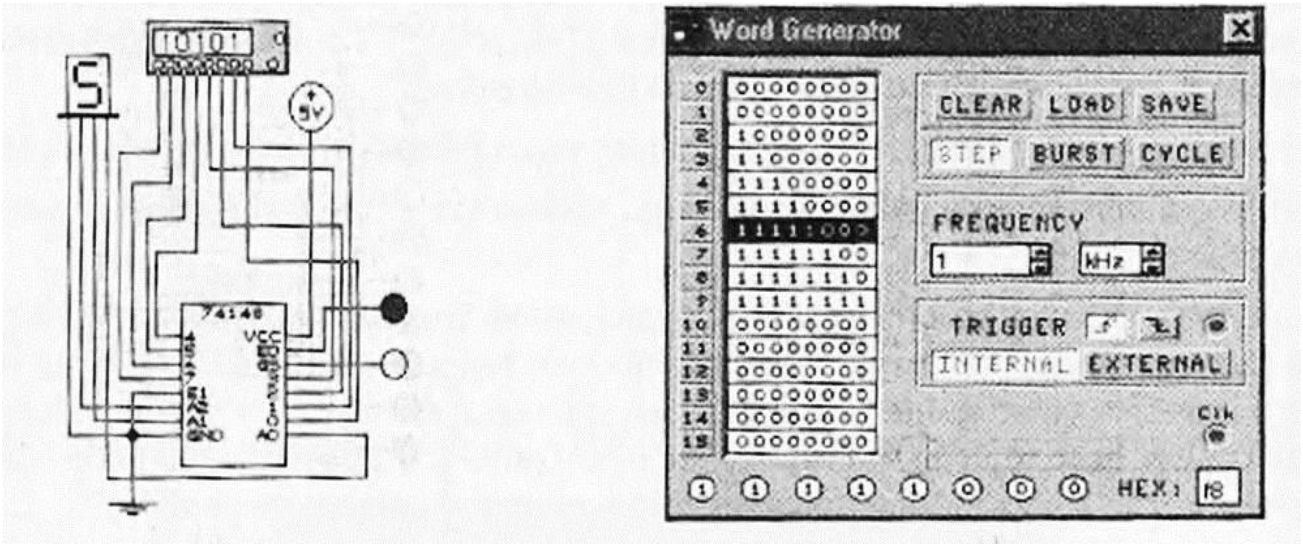
Electromechanical analog of the encoder for encoding decimal numbers 1...7 into binary code (rice. 2) contains buttons specified numbers V view single, double or built switches, controlled digital keys keyboards. State
buttons - on/off – is being installed clocked impulses survey from source of unipolar pulses **Ut** and at the output of the encoder is indicated by logical probes for binary code and an alphanumeric indicator for decimal.



Rice. 2 - Scheme electromechanical encoder

Since real keyboards can press several keys at once, in encoders is used principle priority senior discharge, those. at pressing, for example, keys 9, 5 And 2 on exit encoder will be generated code 1001, corresponding digital
9. It should be noted that encoders as a separate class of functional devices are presented V most rich TTJI series total two IMS - 74147 And 74148, and The latest integrated circuit is also available in the EWB program library. Its circuit diagram is shown in Fig. 3, a), and the operating modes of the word generator used are shown in Fig. 3, b.

Purpose conclusions IMS 74148: 0 ... 7 - entrances; A0, Al, A2 - outputs; E1 - entrance resolution ; E0, GS – outputs for cascading encoders. When modeling, it is necessary to pay attention to the implementation of the priority principle, while taking into account that all inputs and outputs are inverse (in the functional diagram of the IC in the EWB program, they are shown as straight lines).



a) b)

Rice. 3 – Circuit diagram of the integrated circuit 74148 (a)
And panel generator words With installations For tests (b)

Content practical work, performed students during the lesson

1. Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

– program circuit design modeling Electronics Workbench EWB 5.12.

2. Tasks For execution laboratory work:

Base level:

1) Synthesize and investigate the operating logic of a 3x8 decoder using a logic converter and a word generator

2) To investigate the operating logic of the 4×16 decoder, implemented in the form of an IMS 74154 (K155ID3) using a word generator.

3) Synthesize And research logic functioning encoder 8×3 With using a logical converter and a word generator.

4) Research logic functioning encoder 8×3, realized V view IMS 74148 (KM555IV1) using a word generator.

Increased level:

5) Synthesize a circuit fragment encoder keyboards And explore logic its functioning.

3 Order execution of work:

Task 1. Synthesize and investigate the operating logic of a 3x8 decoder With help logical converter And generator words . For this complete the following operations:

1) Open the logic converter, activate terminals A, B and C by clicking on them with the cursor.

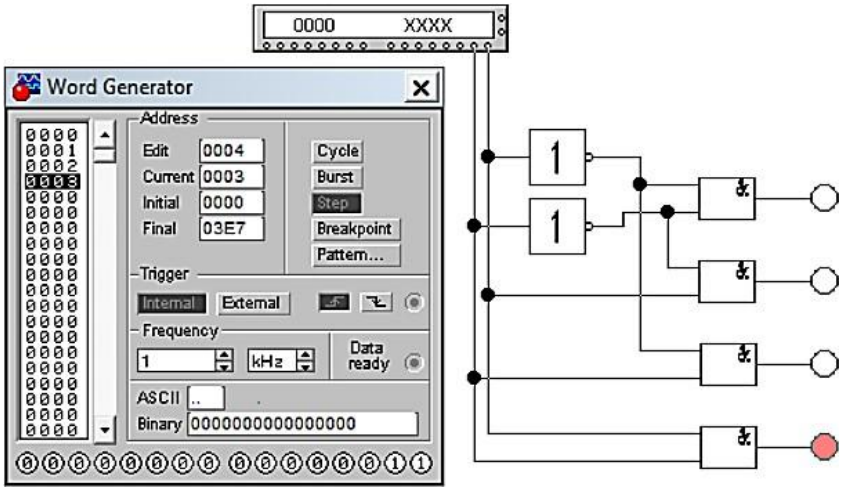
2) In the truth table that appears on the screen, make changes so that the output column contains “1” in the row with address 000, and the remaining rows of the column should contain “0”.

3) Click display button logical (Boolean) functions, By which synthesize Part schemes decoder, which will reply for activation zero exit, those. for the appearance of a logical one at this output, provided that logical zeros are present at all three inputs. Include part of the circuit in the report.

4) Sequentially repeat the actions for lines with addresses 001, 002, etc. up to 007, defining logical functions by which to similarly synthesize other parts of the decoder, responsible for activating the first, second, and so on seventh outputs.

5) IN report display diagram decoder, which necessary minimize, removing unnecessary inverters.

6) Check the operation of the synthesized decoder circuit using a word generator and logic probes, connecting them to the decoder outputs, for example, as shown in Fig. 4. To do this, set a cycle from 0000 to 0007 in the word generator, in which to write the corresponding codes.

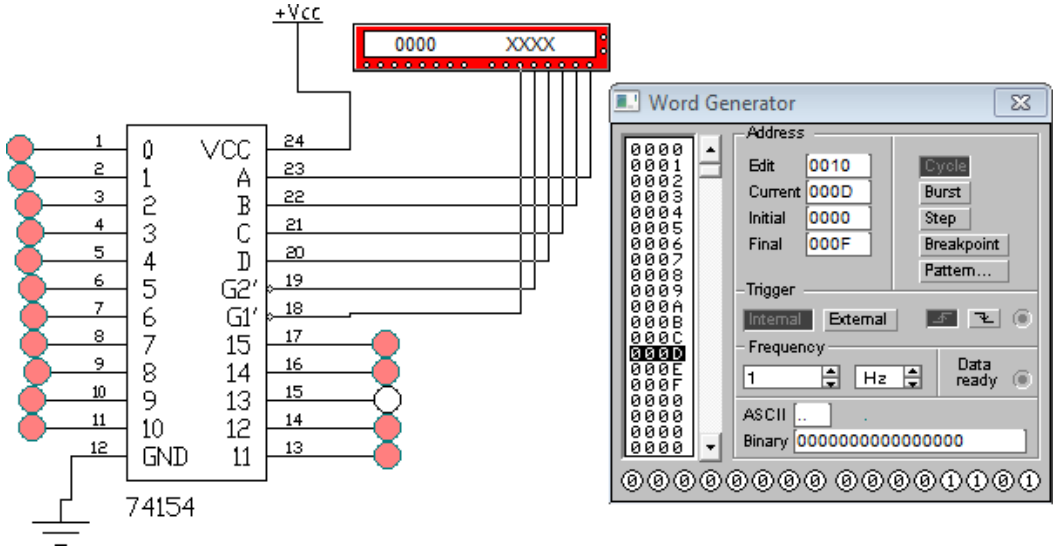


Rice. 4– Example schemes research decoder 2x4

7) Do it conclusions By results conducted research O principles construction and logic of operation of the synthesized decoder.

Exercise 2. Research logic functioning decoder 4×16, implemented in the form of an IMS 74154 (K155ID3) using a word generator. To do this, perform the following operations:

1) On the toolbar, click the Digital button, in the context-sensitive menu that opens, select the 741xx button and drag it onto the EWB program working field, select the 74154 microcircuit for this purpose. Assemble the research circuit as shown in Fig. 5.



Rice. 5 – IMS connection diagram 74154 (K155ID3)

2) Bring in V report By laboratory work table truth microcircuits 74154. Determine the function of inputs G1` and G2`.

3) For research logic functioning decoder ask V generator words cycle from 0000 to 000F cell in which to write the corresponding codes.

4) Launch generator words With clock frequency 1 Hz, How shown on rice. 14, conduct an analysis of the operating logic of the 4×16 decoder.

5) Do it conclusions By results conducted research O principles construction , operation and logic of the 4×16 decoder.

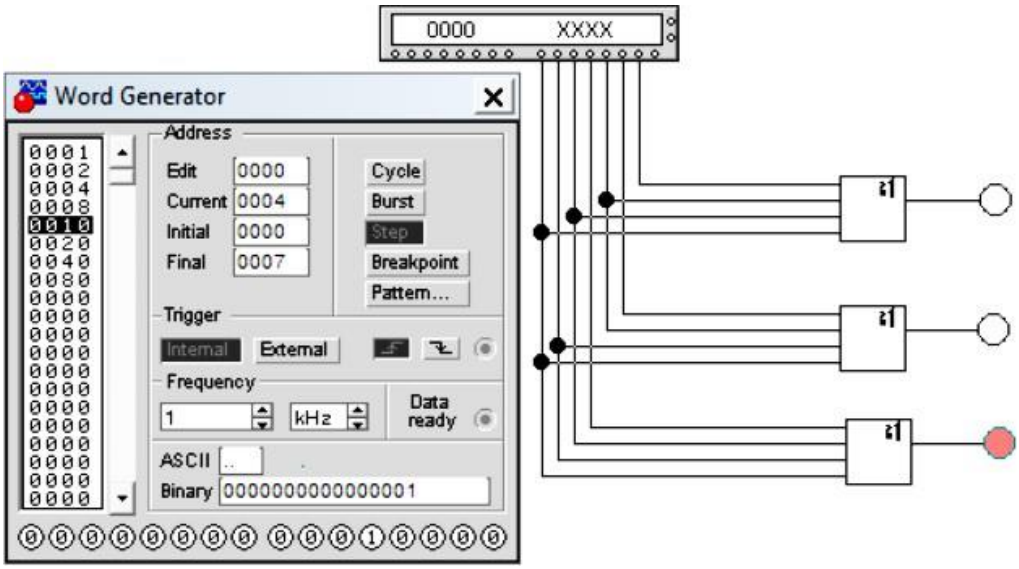
Task 3. Synthesize and investigate the operating logic of an 8x3 encoder With help logical converter And generator words. For this complete the following operations:

1) Bring in V report By laboratory work table truth encoder 8×3, having 8 unitary inputs ***x*** and 3 binary outputs ***Y*** .

2) On basis tables truth make up logical functions V view perfect disjunctive normal forms (PDNFs) for each output binary digit of the encoder by writing in logical units. For example, for the least significant digit, the logical function will be:

$$Y_0 = x_1 + x_3 + x_5 + x_7 .$$

3) Synthesize on basis received logical functions diagram encoder 8×3 using standard logic gates. An example is shown in Fig. 6.



Rice. 6 - Scheme research encoder 3 x 8

4) Collect diagram encoder 8×3 V program EWB And check her performance.

5) Conduct a study of the logic of the encoder operation using a generator words V step by step mode. For what V cells generator With 0000 By 0007 write down sequentially codes 0001, 0002, 0004, 0008, 0010, 0020, 0040 and 0080, which form a unitary code at the output terminals of the word generator.

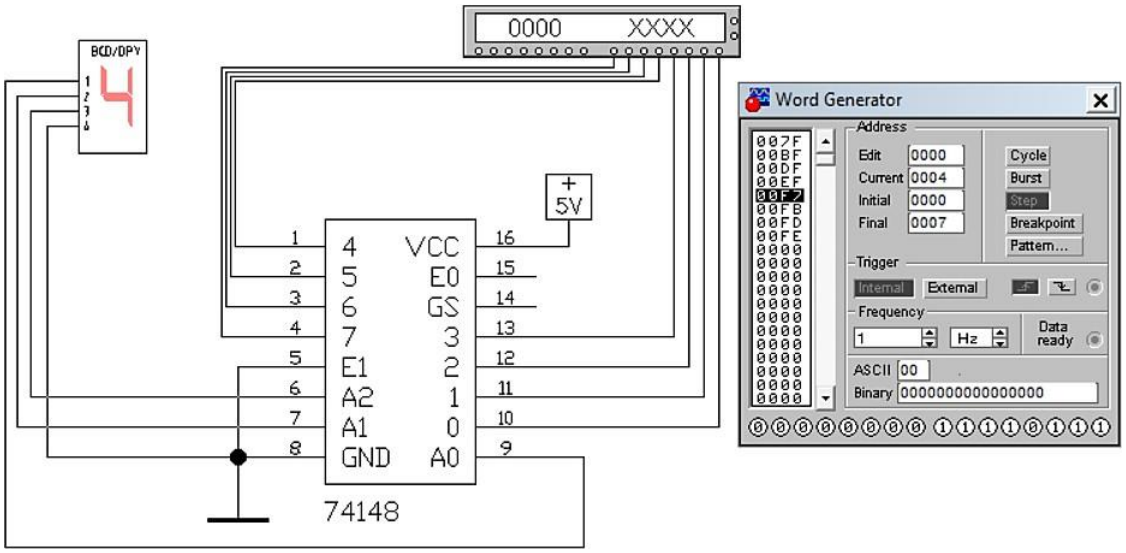
6) Do it conclusions By results conducted research O principles construction , operation and logic of the 8x3 encoder.

Exercise 4. Research logic functioning encoder 8×3, implemented in view IMS 74148 (KM555IV1) With help generator words. For this complete the following operations:

1) On the toolbar, click the Digital button, in the context-sensitive menu that opens, select the 741xx button and drag it onto the EWB program working field, select the 74148 microcircuit for this purpose. Assemble the research circuit as shown in Fig. 7, using the seven-segment indicator with a decoder, located in the Indicators panel, to display the output binary code .

2) Write down truth table encoder 8×3 V inverse view.

3) When recording unitary code in the word generator should take into account, that all the entrances and you move - inverse, Although on functional scheme IMS 74148v program EWB They are shown as straight lines. In this regard, set up a cycle in the word generator from cell 0000 to cell 0007, in which write down sequentially next codes: 007F, 00BF, 00DF, 00EF, 00F7, 00FB, 00FD, 00FE.



Rice. 7– Scheme inclusions IMS 74148 (KM555IV1)

4) Start the word generator with a clock frequency of 1 Hz, analyze the logic of the 8x3 encoder operation.

5) Do it conclusions By results conducted research O principles construction , operation and logic of the 8x3 encoder, implemented on the 74148 IC (KM555IV1).

Task 5. Synthesize a fragment of a keyboard encoder circuit and investigate the logic of its operation.

Production tasks synthesis : Synthesized fragment encoder keyboards must provide encoding three symbols, given By option (cm. table 6) V in lowercase and uppercase. Encode using KOI-8 code (see Table 7). Design the encoder fragment circuit using 8-input OR elements. Use the Shift key to enter uppercase characters.

Table 6 - Table task options

Option number	**Symbols**	**Option number**	**Symbols**
1.	out	2.	beam
3.	Boer	4.	fur
5.	elm	6.	prostrate
7.	Goal	8.	wholesale
9.	smoke	10.	pouf
11.	ruff	12.	roar
13.	bug	14.	catfish
15.	pharynx	16.	shooting range

17.	Name	18.	mustache
19.	whale	20.	hair dryer

Table 7 – Fragment of the KOI-8 encoding table for Cyrillic symbols in hexadecimal form.

symbol	code	symbol	code	symbol	code	symbol	code
yu	00	p	10	Yu	20	P	30
A	01	I	11	A	21	I	31
b	02	r	12	B	22	R	32
c	03	With	13	C	23	S	33
d	04	t	14	D	24	T	34
is	05	in	15	E	25	In	35
f	06	f	16	F	26	F	36
g	07	in	17	G	27	In	37
x	08	h	18	X	28	B	38
and	09	y	19	And	29	y	39
y	0A	h	1A	Y	2A	Z	3A
k	0B	w	1B	K	2B	Sh	3B
l	0C	eh	1C	L	2C	E	3C
m	0D	sch	1D	M	2D	SCH	3D
n	0E	h	1E	N	2E	Ch	3E
O	0F	ъ	1F	ABOUT	2F	Ъ	3F

The order of synthesis and research:

1) Write a table of correspondence for the given characters in the lowercase and in capital form. An example for the "noise" symbols is given in Table 8.

Table 8 - Conformance table for symbols w, y, m in binary code KOI- 8

Symbol	**Keys**	**Hexadecimal code**	**Binary code**							
			Y 7	**Y 6**	**Y 5**	**Y 4**	**Y 3**	**Y 2**	**Y 1**	**Y 0**
sh	sh	1B	**0**	**0**	**0**	**1**	**1**	**0**	**1**	**1**
Sh	sh i Shift	3B	**0**	**0**	**1**	**1**	**1**	**0**	**1**	**1**
in		15	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**
In	in andShift	35	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**
m		0D	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**1**
M	m and Shift	2D	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**1**

From tables it is visible, What pressing lowercase symbol "sh" should call appearance logical 1 on fourth, third, first And zero discharges encoder, A at pressing for the capital letter "Ш" the logical 1 will also additionally appear in the fifth digit of the code.

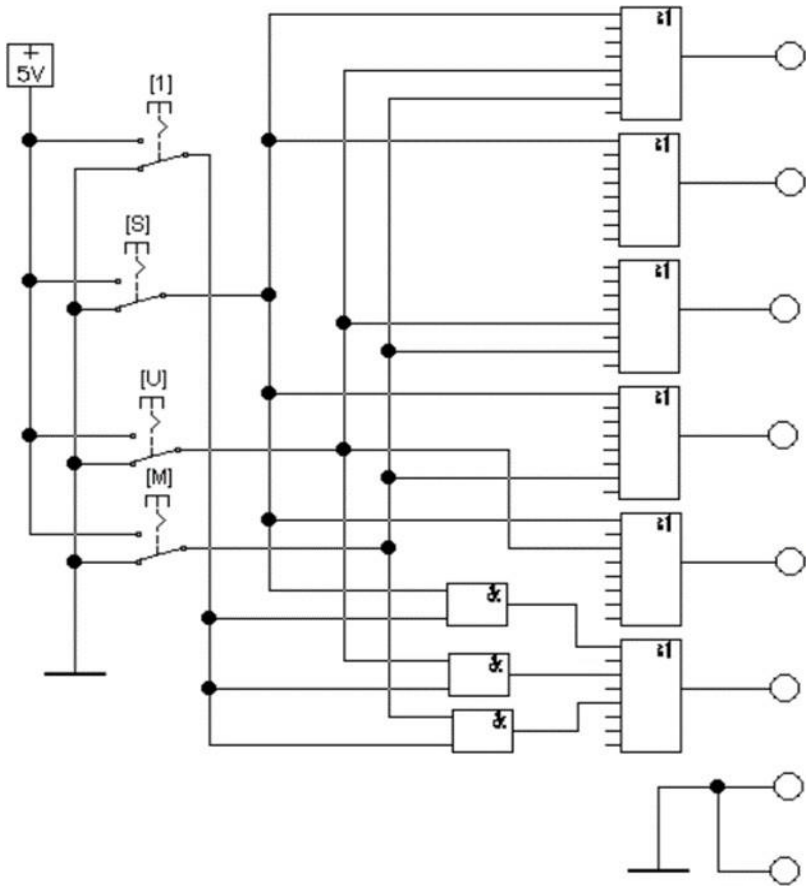
2) Taking advantage of table, produce unification logical 1, incoming With pressed keys, using elements OR for each digit of the output code. For example, logical 1 V younger discharge **Y 0** is being formed at pressing any from three keys, A logical 1 in the next digit **Y 1** is formed by pressing only one of these keys "sh".

From the analysis of the table it is clear that the two most significant digits of the output code **Y 7** and **Y 6** always have logical 0, i.e. do not depend on the input code.

Some peculiarity is observed in the fifth digit - a logical 1 appears with an additional condition, those. at pressing keys Shift And one from given keys. This

means, What For formations logical 1 V this case necessary use the AND element that allows this condition to be met.

3) Compose principled diagram For given encoder. Example schemes The cipher for encoding the symbols ш, у and м is shown in Fig. 8. The Shift key in this diagram is switched by button 1



Rice. 8 - Scheme fragment encoder keyboards For symbols w, mind

4) Conduct study logic functioning synthesized fragment of the keyboard encoder.

5) Do it conclusions By results conducted research O principles construction , operation and logic of the keyboard encoder.

4. Content report about work

IN In the report, please provide:

– topic And target work work ,

– practical tasks;

– designs ;

– results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, timing diagrams, etc.;

– conclusions O done work.

5. Control questions For preparation To protection report:

1) Scroll And characteristic combinational digital devices.

2) Characteristic principles constructions And work decoders And encoders.

3) Order synthesis And research logic functioning decoder 3x8 With using a logical converter and a word generator.

4) Order research logic functioning of the decoder 4x16, implemented in the form of an IMS 74154 (K155ID3) using a word generator.

5) Order synthesis And research logic functioning encoder 4x2 With using a word generator.

6) Order research logic functioning encoder 8x3, realized in the form of IMS 74148 (KM555IV1) using a word generator.

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 14

Subject: **STUDY COMBINATIONAL DIGITAL DEVICES: MULTIPLEXERS AND DEMULTIPLEXERS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of combinational digital devices using universal packages of applied computer programs;

– conduct research combinational digital devices based on their schematic models,

– synthesis of combinational digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study multiplexers And demultiplexers.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study multiplexers And demultiplexers.	55 min
Final Part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENTS OF PRACTICAL WORK

Brief theoretical or reference and information materials

Under ***combinational digital device*** *(KCU)* understood digital A device that converts a set of *N* input digital signals into *M* output signals, where the state of the output signals at a given moment in time is determined by the state of the input signals at the same moment. In other words, a digital control unit (DCU) "does not remember" the history of signals arriving at its inputs. The operating rules of a DCU are determined by the Boolean functions they implement.

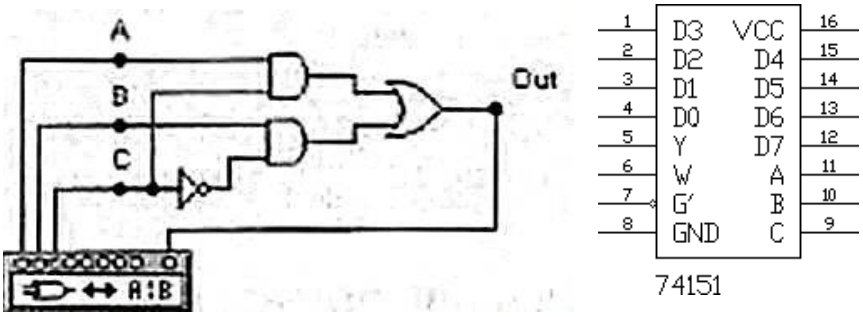
Implementing a control logic unit (CLU) involves selecting specific logic elements from a given set and connecting them in such a way as to ensure the dependence of digital output signals on input signals according to specified operating rules. Low-integration integrated combinational logic circuits (ILCs), which form the basis of digital electronics, are widely used in the implementation of CLUs.

Multiplexers And demultiplexers

Multiplexers (*from English multiplex – multiple*) are used for switching in given in order signals, incoming With several input tires on one day off. A multiplexer may have, for example, 16 inputs and 1 output. This means that if 16 digital signal sources – serial digital signal generators – are connected to these inputs, words, That bytes from any from generators Can transmit on the only one Output. To select any of the 16 channels, it is necessary to have 4 selection inputs ($2^{x4} = 16$), to which the channel's binary address is fed. Thus, to transmit data from channel number 9, the code 1001 must be set at the selection inputs. For this reason, multiplexers are often called selectors or selector-multiplexers.

Multiplexers are used , for example, in microprocessors (MP) to output to one And those same conclusions MP addresses And data, What allows significantly reduce general number of microcircuit pins; in microprocessor control systems, multiplexers are installed at remote sites to enable the transmission of information over a single communication line from several sensors installed on them.

Fig. 1, a) shows the circuit diagram of a two-channel multiplexer consisting of OR, HE elements and two AND elements, and Fig. 1, b) shows the functional circuit diagram of the IMS 74151 (K155KP7) eight-channel selector-multiplexer, the terminals of which have the following purpose: D0 ... D7 - entrances; GND — general; VCC - voltage nutrition +5 IN; G' - enable input (active level - low); Y, W - direct and inverse outputs; A, B, C - address inputs 2°, 2^{1} and 2^{2}.



a) *b)*

Fig. 1 – Schematic diagrams of a two-channel multiplexer (a) and IMS 74151 eight-channel (b) multiplexer

From the results of modeling a two-channel multiplexer using a logical converter (rice. 2) it is visible, What his day off signal is described Boolean expression OUT = BC' + AC, i.e. signal from channel A passes at the exit at the address input C = 0, and from channel B – at C = 1, which corresponds to the logic of the multiplexer operation.

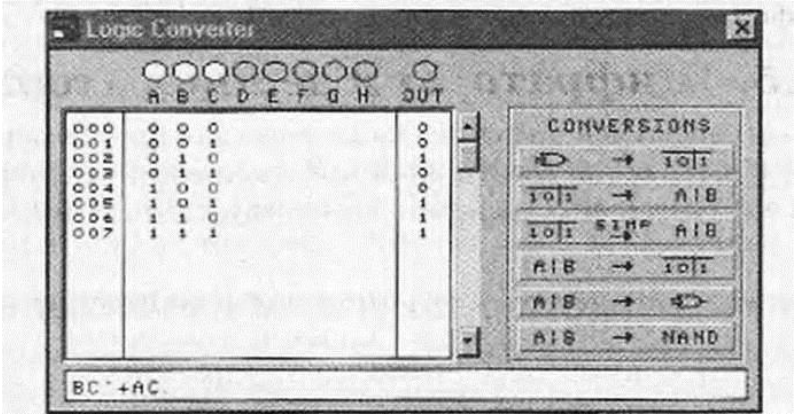
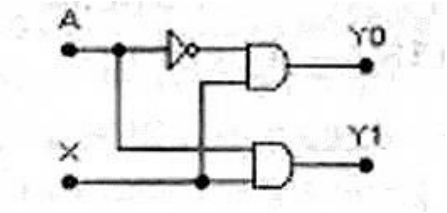


Fig. 2 – Results of modeling a two-channel multiplexer Demultiplexers V functional

relation opposite multiplexers.

WITH their help signals With one informational entrance are distributed V required sequences across several outputs. Selection of the desired output bus, as in a multiplexer, is ensured by setting the corresponding code on the address inputs. With ***m*** address inputs, the demultiplexer can have up to 2^m outputs.

The operating principle of the demultiplexer is explained using the diagram in Fig. 3, which shows: X - informational entrance, A - entrance addresses, Y0, Y1 outputs. Scheme contains two elements AND, one element NO. From rice. 27 not difficult notice, What at A = 0 signal With information input is transmitted to the output Y0 and when A = 1 – to the output Y1. It should be noted that the industry demultiplexers How such Not are being released, because mode Demul - Tiplexor Maybe be implemented How private happening V others devices, For example, V decryptors, which were discussed earlier.



Rice. 3 - Scheme two-channel demultiplexer

Content practical work, performed students during the lesson

Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

– program circuit design modeling Electronics Workbench EWB 5.12.

Tasks For execution laboratory work:

Base level:

1) Synthesize And research logic functioning 4-x channel Multiplexing garbage using a logic analyzer.

2) Research logic functioning eight-channel selector-multiplexer, implemented in the form of an IMS 74151 (KM155KP7) with the help of a logic analyzer.

3) Synthesize and investigate the operating logic of a 4-channel demultiplexer using a logic analyzer.

Increased level:

4) Synthesize And research logic functioning given By variant of the multiplexer on the IC.

Order execution works:

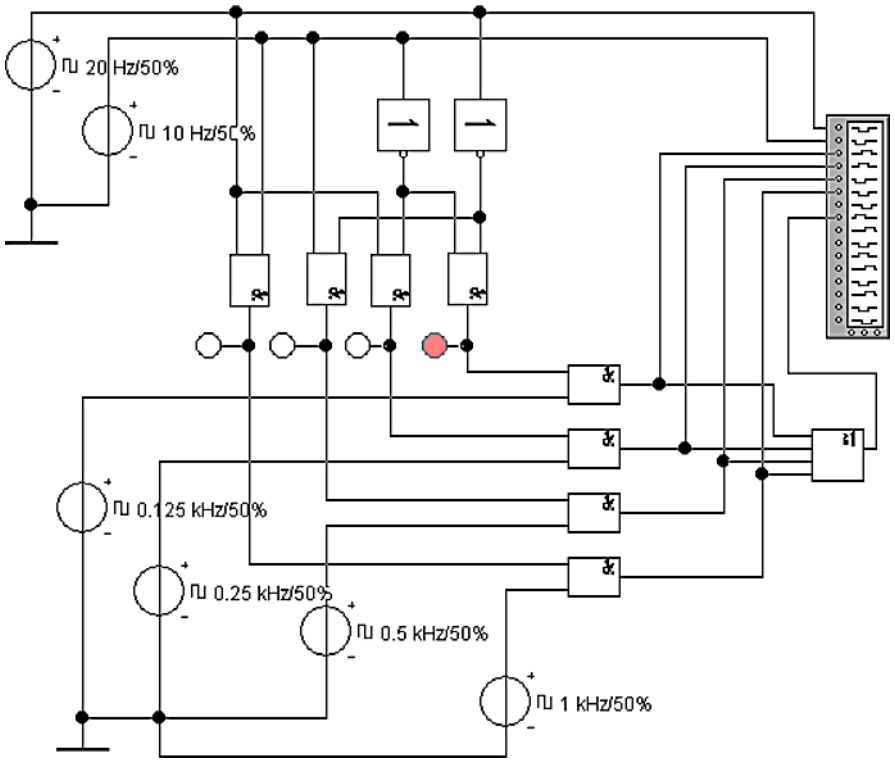
Exercise 1. Synthesize And research logic functioning 4-x channel multiplexer using a logic analyzer . To do this, perform the following steps:

1) Compose table conformity (truth) 4-x channel single-digit multiplexer , include it in the lab report.

2) Conduct analysis structures 4-x channel multiplexer, from whom follows, that the multiplexer must consist of 4 keys (AND logic elements), a 4-input OR element and a 2x4 decoder that generates a unitary code that ensures the inclusion of one of the 4 keys.

3) Collect diagram research 4-x channel multiplexer, given on rice.

4. Clock generators with frequencies of 0.125 kHz, 0.25 kHz, 0.5 kHz, and 1 kHz simulate data transmission channels. Clock generators with frequencies of 10 Hz and 20 Hz provide automatic address switching for channel switching. Logic probes are used to indicate the number of the switched channel.



Rice. 4 - Scheme research 4-x channel single-bit multiplexer

4) Double click open logical analyzer And launch work circuit under study. Configure the logic analyzer by setting the time base (clocks per division) to 16 or 32.

5) Using a logic analyzer and logic probes displaying the addresses of switched channels, analyze the operating logic of the synthesized multiplexer. After stop logical analyzer view on his On the screen, you can see timing diagrams of the input signals for each channel and the output signals in the common bus, using horizontal scrolling if necessary.

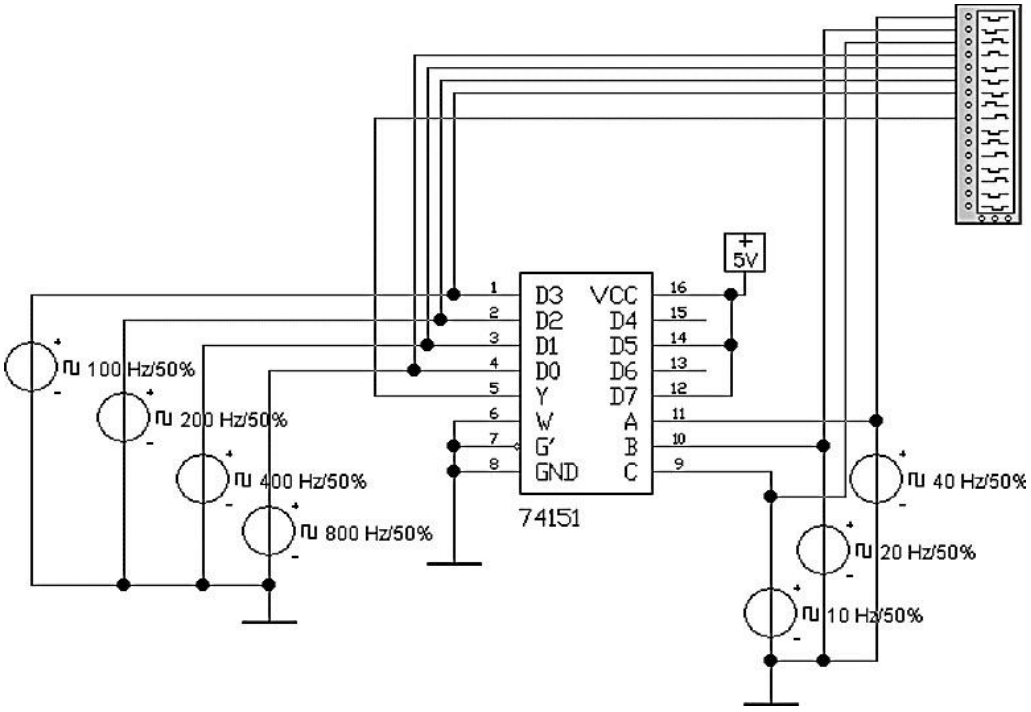
6) Display the logic analyzer timing diagrams in the lab report .

7) Do it conclusions By results conducted research O principles construction , operation and logic of functioning of a 4-channel single-bit multiplexer.

Task 2. Investigate the operating logic of an eight-channel selector-multiplexer implemented as a 74151 (KM155KP7) IC using a logic analyzer . To do this, perform the following steps:

1) Compose table conformity (truth) 8th channel single-digit multiplexer , include it in the lab report.

2) On the toolbar, click the Digital button, in the context-sensitive menu that opens, select the 741xx button and drag it onto the EWB program working field, select the 74151 microcircuit for this purpose. Assemble the research circuit as shown in Fig. 5, using a logic analyzer to display timing diagrams.



Rice. 5– Scheme inclusions IMS 74151 (KM155KP7)

In the circuit shown in Fig. 5, clock generators with frequencies of 100 Hz, 200 Hz, 400 Hz and 800 Hz simulate data transmission at different speeds through channels D3, D2, D1 And D0 respectively. By channels D4 - D7 are transmitted logical potentials. Clock generators impulses With frequencies 10 Hz, 20 Hz And 40 Hz provide automatic address switching for circuit switching.

3) Double click open logical analyzer And launch work circuit under study. Configure the logic analyzer by setting the time base (clocks per division) to 16 or 32.

4) Using a logic analyzer, analyze the logic of the synthesized device multiplexer. After stop logical analyzer view on on his screen temporary diagrams addresses, input signals By to everyone channel And weekend signals in the common bus, using horizontal scrolling if necessary.

5) Determine what data is transmitted through each channel of the multiplexer. Display the logic analyzer timing diagrams in the lab report.

6) Do it conclusions By results conducted research O principles construction , work And logic functioning 8th channel single-digit multiplexer, implemented on IC 74151 (KM155KP7).

Exercise 3. Synthesize And research logic functioning 4-x channel demultiplexer using a logic analyzer . To do this, perform the following steps:

1) Create a table of correspondence (truth) for a 4-channel single-bit demultiplexer and include it in the laboratory report.

2) Conduct an analysis of the structure of a 4-channel demultiplexer, from which it follows that the demultiplexer must consist of 4 keys (logical AND elements) and a 2x4 torus decoder that generates a unitary code that ensures the opening of one of the 4 keys.

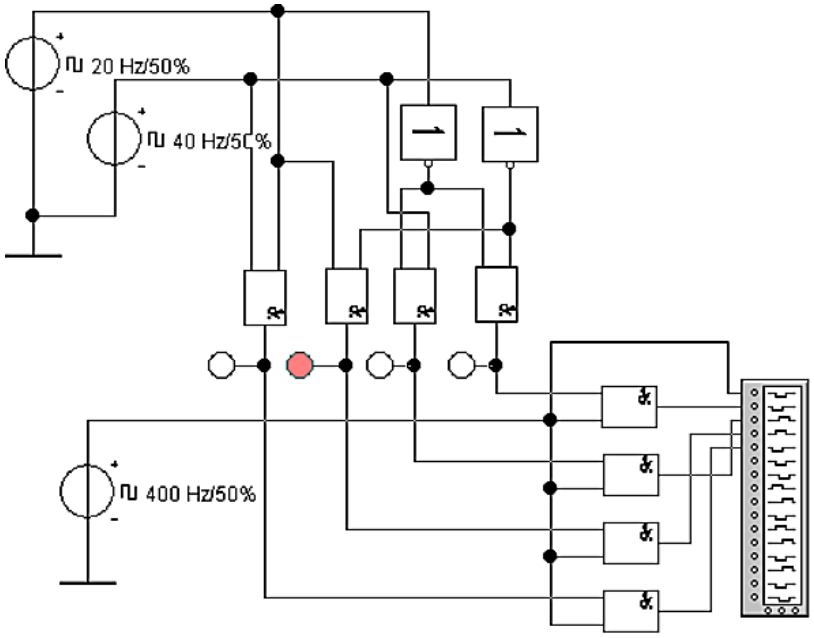
3) Collect diagram research 4-x channel demultiplexer, given on rice.

6. The 400 Hz clock generator simulates the data transmission channel (common bus). The 10 Hz and 20 Hz clock generators provide automatic switching addresses For switching channels. Logical samples are intended to determine the number of the switched channel.

4) Double click open logical analyzer And launch work circuit under study. Configure the logic analyzer by setting the time base (clocks per division) to 16 or 32.

5) Using a logic analyzer and logic probes displaying the addresses of the switched channels, analyze the operating logic of the synthesized demultiplexer. After stopping the logic analyzer, view the time data on its screen. diagrams input signals V general tire And weekend signals By to everyone the selected channel, using horizontal scrolling if necessary.

6) Determine what data is transmitted over each demultiplexer channel. Display the logic analyzer timing diagrams in the lab report.



Rice. 6 - Scheme research 4-x channel 1 discharge demultiplexer

7) Do it conclusions By results conducted research O principles construction , operation and logic of functioning of a 4-channel single-bit demultiplexer.

Task 4. Synthesize and investigate the operating logic of a given IC multiplexer (high level).

Table 9 – Options for synthesizing multiplexers

Option	**Exercise**	**Option**	**Exercise**
1.	2-x channel 4-x discharge on IMS 74257 (K155KP11)	2.	3-channel single-bit on IC 74151 (K155KP15)
3.	2-x channel 4-x discharge on IMS 74258 (K155KP14)	4.	5th channel single-digit on IMS 74151 (K155KP15)
5.	4-channel 4-bit on IMS 74257 (K155KP11)	6.	6th channel single-digit on IMS 74151 (K155KP15)

7.	4-x channel 4-x discharge on IMS 74258 (K155KP14)	8.	7th channel single-digit on IMS 74151 (K155KP15)
9.	4-channel 2-bit on IMS 74153 (K155KP2)	10.	5th channel single-digit on IMS 74150 (K155KP1)
11.	4-channel 2-bit on IMS 74253 (K155KP12)	12.	6th channel single-digit on IMS 74150 (K155KP1)
13.	8- channel single-bit on the 74153 IC (K155KP2)	14.	7th channel single-digit on IMS 74150 (K155KP1)
15.	8- channel single - bit on IMS 74253 (K155KP12)	16.	9th channel single-digit on IMS 74150 (K155KP1)
17.	16-input single-digit multiplexer on the 74150 IC (K155KP1)	18.	3-x channel two-digit on IMS 74153 (K155KP2)
19.	4-channel 2-bit on IMS 74352	20.	3-x channel two-digit on IMS 74253 (K155KP12)

Recommendations By synthesis And research :

1) Compose table conformity (truth) given multiplexer, bring in her in the lab report.

2) On basis tables truth produce development schemes given multiplexer .

3) When synthesizing a multi-bit multiplexer in order to distinguish data related to To various discharges, install V generators, simulating transmission data, different porosity, For example, For one discharge porosity 2 (50%), A For another category – 4 (25%).

4) At synthesis of multiplexers with a number of channels that are not multiples of 2, it is necessary to synthesize a combinational circuit that will reduce the number of addresses (quantity) of channels to a given number.

5) The study of the operating logic of a given multiplexer is carried out using a logic analyzer.

6) IN report By laboratory work introduce synthesized circuit multiplex of the sora, its truth table, timing diagrams in a logic analyzer demonstrating the logic of its operation.

7) IN conclusion do conclusions By results conducted research O principles of construction, operation and logic of functioning of a given multiplexer.

Content report about work

IN In the report, please provide:

– topic And target work work ,

– practical tasks;

– designs ;

– results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, timing diagrams, etc.;

– conclusions O done work.

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 15

Subject: **STUDY TRIGGERS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of sequential digital devices using universal packages applied computer programs;

– conduct study sequential digital devices on basis their circuit models,

– synthesis of sequential digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

TRAINING AND MATERIAL SUPPORT:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study triggers.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study triggers.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENT LABORATORY CLASSES

Brief theoretical or reference and information materials

Sequential or accumulating nodes of digital devices are nodes that contain memory elements, specifically triggers. Two types of accumulating nodes can be distinguished: registers and counters.

Register - accumulating knot, designed For reception, storage, transformations And issuance binary information. ***Counter*** - accumulating knot, designed for counting events, counting pulses arriving at the counting input.

Among sets input signals accumulating node Can highlight information , control, synchronization . Under the influence of input signals, the node is capable fulfill that microsurgery, on which He configured preliminary filing a certain combination of control signals.

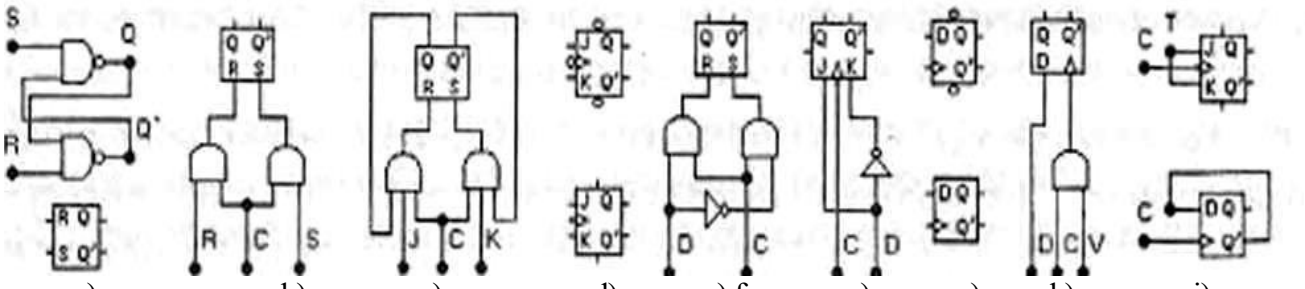
Actually ***microsurgery is ending change states node*** synchronously under the action of a synchronization signal or asynchronously when a signal is applied to the asynchronous input of the preliminary installations node V certain state. Executed knot microoperations can be any, which required For execution given algorithm. That's why often a counter, For example, simultaneously Maybe accept parallel information in All bits, that is, to perform a micro-operation characteristic of the register, and vice versa, the register is designed in such a way that it can also perform the function of counting the number of pulses. That is, both the functions of a register and a counter can be implemented in a single unit. Complex micro-operations can demand attracting additional combinational nodes for implementation microoperations, on which Not calculated used chip register or counter.

Managers signals allow choose mode work node , That There is ask the required micro-operation. The micro-operation itself is completed at the moment the clock signal is triggered. or V moment parish signal on asynchronous entrance node. If knot contains information inputs for parallel reception of information, then they can be numbered in order or With taking into account their weight. Weekend chains node can be organized By scheme With three states, which will require an additional input to control the output amplifiers.

Triggers

Triggers are widely used in many units of electronic equipment as independent products or V quality basic elements For constructions others, more complex devices (counters, registers, storage devices). ***They are the simplest sequential devices*** , common property which is the ability to remain for a long time in one of two possible stable states, which are recognized by the value of their output signals.

IN the simplest execution trigger represents by yourself symmetrical a structure of two OR-NOT or AND-NOT logic elements, covered by a crossed positive feedback communication. Trigger on elements AND-NOT And his "integral" analogue V program EWB shown on rice. 1, A). ***Such trigger they call symmetrical*** (used Also names - bistable cell, memory cell, asynchronous RS trigger); ***it has two stable states*** , which are provided for check connections exit each element with one of the inputs of another. **Free *inputs*** are used for control and ***are called*** **information *or* logical** . One of the outputs of the trigger is called direct (due to symmetry schemes them Maybe be any) And denote letter Q, A another - inverse And denoted by $\underline{Q}$ (in EWB – Q '). The state of the trigger is often identified with the signal at the direct output , i.e. they say that the trigger is in in a single state, if Q=1, and Q ' =0, and in zero if Q=0, and Q ' =1.



a) b) c) d) e) f) g) h) i)

Fig. 1 – Trigger circuits

Change states trigger is produced external signals ; this process called switching, flip-flopping, overturning, etc. The start of the flip-flop of the trigger (see Fig. 1, a) occurs with the arrival of a positive voltage drop at the input of the closed element. ***Informational entrance*** , By to whom trigger is being installed V single state (Q=1; Q ' =0), ***they call single or S-input*** (from English set - installation), A V zero (Q=0, Q ' =1) – ***zero or R-input*** (reset). ***The combination of input signals*** S=R=0 ***is called*** neutral or ***storage mode*** – in this mode, the trigger stores the state it was brought to in the previous clock cycle. If a one signal is applied to one of the inputs, keeping a zero signal on the other, the trigger will take a state that is uniquely determined by the combination of input signals. If switching signals are applied to both inputs simultaneously (combination S=R=1), logical zeros will appear at both outputs and the device will lose properties trigger; That's why such ***combination they call*** **prohibited** , (undefined).

More complex schemes triggers contain considered RS trigger And control devices that are combination devices that transform input information into a combination of signals, under the influence of which the trigger itself takes one of two stable states.

The main role in the formation of the properties of the trigger system belongs to the control device. IN schematic relation devices management They are distinguished by a great variety . ***By changing the control device circuit and the methods of its connections to the memory cell*** (RS trigger), ***triggers with different functional properties can be obtained*** .

Entrance signals V dependencies from performed roles ***are subdivided on three cathe-mount ains*** :

- informational (logical),
- preparatory (permissive),
- executive (command).

Signals on informational entrances determine information , which will write-sana in the trigger. The role of preparatory and executive signals is auxiliary: with their help Can V necessary moment interrupt action trigger or groups triggers, saved information on exit. ***Executive signals set*** the moment reception input information trigger And serve For synchronization work rows devices, forming functional knot. ***These signals often So And they call - synchronizing or tactfully*** .

Entrances trigger By character input signals are subdivided Also on three by category :

- informational (logical),
- presets (preparatory),
- clock (synchronizing).

Informational entrances there are at everyone triggers, Then How preparatory And so they may be absent.

The trigger type is determined by the functional relationship between the input and output signals , which can be expressed in different ways: timing diagrams, characteristic equations, tables external transitions (tables states), transition graphs.

According to the method of entering information, triggers are divided into **asynchronous** ***and*** **synchronous** . U ***asynchronous triggers there are only informational (logical) inputs*** ;

An example of such a trigger is the RS trigger in Fig. 1, a. ***The main disadvantage of - asynchronous triggers is*** unsatisfactory noise immunity under conditions of possible signal time delays (the so-called signal races or competitions). ***This disadvantage is eliminated in synchronous triggers*** by using an additional command signal, which is fed to the synchronizing (clocking) input C (rice. 1, b). ***Synchronizing signals are being produced special generator***

clock pulses , which set the frequency of information change at discrete moments in time and thus the general rhythm of operation of most hardware components. In this case, the reversal (triggering) synchronous triggers is happening only at participation clock pulses whose duration is much shorter than their period. The rest of the time, the trigger does not respond to input signals, nor to interference of various origins.

IN dependencies from Togo, Which parameter input signals use For Information recording triggers are divided into three categories :

- with static management recording (controlled By level input signal),
- With dynamic management (controlled By front or straight away),
- two-stage.

For asynchronous triggers, the signals at the information inputs serve as control signals , for synchronous triggers, the clock pulse serves as control signals. ***A trigger with static control is triggered V moment*** , When input signal reaches threshold level; For Synchronous triggers, this means that during the clock pulse, a change in signals at the data inputs causes new triggerings, i.e., synchronous triggers with static control behave like asynchronous triggers when the clock input is active. This drawback is eliminated in triggers with dynamic and two-stage control. ***Triggers with dynamic control respond to a voltage transition*** from zero to one (active edge) or from one to zero (active edge of the control pulse). ***Triggers with edge control of the input signal*** (triggers with an internal delay) wide are applied on practice. Opportunity delays moment flip-flopping the trigger for a time equal to the duration of the clock pulse is effectively used in processing information, allowing produce By front clock impulses reading information , and according to the slice – a record.

Two-stage triggers contain two cells memory , recording information V which occur sequentially at different points in time. This structure of triggers is called a "master-slave" system or MS-structure (from the English master-slave). ***The first stage*** (master) ***serves for intermediate recording of input information ,*** and ***the second*** (slave) - ***for subsequent memorization and storage*** . Since this process is happening for two tact, That ***such triggers they call Also two-stroke*** . Control two-stage trigger Maybe Not only two, But And one clock with a pulse: recording information V leading step is happening With arrival clock pulse on the front, and rewriting to the slave – at the moment of its end (on the decline).

Note that ***triggers with dynamic and two-stage control are often called*** flip-flop, while those with static control are called latch. The trigger symbol on schemes serves letter T, A two-stage - TT, What reflects his internal device .

Let's consider most common types triggers.

JK trigger is a universal device ; its versatility lies in V volume, What They, Firstly, can be used V registers, counters, frequency dividers and other components, and secondly, by properly connecting their terminals, they can easily be converted into triggers of other types. This allows the industry to reduce the range of triggers without limiting the capabilities of hardware developers.

Scheme simplest JK flip-flop shown on rice. 1, V, A his analogues V EWB program – on rice. 1, G, Where indicated: J, TO - informational entrances; > - clock entrance; conclusion above – asynchronous presetting of the trigger to a single state (Q = 1) regardless of the state signals on entrances (functionally similar entrance S RS trigger); conclusion down -asynchronous preset V zero state (So called cleaning trigger, after which Q ' = 1); availability circles on images conclusions means, What active are low-level signals, and for the clock input, the trigger is switched not by the leading edge of the clock pulse, but by its edge (by the trailing edge of the pulse).

From the JK trigger circuit in Fig. 1, it follows that What its state depends not only on - signals on entrances J And TO, But And from logically related With them weekend signals, What allows you to exclude prohibited states. The functional feature of these triggers is that What at everyone combinations input signals, except TO = J = 1, They are in effect like RS trigger, and entrance J plays role S-input, A TO - role R-input; at TO = J = 1 V each At this point the trigger flips over and the output signals change their value.

D-triggers, unlike those considered, ***have one for setting to states 1 and 0 informational D-input*** (D - from English delay - tightening, delay). Functional The peculiarity of triggers of this type is that the signal at the output Q in clock cycle ***n*** +1 repeats the input signal ***Dn*** V previous tact ***n*** And saves (remembers) This state to next clock pulse. In other words, the D-trigger delays the information by one clock cycle, existing on D-input, those. law functioning D-trigger Very simple: $Q^{n+1} = D^{n}$. D-triggers store information using synchronization circuits, so all real D-triggers are clocked. Clock input control can be static, dynamic, or two-stage.

A D-trigger can be formed from any synchronous RS- or JK-trigger if mutually inverse signals D and D **' are simultaneously applied to their information inputs** (Fig. 1, e, d). Functional diagrams of D-triggers with and without presetting are shown in Fig. 1, g.

DV triggers represent by yourself modification D-triggers . Their logical functions are determined presence additional entrance V, playing role permitting By with respect to the input D (Fig. 1, 3). When V = 1, the trigger functions as a D-trigger, when V = 0 it passes V mode storage information regardless from shifts signals on at the entrance D. Information written into a conventional D-trigger cannot be stored for more than one clock cycle: with each clock pulse, the state of the trigger is updated. The presence of a V-input expands the functional possibilities D-trigger, allowing V necessary moments time save information at the outputs within the required number of cycles.

T And TV triggers (counting triggers) have one informational T-entrance (from English toggle - switch) And differ simplicity actions. Change states Here all sorts of things happen once, When input signal changes your own meaning V certain direction - from zero to one or from one to zero; this is the only type of trigger whose current state is determined Not information on entrances, A condition his V previous tact. By according to sobu input input information T-triggers can be asynchronous And synchronous. The methods for forming T-triggers based on JK- and D-triggers are shown in Fig. 1, and.

To study trigger circuits, it is advisable to use a word generator and LED indicators at the outputs, while for clocking the triggers it is necessary to use the output synchronization generator. ***Final task research is receiving tables transitions*** , being one from main characteristics trigger. It is advisable to ***obtain it in the following order*** :

– sequentially apply the corresponding active signals to the trigger preset inputs signals (0 or 1) And fix state exit triggers For this case; For to check the asynchronicity of these inputs, repeat the specified operations for different signal states at the clock and information inputs;

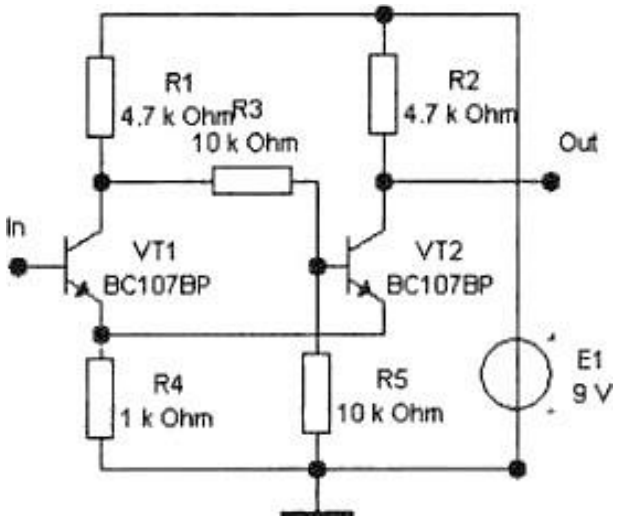
– apply signals 0 and 1 to the information inputs various combinations (at the inputs asynchronous presets at This should be corresponding inactive signals – 0 For inverse And 1 For straight) And fix For each combinations state trigger outputs ;

– on basis received results make up table transitions.

Schmitt triggers

IN thirties years XX centuries radio engineers, engaged in pulsed technology, related With development radar, And others applications electronics, tormented eternal problem discharge useful signal on background irregular interference. The one sought pulse goals

was literally fished out from a multitude of false impulses. The corresponding circuit was described V 1938 year ABOUT. G. Schmitt And received Name "Trigger Schmitt." IN those time The main - components of the devices were vacuum tubes (radio tubes). The Schmitt trigger was implemented on a double triode, as a two-stage amplifier, covered by internal positive feedback. The feedback was weak and its depth was selected so that to prevent stable self-generation. The result was a device that, when excess input voltage some threshold level (voltage response) jumped to another stable level (release voltage). The accepted Here terminology borrowed from relay techniques. Transfer characteristic TS by voltage has view loops hysteresis, similar magnetic hysteresis. Therefore, on the conventional graphic symbols of the TS, a characteristic generic mark in the form of a loop is placed hysteresis. So change component bases TS were completed on bipolar transistors , A then And By integral technologies, They entered V series TTL And CMOS microcircuits. Let's consider the operation of a classic Schmitt trigger circuit with two transistors (VT1 and VT2) with emitter connections (see Fig. 2). The input signal is fed to the *In input* (VT1 base), and the output signal is taken from the Out pin (VT2 collector).



Rice. 2 - Schematic diagram Schmitt trigger on transistors

Schmitt triggers, being asymmetrical devices, differ significantly from majority their own brothers: such common triggers, How RS, JK, D And T, which belong to the symmetrical group. The cascades in them are not identical in their parameters and connections. between them, But The main thing difference consists of V volume, What day off signal V The absence of an input is clearly defined. Therefore, such triggers lack memory and are used as triggering devices or for generating a sequence of rectangular pulses from arbitrary signals, such as sinusoids. In general, this type of trigger is closer to pulse rather than digital devices.

Content practical work, performed students during the lesson

1. Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

– operating system Microsoft Windows,
– text CPU Microsoft Office Word or OpenOffice.org Writer,
– program circuit design modeling Electronics Workbench EWB 5.12.

2. Plan execution practical works:

Tasks basic level:

1) To investigate the internal structure and operating logic of a simple RS flip-flop using a word generator.

2) To investigate the internal structure and operating logic of a synchronous single- stage RS trigger using a word generator.

3) Research logic functioning synchronous two-stage JK flip-flop with direct clock input and preset inputs using a word generator and logic analyzer.

4) To investigate the operating logic of a counting T-trigger using a word generator and a logic analyzer.

5) Research logic functioning two-stage D-trigger With help word generator and logical analyzer.

Tasks increased level:

6) Research logic functioning And methods applications Schmitt trigger .

7) Synthesize diagram given trigger V basis OR-NOT And conduct study of the logic of its functioning.

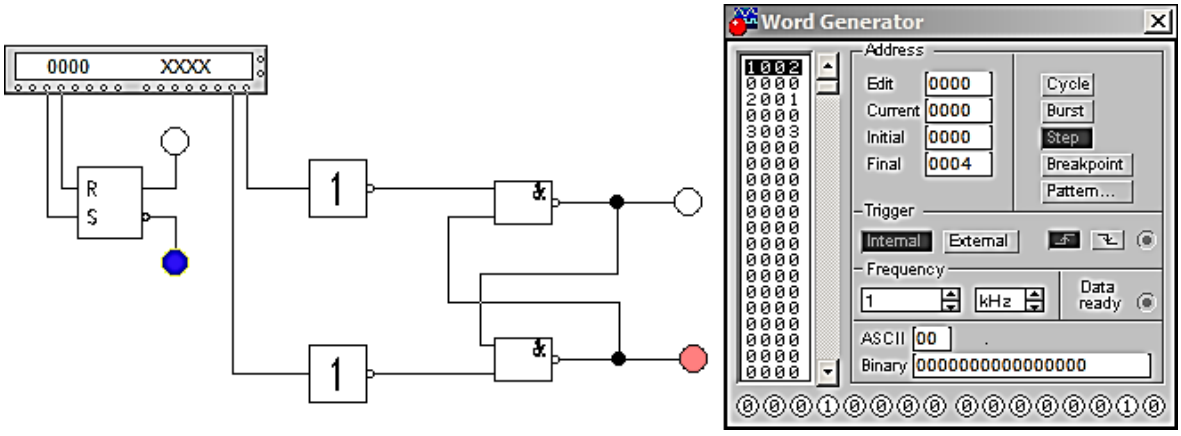
8) Conduct a study of the internal structure and operating logic of the triggers contained in a given logic microcircuit.

3. Order execution works:

1. Study triggers

Task 1. Explore the internal structure and functioning logic of the simplest RS trigger With help generator words . For this complete next actions :

1) Collect diagram research RS trigger, depicted on rice. 3, V which Two triggers are shown : on the left is a trigger from the EWB library, on the right is a trigger synthesized using logical elements.



Rice. 3 - Scheme research asynchronous RS trigger

2) IN cells generator words With 0000 By 0004 write down sequentially codes: 1001, 0000, 2001, 0000, 3003.

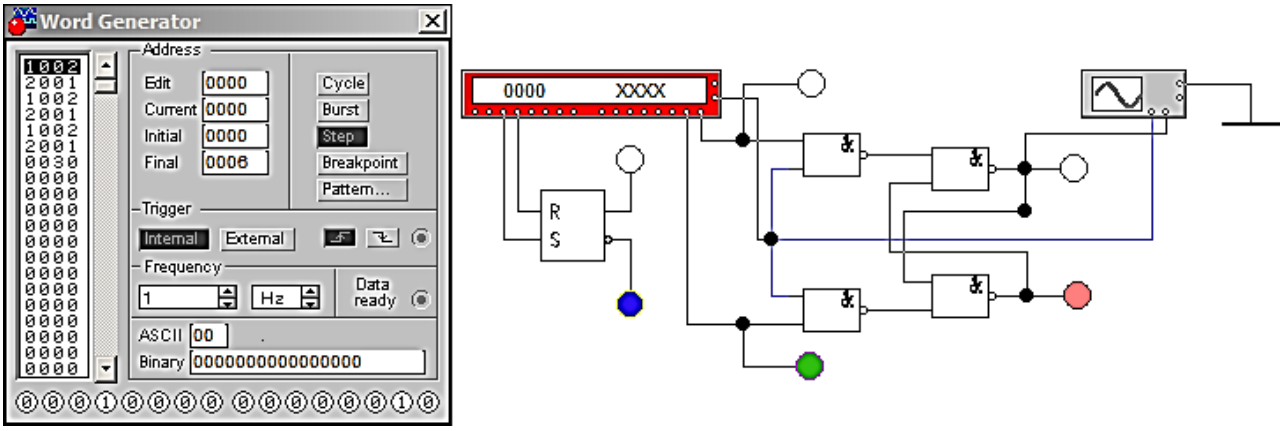
3) Launched generator words in step-by-step mode, set the transition table of the library RS trigger.

4) Determine where each input and output is on the synthesized trigger circuit, write down its transition table.

5) Do it conclusions By results work done .

Task 2. Investigate the internal structure and operating logic of a synchronous single-stage RS trigger using a word generator . To do this, perform the following steps:

1) Collect diagram research RS trigger, depicted on rice. 4, V which given two trigger: left asynchronous trigger from libraries EWB, on the right - synchronous single-stage trigger, synthesized on logical elements. Synchronization The trigger control inputs are controlled by the synchronization pulses of the word generator.



Rice. 4 - Scheme research synchronous single stage RS trigger

2) IN cells generator words With 0000 By 0006 write down sequentially codes: 1001, 2001, 1002, 2001, 1002, 2001, 3003.

3) Set the oscilloscope's time (horizontal) baseband (Time Base) to 0.5 s/div; vertical development By both of them channels install 5 In/del; vertical Channel A offset – +1.0; channel B vertical offset – -1.0.

4) After running the word generator in step mode, display the trigger's timing diagrams in the report. Determine which clock edge switches the trigger from one state to another.

5) Do it conclusions By results work done .

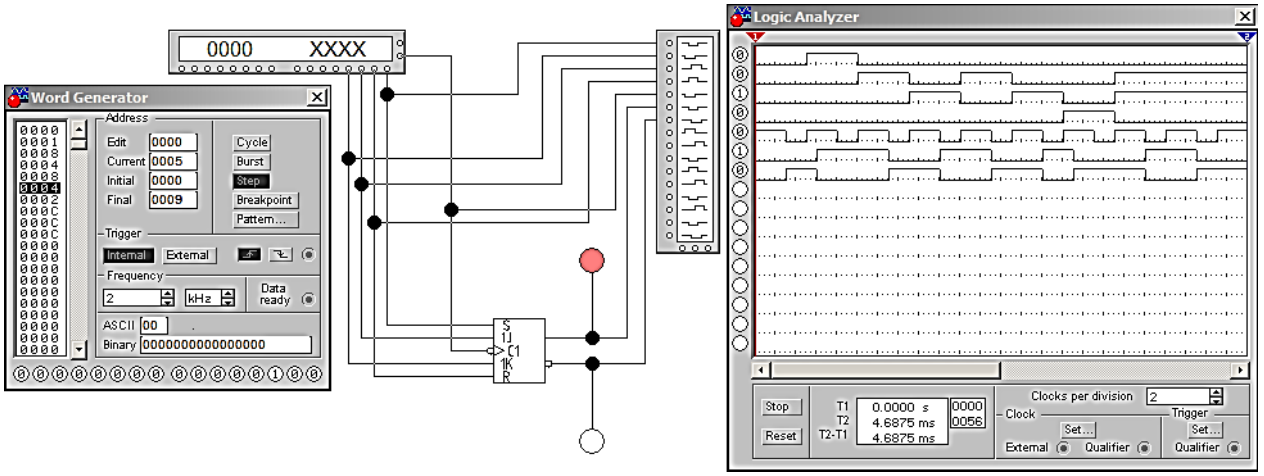
Task 3. Investigate the operating logic of a synchronous two-stage JK flip-flop with a direct clock input and preset inputs using a word generator and a logic analyzer . To do this, perform the following steps:

1) Assemble the JK flip-flop research circuit shown in Fig. 5, which shows JK flip-flop from libraries EWB, located V components Digital. This The trigger has preset inputs R and S with a high active level. Synchronization of the trigger control inputs is carried out by clock pulses of the word generator with a frequency of 2 kHz.

2) To supply control signals to the trigger inputs in the word generator cells from 0000 to 0009, write the following codes sequentially: 0000, 0001, 0008, 0004, 0008, 0004, 0002, 000C, 000C, 000C.

3) Install generator words V cyclical mode.

4) In the logic analyzer, set the frequency of the internal generator to 8 kHz. To do this, press the Set button, and after setting, press the Accept button.



Rice. 5 - Scheme research synchronous two-stage JK trigger

5) Install V window divider temporary intervals (Clocks per division) meaning 2.

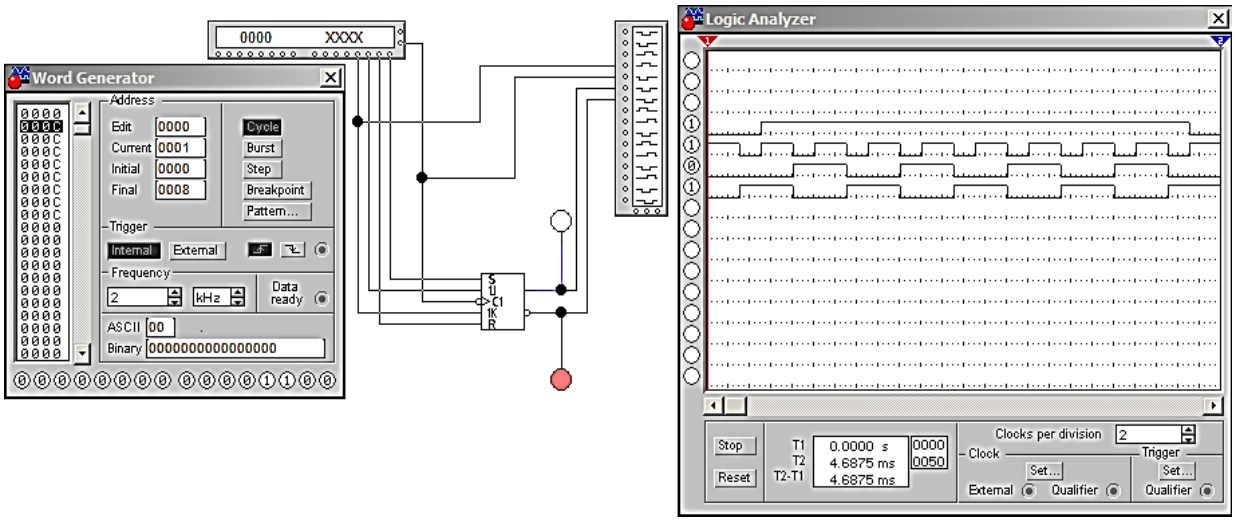
6) Start the circuit under study and, after the timing diagrams appear on the analyzer screen, stop the circuit or pause it.

7) Display the timing diagrams of the JK trigger operation in the report, analyze them, and establish a transition table (states) of this trigger.

8) Do it conclusions By results work done .

Exercise 4. Research logic functioning counting T-trigger With using a word generator and a logic analyzer . To do this, follow these steps:

1) Assemble the JK flip-flop research circuit shown in Fig. 6. The basis of the circuit is JK flip-flop from libraries EWB, located V components Digital. This The trigger has preset inputs R and S with a high active level. Synchronization of the trigger control inputs is carried out by clock pulses of the word generator with a frequency of 2 kHz.



Rice. 6 - Scheme research counting T- trigger

2) To convert a JK flip-flop into a counting T flip-flop, logical 1s must be supplied to the J and K inputs. To implement this, programmatically assign the code 000C to the word generator cells with addresses 0001–0008, and leave the code 0000 as zero.

3) Install generator words V cyclical mode.

4) In the logic analyzer, set the frequency of the internal generator to 8 kHz. To do this, press the Set button, and after setting, press the Accept button.

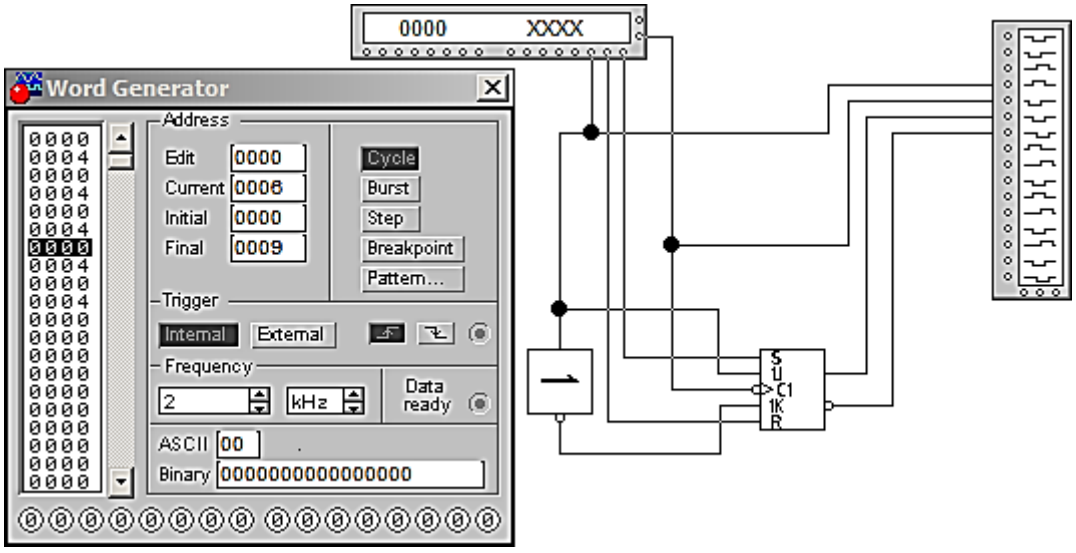
6) Start the circuit under study and, after the timing diagrams appear on the analyzer screen, stop the circuit or pause it.

7) Display the timing diagrams of the T-trigger operation in the report, analyze them, and establish a transition table (states) of this trigger.

8) Do it conclusions By results work done .

Exercise 5. Research logic functioning A two-stage D-type flip-flop using a word generator and a logic analyzer . To do this, follow these steps:

1) Assemble the D-trigger research circuit shown in Fig. 7. The basis of the circuit is JK flip-flop from libraries EWB, located V components Digital. This The trigger has preset inputs R and S with a high active level. Synchronization of the trigger control inputs is carried out by clock pulses of the word generator with a frequency of 2 kHz.



Rice. 7– Scheme research two-stage D - trigger

2) To convert a JK flip-flop into a D flip-flop, inverse signals must be applied to the J and K inputs. To implement this in software, word generator cells with addresses 0000, 0002, 0004, 0006, 0008 write down null code 0000, A V cell 0001, 0003, 0005, 0007 And
0009 write down code 0004.

3) Create a cycle in the word generator from cell 0000 to cell 0009, setting the word generator to cyclic mode.

4) IN logical analyzer install frequency internal generator, equal 8 kHz, to do this, press the Set button, and after setting, press the Accept button.

6) Start the circuit under study and, after the timing diagrams appear on the analyzer screen, stop the circuit or pause it.

7) Display the timing diagrams of the D-trigger operation in the report, analyze them, and establish a transition table (states) of this trigger.

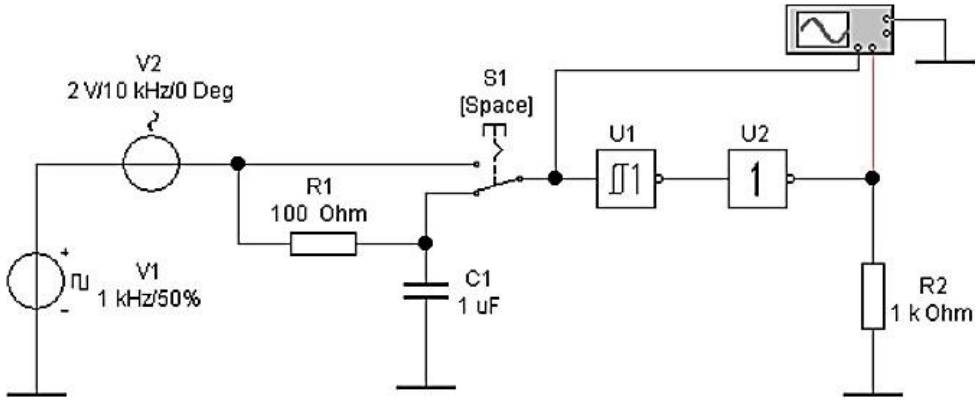
8) Do it conclusions By results work done .

Exercise 6. Research logic functioning and methods applications Schmitt trigger (high level) . To do this, follow these steps:

1) Assemble the non-inverting Schmitt trigger research circuit shown in Fig. 8. The basis of the circuit is the inverting Schmitt trigger U1 from the EWB library, located in the Logical Gates components.

Generator clock impulses (element V1) intended For formations sequences data. Generator harmonic signal (element V2) imitates induced in lines in-phase connections interference. Elements integrating chains R1 And C1 provide distortions pulsed sequences data, emerging for check influences physical

communication lines. Thus, the input of the inverting Schmitt trigger U1 receives either an additive mixture digital signal And in-phase analog interference (key S1 V top position), or a distorted and noisy signal (key S1 in the lower position).



Rice. 8– Scheme research non-inverting Schmitt trigger

To conduct research, connect the 1st channel of the oscilloscope (channel A) to the input of the inverting Schmitt trigger, and the 2nd channel (channel B) to the output of the inverter U2.

2) Obtain the transfer characteristic of a non-inverting Schmitt trigger, i.e. the dependence weekend voltage from input. For this execute next operations:

— Set the initial data in the circuit: in the clock pulse generator V1 – amplitude 5 V, frequency 1 Hz, duty cycle – 2 (50%). In the generator V2, initially set the common-mode interference amplitude equal to 0. Switch S1 is closed in the upper position;

— open oscilloscope, install V him development B/A;

— launch simulator EWB And visually observe, How By measure growth the entire curve is plotted ;

— define V what direction is being drawn figure hysteresis relative to the movement of the clockwise hand;

— bring in received transmission characteristics V report By laboratory ra-
bot.

3) Get transmission characteristics inverting trigger Schmitt. For
To do this, perform all the operations of the previous point, but first switch the 2nd channel (channel B) of the oscilloscope to the output of the Schmitt trigger U1. Compare the obtained transfer characteristics.

4) To conduct research into the operating logic of a non-inverting Schmitt trigger, do the following:

— Set the initial data in the circuit: in the clock pulse generator V1 – amplitude 0.1 V, frequency 1 Hz, duty cycle – 2 (50%). In the generator V2, set the common-mode amplitude interference equal to 5 V, frequency – 10 kHz. Switch S1 is closed V upper position; connect the 2nd channel (channel B) of the oscilloscope back to the output of the inverter U2;

— open oscilloscope, install V him temporary development Y/T;

— run the EWB simulator, obtain an oscillogram of the harmonic signal at the trigger input and the pulse signal at its output;

— bring in received oscillograms V report By laboratory work;

— define which threshold meaning triggering trigger more: at when switching from low voltage to high voltage or when switching from high to low voltage.

5) Conduct a study on the feasibility of using a non-inverting Schmitt trigger to protect against high-frequency interference in a communication line without distortion. To do this, perform the following operations:

— set the initial data in the circuit: in the clock pulse generator V1 – amplitude 5 IN, frequency 1 kHz, porosity - 2 (50%). IN generator V2 install amplitude

in-phase high-frequency interference equal 1 IN, frequency - 10 kHz. Key S1 closed V upper position; connect the 2nd channel (channel B) of the oscilloscope back to the output of the inverter U2;

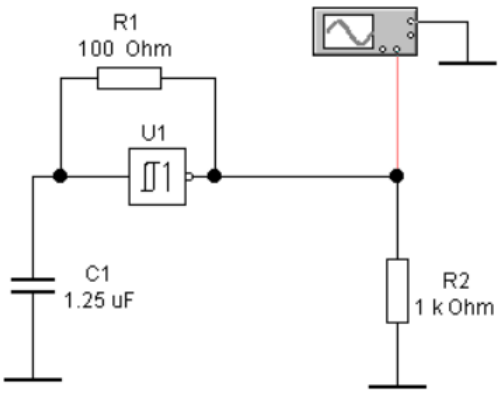
— open oscilloscope, install V him temporary development Y/T;
— run the EWB simulator, obtain oscillograms of the input signal and output signal;
— bring in received oscillograms V report By laboratory work;
— define, What happened With hindrance And on How many exactly restored primary signal;
— increase amplitude in-phase HF interference to 1.5 IN, A then to 3 IN, repeating research operations to determine what happened to the output signal ;
— do conclusion O potential possibilities trigger Schmitt By cutoff HF By-fur.

6) Conduct study possibilities applications non-inverting trigger Schmitt to protect against high-frequency interference in a communication line with distortions. To do this, perform the following operations:

— Set the initial data in the circuit: in the clock pulse generator V1 – amplitude 5 V, frequency 1 kHz, duty cycle – 2 (50%). In the generator V2, set the common-mode amplitude high-frequency interference equal 3 IN, frequency - 10 kHz. Key S1 closed V lower position;
— open oscilloscope, install V him temporary development Y/T;
— run the EWB simulator, obtain oscillograms of the input signal and output signal;
— bring in received oscillograms V report By laboratory work;
— define, What happened With hindrance And on How many exactly restored primary signal;
— increase the amplitude of the common-mode RF interference to 5 V, repeat the research operations , and determine what happened to the output signal;
— do conclusion O potential possibilities trigger Schmitt By cutoff HF By-fur.

7) Conduct research possibilities applications non-inverting trigger Schmitt For generation impulses. For this execute next operations:

— collect generator circuit impulses on the inverting trigger Schmitt, shown in Fig. 9;



Rice. 9 - Scheme generator impulses on trigger Schmitt

— install V scheme element values: C1 = 1.25 μF, R1 = 100 Ohm, R2 = 1 kOhm;
— launch simulator EWB, get oscillogram pulse signal;
— bring in received oscillogram in report By laboratory work;
— measure the pulse repetition period T and duration using the oscilloscope cursors positive impulse τ , received results bring in V report By laboratory work;

— calculate the pulse repetition frequency and their duty cycle, and record the obtained results in the laboratory report;

— increase initial capacity capacitor C1 V 10 times, get an oscillogram of pulses, measure the period of their duration and period, calculate the frequency and duty cycle, for V report By laboratory work oscillogram impulses, measured And calculated parameters;

— decrease initial capacity capacitor C1 V 10 once, get oscillogram of pulses, measure the period of their duration and period, calculate the frequency and duty cycle, for V report By laboratory work oscillogram impulses, measured And calculated parameters;

— draw a conclusion about how the value of the capacitance affects the parameters of the generated pulse signal.

8) Do conclusions By results research logic functioning And ways to use the Schmitt trigger.

Task 7. Synthesize a circuit of a given trigger in the OR-NOT basis and conduct a study of the logic of its operation (advanced level).

Task 7 increased level is being carried out students on one's own By given options, given in Table 1.

The task is completed and presented in the laboratory report in the same way as tasks 1–5.

Table 1 - Table options For tasks 7

No. vari anta	**Synthesized trigger**	**No. vari anta**	**Synthesized trigger**
1.	Asynchronous RS trigger	2.	Asynchronous RS trigger
3.	Synchronous single-stage RS trigger	4.	Synchronous single-stage RS trigger
5.	Two-stage JK trigger	6.	Two-stage JK trigger
7.	Counting T- trigger	8.	Counting T- trigger
9.	Two-stage D- trigger	10.	Two-stage D- trigger
11.	Asynchronous RS trigger	12.	Asynchronous RS trigger
13.	Synchronous single-stage RS trigger	14.	Synchronous single-stage RS trigger
15.	Two-stage JK trigger	16.	Two-stage JK trigger
17.	Counting T- trigger	18.	Counting T- trigger
19.	Two-stage D- trigger	20.	Two-stage D- trigger

Task 8. Conduct a study of the internal structure and operating logic of the triggers contained in a given logic microcircuit (high level).

Task 8 increased level is being carried out students on one's own By given options, given in Table 2.

Table 2 - Table options For tasks 8

No. vari anta	**IMS**	**Varian t No.**	**IMS**
1.	7472 (K155TV1)	2.	7474 (K155TM2)
3.	74113 (K155TV10)	4.	7477 (K155TM5)
5.	74114 (K155TV11)	6.	7475 (K155TM7)
7.	74109 (K155TV15)	8.	74175 (K155TM8)
9.	74107 (K155TV6)	10.	74174 (K155TM9)
11.	74112 (K155TV9)	12.	74173
13.	7473	14.	74279 (K155TR2)
15.	7478	16.	7414 (K155TL2)
17.	7476	18.	74132 (K155TL3)
19.	74373 (K155IR22)	20.	74377 (K155IR27)

IN this task must be completed next actions:

1) IN networks Internet find passport data given microcircuits. For this You can use the website of Microchips... – URL: https://www.microshemca.ru

2) Using the chip's datasheet, you can understand its purpose and operating principle. work And typical application, at this bring in V report By laboratory work description and internal structure of the microcircuit, the table of its states.

3) To develop a methodology for studying the microcircuit in such a way as to check its internal structure And logic functioning, specified V passport data, A Also check all the given options for using the microcircuit.

4) Assemble a circuit for studying a given logic chip by finding it in the EWB library located in the Logical Gates components, using all the signal sources and measuring devices necessary for the study .

5) Conduct a study of the internal structure and operating logic of a given logic microcircuit using the developed methodology.

6) Do conclusions By results research.

4. Content report about work

IN In the report, please provide:

– topic And target work work ,

– plan work (performed tasks);

– designs ;

– results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, oscillograms, etc.;

– conclusions O done work.

5. Control questions For preparation To report protection :

1) Scroll And characteristic subsequence (accumulating) digital devices.

2) Purpose, types and characteristics of principles constructions and work triggers.

3) Purpose, types And characteristic principles constructions And work counters-
kov.

4) Purpose, types And characteristic principles construction and work of registers.

5) Order research internal structures And logic functioning simpler-
neck RS trigger With help generator words.

6) The order of studying the internal structure and logic of the functioning of the - synchronous single-stage RS trigger by using generator words.

7) Order research logic functioning synchronous two-stage JK trigger With straight clock entrance And entrances presets With help generator words and logical analyzer.

8) Order research logic functioning counting T-trigger With using a word generator and a logical analyzer.

9) Order research logic functioning two-stage D-trigger using a word generator and a logic analyzer.

10) Order research logic functioning And methods applications trigger

Schmitt.

11) Order synthesis schemes given trigger V basis OR-NOT And research the logic of its functioning.

12) Analysis internal structures And logic functioning triggers, contained in a given logic chip.

The practical work was developed by an
associate professor of the Department of
Digital Robotic Systems and Electronics of
the Institute of Advanced Engineering,
Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 16

Subject: **STUDY REGISTERS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of sequential digital devices using universal packages of applied computer programs;

– conduct study sequential digital devices on basis their circuit models,

– synthesis of sequential digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

TRAINING AND MATERIAL SUPPORT:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study registers.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study registers.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENT LABORATORY CLASSES

Brief theoretical or reference and information materials

Sequential or accumulating nodes of digital devices are nodes that contain memory elements, specifically triggers. Two types of accumulating nodes can be distinguished: registers and counters.

Register - accumulating knot, designed For reception, storage, transformations And issuance binary information. ***Counter*** - accumulating knot, designed for counting events, counting pulses arriving at the counting input.

Among sets input signals accumulating node Can highlight information , control, synchronization . Under the influence of input signals, the node is capable fulfill that microsurgery, on which He configured preliminary filing a certain combination of control signals.

Actually ***microsurgery is ending change states node*** synchronously under the action of a synchronization signal or asynchronously when a signal is applied to the asynchronous input of the preliminary installations node V certain state. Executed knot microoperations can be any, which required For execution given algorithm. That's why often a counter, For example, simultaneously Maybe accept parallel information in All bits, that is, to perform a micro-operation characteristic of the register, and vice versa, the register is designed in such a way that it can also perform the function of counting the number of pulses. That is, both the functions of a register and a counter can be implemented in a single unit. Complex micro-operations can demand attracting additional combinational nodes for implementation microoperations, on which Not calculated used chip register or counter.

Managers signals allow choose mode work node , That There is ask the required micro-operation. The micro-operation itself is completed at the moment the clock signal is triggered. or V moment parish signal on asynchronous entrance node. If knot contains information inputs for parallel reception of information, then they can be numbered in order or With taking into account their weight. Weekend chains node can be organized By scheme With three states, which will require an additional input to control the output amplifiers.

Registers

The main thing appointment registers - storage And transformation multi-bit binary numbers. Registers along with counters And memorable devices are the most common devices in digital technology. Despite their relative simplicity, registers have great functionality ***. They are used*** as control And memorizing devices, generators And converters codes, counters, dividers frequencies, nodes temporal delays. ***Registers are being carried out*** on synchronous trig gerah D- or JK-type With dynamic or static management. ***Single trigger Maybe remember (register) one discharge (bit) binary information*** . Such The trigger can be considered a single-bit register. ***Writing information to the register is called an operation.*** **input** ***or*** **records.** ***Issuance information external devices characterizes the operation*** **of output** ***or*** **reading** . Writing information to a register does not require its preliminary zeroing.

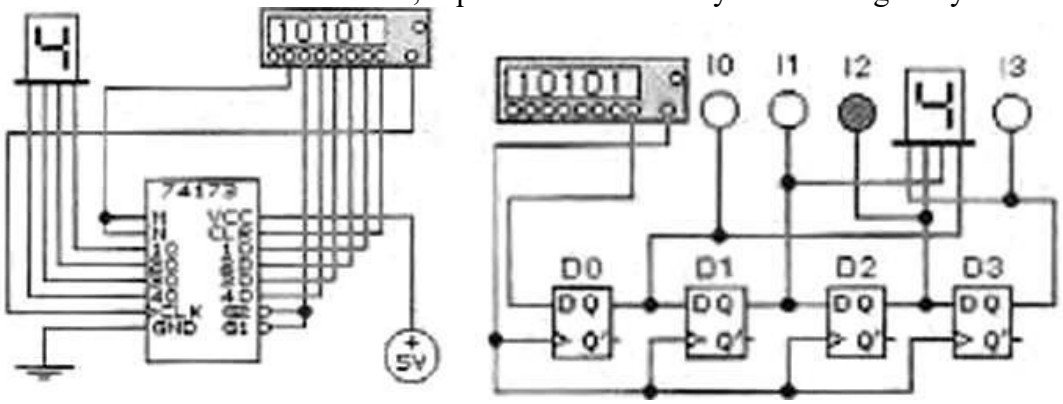
The concept of “weighting coefficient” is not applicable to register bits, unlike the counter, because weight addiction between separate discharges entirely is determined for writing V register information. By this reason on conditional images registers The numbering of information inputs and outputs is applied sequentially.

All registers are divided into two categories based on their functional properties : accumulative (memory, storage) and shift registers. Shift registers, in ***turn, are divided by their input and output method*** into parallel, serial, and combined (parallel-serial and serial-parallel). ***By direction transmissions (shift) information*** - on unidirectional And reversible .

Most simple registers are registers memory . Their appointment - storing small amounts of binary information for a short period of time. These registers are a set of synchronous triggers, each of which stores one digit of a binary number. ***Input (writing) and output (reading) of information is performed parallel code*** . Input provided clock impulse, With arrival another one clock impulse recorded information is being updated. ***Reading is produced in direct or reverse code*** (in the latter case – from inverted outputs).

Storage registers are sets of flip-flops with independent information entrances And usually common clock entrance. IN such quality are used synchronous triggers, composed of microcircuits containing several independent triggers in one housing, for example K155TM8 (74175), K155TM9 (74179) and others, which can be consider How 4 ... 6-bit registers memory. Extension bit depth The number of memory registers is achieved by adding the required number of triggers, the clock inputs of which are connected to the synchronization bus.

Register K155IR15 (74173) is a library component of EWB and can serve example devices storage With three weekends states (scheme inclusions - in Fig. 1, a). Note again extremely unsuccessful location conclusions register 74173 And their discrepancy with the original. As can be seen from Fig. 1, b, K155IR15 is a four-digit register. It has exits 1Q...4Q With third Z-state (at signal 1 on conclusions G2, G1), A his inputs 1D...1D are equipped with logical elements for recording enable by applying a logical 0 to entrances M, N (V EWB wrongly shown straight). It is used register How four- row source code, capable service directly tire data digital systems .



Rice. 1 - Scheme inclusions register 74173 (A) With installations generator words (V) and the simplest scheme shift register on D-triggers (b) With installations generator words (G) to test it

Loading of information into the register is performed synchronously with the positive - difference clock impulse, If on entrances M, N are present voltage low level. If on one from these entrances voltage high level, after parish positive tactful difference V register should stay previous data. Entrance reset CLR has high active level. If on G2 inputs, G1 filed voltage active low level, data , contained V register, are displayed on exits 1Q...4Q, presence Although would one voltage high level on entrances permissions G2 And G1 causes Z-state (disconnection) For weekend lines. At this data from register V tire data systems Not pass,

The register outputs do not affect the operation of other similar outputs connected to the conductors tires. On work of inputs CLR reset and clock WITH change levels on entrances resolution has no effect.

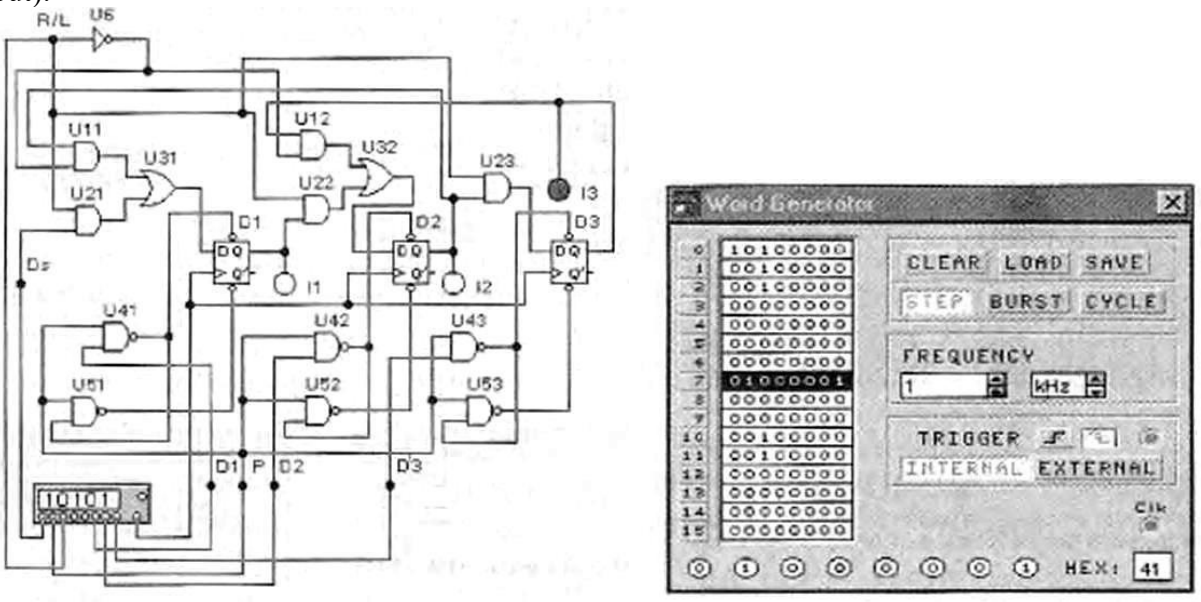
Register K155IR15 consumes current 72 mA And has clock frequency to 25 MHz; The 74LS173 variant consumes 30 mA at a clock frequency of 30 MHz. The generator's operating modes in the register circuit and some of its code combinations are shown in Fig. 1, c.

The second common class of registers are shift registers , which are distinguished by a great diversity both in terms of functionality and in terms of circuit solutions and characteristics. ***Shift registers*** , in addition to the storage operation, ***perform the conversion*** of serial binary code into parallel, and parallel into serial; they ***perform*** arithmetic and logical operations ***serve*** as time delay elements **.**

To my own name They obliged characteristic For these devices operations shift. ***WITH with - each clock pulse, the trigger contents are rewritten (shifted) each discharge V neighboring discharge without changes order following units And zeros*** . When shift information to the right after each clock impulse bit from more senior times a row shifts V younger, A at shift to the left - vice versa. This process illustrated about the simplest shift register in Fig. 1, b, d.

In domestic circuits, the register symbol is the letters RG. For shift registers, the shift direction is also indicated: > - to the right; < - to the left; <-> - reversible (bidirectional).

Fig. 2, a shows ***the diagram of a universal register*** , which can perform the following functions: consistent reception information (entrance Ds, on tire management signal P = 0); parallel loading (inputs D1 ... D3, R = 1); shift to the right And to the left (on at the entrance control R/L signal 1 and 0, respectively). The register is implemented on D-triggers with presetting by low-level signals at the R-inputs (lower output) to the zero state and to the one state at the S-input (upper output).



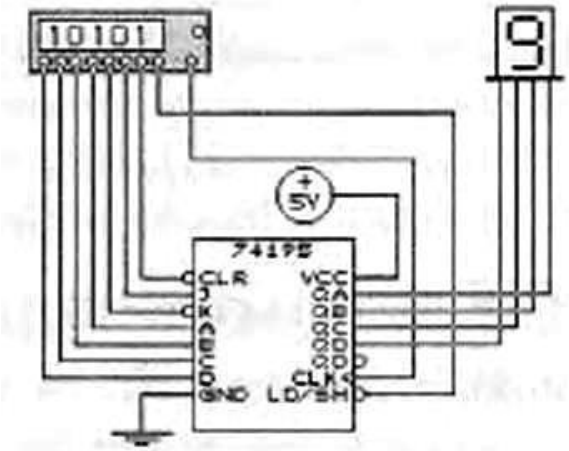
a) b)

Rice. 2 - Scheme universal register (a)
And installations word generator (b) to test it

At null binary combinations (cm. rice. 2, b) signals Ds = 1 And R/L = 1. That's why at the output of U21, a signal 1 is generated, which is transmitted through U31 to the D-input of trigger D1 and under action clock signal translates his V single state. IN subsequent two combinations signal R/L = 1, That's why signal 1 With first trigger is being rewritten in second (through U22, U32), A then through U23 - V third (shift to the right). At combinations 3 - 4 signal

R/L = 0, at this elements U21, U22 are blocked, And on exit U6 is being formed signal 1, under the influence of which signal 1 from the output of trigger D3 through U12, U32 is rewritten into D2, and then through U11, U31 - V D1 (shift to the left). At combinations 7 signal permissions parallel loading R = 1, while at the inputs D1 ... D3 receives code 001, in as a result of which the triggers D1 (via U41, U51) and D2 (via U42, U52) are set to the zero state via the R-inputs, and the trigger D3 through U43, U53 is being translated By S-entrance single state. At In combinations 8, 9 (R/L = 0) a shift is made to the left, and in combinations 10, 11 (R/L = 1) a shift is made to the right.

We will consider the operation of another shift register using the example of the library register 74195 (K155IR12), the circuit diagram of which is shown in Fig. 3. The IMS 74195 is a high-speed register for performing shift, count, accumulation and mutual parallel-serial operations. transformations digital words. WITH help entrance LD/SH are loading parallel data, And is produced their shift to the right. If on this at the entrance there is tension high level, through entrances first trigger J And TO V register are introduced sequential data. Entrance J has high active level, entrance TO - short; If these Connect the inputs to create a simple D-input. Data is shifted from QA to QB, QC, and then to QD after each positive transition on the CLK clock input.

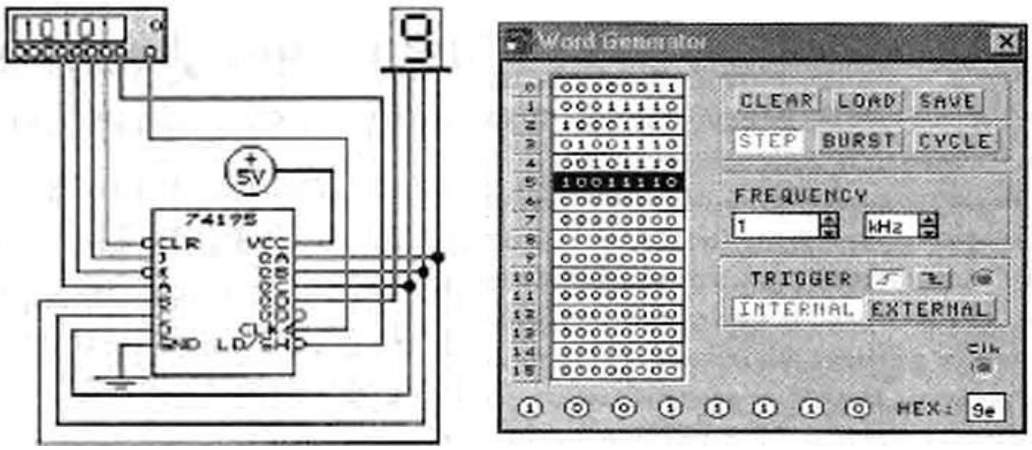


Rice. 3 – Connection diagram of register 74195

If on at the entrance LD/SH present voltage low (active) level, All The four register flip-flops are triggered by a single clock transition (from low to high). Then the data from parallel entrances A ... D are transmitted to the appropriate outputs QA ... QD. Data shift to the left is provided in the circuit where each output Qn is connected by an external jumper with entrance Days, those. scheme inclusions on rice. 43 corresponds only regime receiving and storing data.

Scheme inclusions IMS V mode shift proven on rice. 4, A), modes work torus generator words - on rice. 4, b). For regime shift voltage on at the entrance LD/SH necessary fix on high level. Because of Togo, What All operations V register IR12 strictly synchronous And are performed on pulse edges, the logical levels at the inputs J, K, Dn, LD/SH can be arbitrarily changed before the clock signal arrives.

Voltage low level on at the entrance CLR, except operations zeroing, means also a ban on action clock impulse CLK; For correct reset data is selected the moment when a low-level voltage is present at the CLK input.



Rice. 4 - Scheme inclusions register 74195 V mode shift (A) And facial panel word generator with operating modes in the circuit (b)

Content practical work, performed students during the lesson

Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

– operating system Microsoft Windows,
– text CPU Microsoft Office Word or OpenOffice.org Writer,
– program circuit design modeling Electronics Workbench EWB 5.12.

Plan execution practical works:

Tasks basic level:

1) Research internal structure And logic functioning sequential four-bit shift register using a word generator and a logic analyzer.

2) Research internal structure And logic functioning parallel four -bit register using a word generator and a logic analyzer.

3) Research logic functioning universal register on IMS 74195 (K155IR12) using a word generator.

Tasks increased level:

4) Conduct study internal structures and logic functioning register contained in a given logic chip.

5) Synthesize diagram given register And conduct study logic his functioning .

Order execution works:

Exercise 1. Research internal structure And logic functioning A serial four-bit shift register using a word generator and a logic analyzer . To do this, follow these steps:

1) Assemble the register analysis circuit shown in Figure 5. The circuit is based on a D-trigger, implemented using a JK-trigger from the EWB library, found in Digital components. The register operates in such a way that data is written sequentially by shifting from the least significant bits to the most significant bits, and is read in parallel.

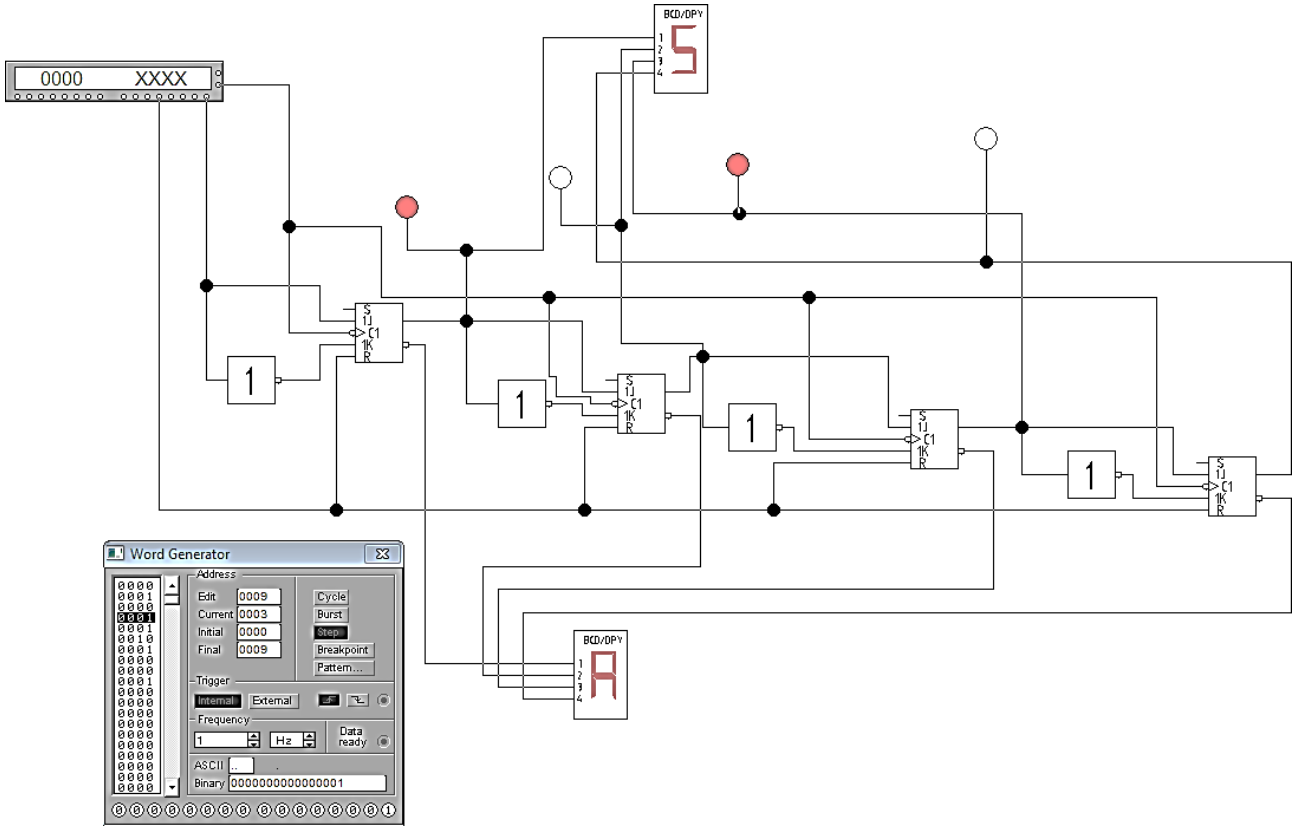
2) Analyze internal structure register And define quantity his information and control inputs.

3) To check the logic of the register operation, program the generator cells words So, to from their younger discharge sequentially was read code numbers, determined by the formula:

$$TO = \mathbf{mod}(N_{list}\ 10) + 1\ ,$$

;

where $N_{is\ spis}$ – student number on the list in the journal, ***mod*** – a function that calculates the remainder of a number to the base 10.



Rice. 5 - Scheme research sequential four-digit register

4) Organize V generator words cycle, providing consistent recording to the register code given numbers With subsequent his full zeroing. Install Word generator in step-by-step mode.

5) Launch being researched diagram V work V step by step mode, sequentially Press the Step button.

6) Analyze state triggers register on each tact, having written down stored numbers in direct and reverse codes in the report.

7) Define V what side to happen shift stored numbers And volume stored information.

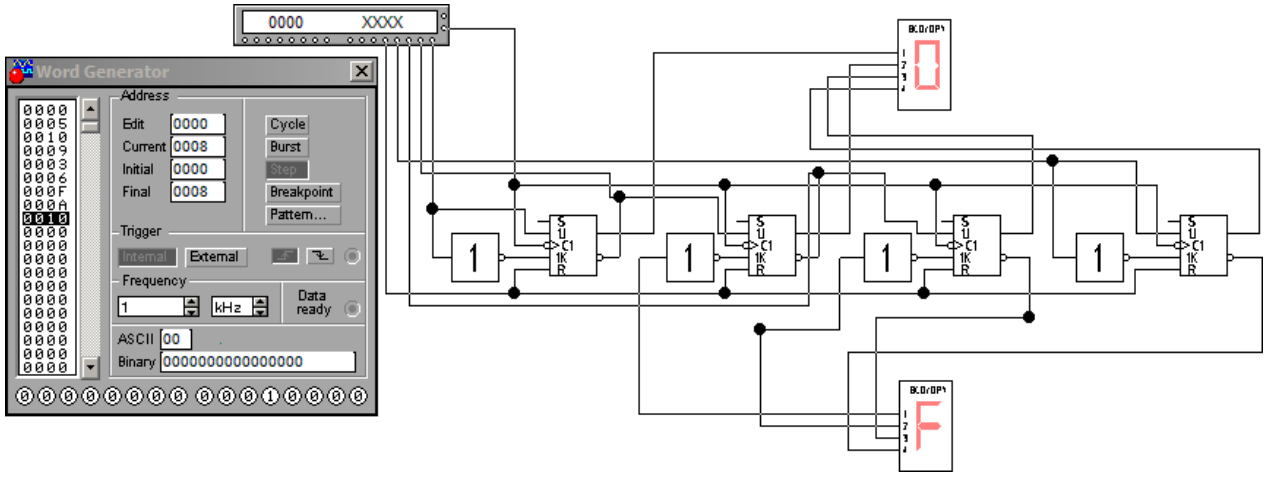
8) Do it conclusions By results work done .

Exercise 2. Research internal structure And logic functioning parallel four-bit register using a word generator and a logic analyzer . To do this, follow these steps:

1) Assemble the register research circuit shown in Figure 6. The circuit is based on a D-trigger, implemented using a JK-trigger from the EWB library, found in Digital components. The register's operating principle is that data is written to it in parallel.

2) Analyze internal structure register And define quantity his information and control inputs.

3) To check the logic of the register operation, program the cells of the word generator in such a way as to first reset the register, then sequentially write the codes of the 4 numbers indicated in Table 3, and finally reset the register to the zero state.



Rice. 6 - Scheme research parallel four-digit register Table 3 – Initial data for tasks 2 and 3.

Номер варианта	Шестнадцатеричный код чисел	Номер варианта	Шестнадцатеричный код чисел
1.	A, 7, 3, 9	2.	D, 3, 5, 9
3.	1, B, 8, F	4.	B, 7, F, 3
5.	3, 7, C, 4	6.	7, C, 5, 8
7.	5, 2, E, 6	8.	2, E, 6. F
9.	4, D, 9, F	10.	4, D, 9, F
11.	E, A, 8, 3	12.	A, 8, 3, 4
13.	8, C, 6, 7	14.	C, 7, A, 6
15.	7, 9, F, B	16.	9, F, B, 1
17.	2, 6, A, E	18.	6, A, E, 5
19.	3, 9, D, 8	20.	9, D, 8, 3

4) Organize V generator words cycle, providing consistent recording into the register of codes for the given numbers. Set the word generator to step-by-step mode.

5) Launch being researched diagram V work V step by step mode, sequentially Press the Step button.

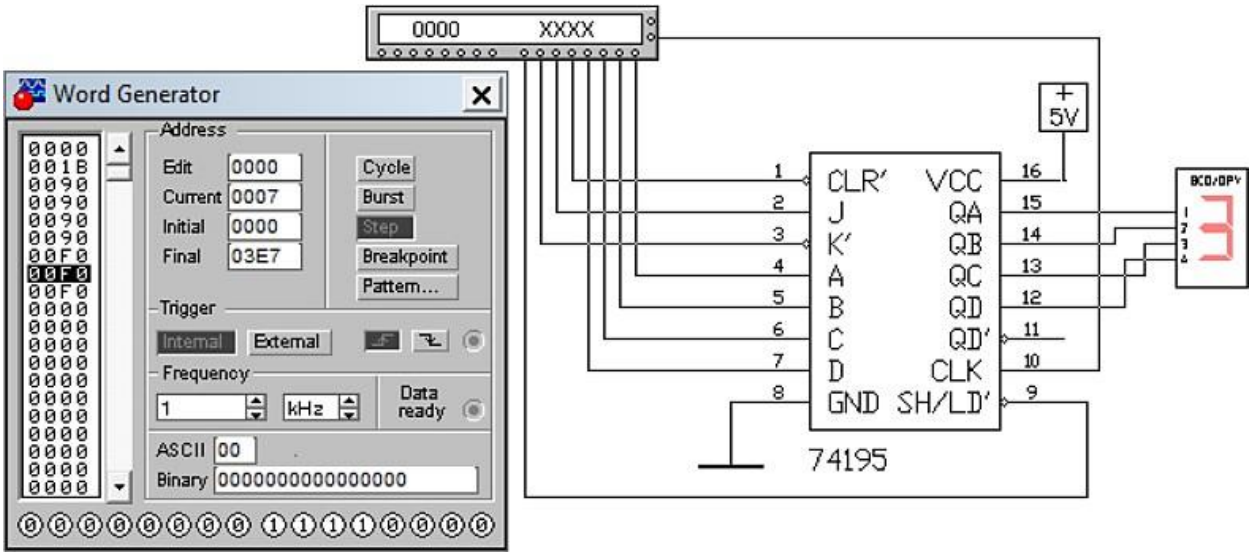
6) Analyze state triggers register on each tact, having written down stored numbers in direct and reverse codes in the report.

7) Define volume stored information V register.

8) Do it conclusions By results work done .

Task 3. Research the operating logic of a universal register on an integrated circuit 74195 (K155IR12) With help generator words . For this complete next actions :

1) Collect diagram research universal register, depicted on rice 7.



Rice. 7 – IMS connection diagram 74195 (K155IR12)

2) Analyze logic functioning IMS With taking into account given information . IMS 74195 is a high-speed register for performing shift, count, accumulation and mutual parallel-serial conversion of digital words.

Peculiarities management IMS 74195 (K155IR12), located V components Digital in the additional panel " → " (Shift Registers), are as follows:

– reset register V zero state is produced at availability voltage low level (logical zero) at the CLR' input, to perform all other operations, a logical one must be present at this input;

– zero level at the LD/SH input ;

– consistent recording with shift data to the right is produced through entrances the first - trigger J and K' in the case when a high- level voltage is present at the input LD/SH';

– writing data into the register, i.e. their transfer from parallel inputs A ... D are transmitted on corresponding exits QA...QD, A Also shift data V direction from QA To QB, QC, A then To QD is being carried out after each positive difference on clock CLK input .

3) To check the logic of the universal register, program cells generator words like this in this way, to at the beginning reset (reset) register, after which download parallel code maximum numbers from tables 3 By specified option, and then write the minimum number from table 3 sequentially into the register.

4) Organize a loop in the word generator that ensures the execution of this task . Set the word generator to step-by-step mode.

5) Launch being researched diagram V work V step by step mode, sequentially Press the Step button.

6) Analyze state triggers register on each tact, having written down stored numbers in direct and reverse codes in the report.

7) Do it conclusions By results work done .

Task 4. Conduct a study of the internal structure and logic of functioning register, contained V given logical microcircuit (increased level). This advanced level task is completed by students independently according to the instructions to the options given in Table 4.

Table 4 - Table options For tasks 4.

No. variant	IMS	Option number	IMS
1.	7491	2.	74373 (K55IR22)
3.	74164 (K155IR8)	4.	74374 (K55IR23)
5.	74165 (K155IR9)	6.	74375
7.	74166	8.	74377 (K55IR27)
9.	74194(K155IR11)	10.	74378
11.	74195(K155IR12)	12.	74379
13.	74198(K155IR13)	14.	74174 (K155TM9)
15.	74199	16.	74175 (K155TM8)
17.	74173 (K155IR15)	18.	7475 (K155TM7)
19.	74273	20.	7477 (K155TM5)

IN this task necessary execute next actions:

1) IN networks Internet find passport data given microcircuits. For this You can use the website of Microchips... – URL: https://www.microshemca.ru

2) Using the chip's datasheet, you can understand its purpose and operating principle. work And typical application, at this bring in V report By laboratory work description and internal structure of the microcircuit, the table of its states.

3) Compose methodology research microcircuits like this in this way, to was opportunity check her internal structure And logic functioning, specified V passport data, A Also check All given options applications given microcircuits.

4) Assemble a circuit for studying a given logic chip by finding it in the library EWB. Connect To microcircuit All necessary For research sources signals and measuring devices.

5) Conduct a study of the internal structure and operating logic of a given logic microcircuit using the developed methodology.

6) Do conclusions based on the results research.

Task 5. Synthesize a circuit for a given shift register and conduct a study of the logic of its operation (advanced level).

This advanced level task is completed by students independently using the given options given in Table 5.

Table 5 - Table options For tasks 5.

No. variant	Exercise	No. variant	Exercise
1.	5-bit shift register to the left on 2 discharge on JK triggers	2.	6-bit shift register to the left on 3 discharge on JK triggers
3.	5th discharge register with shift to the right on 2 discharge on JK triggers	4.	6th discharge register with shift to the right on 3 discharge on JK triggers
5.	5th discharge reversible register with a shift of 2 times- row on JK triggers	6.	6th discharge reversible register with a shift of 3 times- row on JK triggers
7.	5-bit shift register to the left on 2 discharge on D triggers	8.	6-bit shift register to the left on 3 discharge on D triggers

9.	5-bit shift register to the right on 2 discharge on D triggers	10.	6-bit shift register to the right on 3 discharge on D triggers
11.	5th discharge reversible register with a shift of 2 times- row on D triggers	12.	6th discharge reversible register with a shift of 3 times- row on D triggers
13.	8-bit shift register to the right on 1 discharge on microcircuit 74373(K155IR22)	14.	8-bit shift register to the left on 1 discharge on microcircuit 74373 (K155IR22)
15.	8-bit shift register to the right on 2 discharge on the 74373 microcircuit (K155IR22)	16.	8-bit shift register to the left on 2 discharge on a microcircuit 74373 (K155IR22)
17.	8-bit shift register to the right on 3 discharge on the 74373 microcircuit (K155IR22)	18.	8-bit shift register to the left on 3 discharge on a microcircuit 74373 (K155IR22)
19.	8-bit shift register to the right on 4 discharge on the 74373 microcircuit (K155IR22)	20.	8-bit shift register to the left on 4 discharge on a microcircuit 74373 (K155IR22)

Methodology execution tasks similar task 1.

By results research do conclusions By structure synthesized shift register and the logic of its operation.

Content report about work

IN In the report, please provide:

– topic And target work work ,

– plan work;

– brief abstract theoretical material;

– designs ;

– results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, voltage diagrams, etc.;

– conclusions O done work.

Control questions For preparation To report protection :

1) List and characteristics of sequence (accumulative) digital devices.

2) Order research internal structures And logic functioning sequential four-digit register shift With help generator words And logic analyzer.

3) Order research internal structures And logic functioning parallel four-digit register With help generator words And logical analyzer.

4) The procedure for studying the logic of operation of the universal register on the 74195 IC (K155IR12) using a word generator.

5) Order synthesis schemes given register shift And research logic his functioning .

6) Analysis results research internal structures And logic functioning of the register contained in a given logic chip.

Laboratory Job developed
Associate Professor of the Department of Digital Robotic Systems and Electronics at the Institute of Advanced Engineering, Doctor of Technical Sciences Sagdeev K.M.

PRACTICAL WORK No. 17

Subject: **STUDY COUNTERS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of sequential digital devices using universal packages applied computer programs;

– conduct study sequential digital devices on basis their circuit models,

– synthesis of sequential digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

TRAINING AND MATERIAL SUPPORT:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study counters.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study counters.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENT LABORATORY CLASSES

Brief theoretical or reference and information materials

Sequential or accumulating nodes of digital devices are nodes that contain memory elements, specifically triggers. Two types of accumulating nodes can be distinguished: registers and counters.

Counters

A counter is a device whose output signals reflect the number of pulses received at the counting input. Triggers can serve as an example of a simple counter: such counter considers to two. Counter, educated chain from ***m*** triggers,

can calculate 2^{m} *in binary code* pulses. Each of the triggers of such a chain is called a counter digit. The number ***m*** determines the number of digits of a binary number that can be written into the counter. The number $K = 2^{m}$ is called the coefficient (modulus) of the count.

Information is being removed With straight And (or) inverse outputs everyone triggers. IN pauses between input impulses triggers save their states, those. ***counter remembers the number of input pulses*** .

Zero state everyone triggers accepted for zero state counter V overall. The remaining states are numbered by the number of received input pulses. When the number of input pulses $N_{in} > K_{sc}$ an overflow occurs, after which the counter returns to zero state And cycle repeats. ***Coefficient accounts*** , like this in this way, ***characterizes the number of input pulses*** required to complete one cycle and return to the initial state. The number of input pulses and the counter state are mutually determined only for the first cycle.

After completion each cycle on exits last trigger arise voltage surges. This defines ***second appointment counters: division numbers input pulses .*** If the input signals are periodic and follow with a frequency F_{in} , then the frequency of the output signals is equal to $F_{out} = F_{in} / K_{count}$. In this case, the counting coefficient is called the division coefficient and is denoted as K_{div} .

In the division mode, the counter ***uses the output signal of only the last trigger,*** intermediate states the rest triggers in attention Not are accepted. Any counter can be used as a frequency divider. Therefore, such a device is often called a counter-divider. Such dividers have an integer division factor. However, the component base of modern microelectronics allows for the creation of dividers with fractional division factors.

The symbols for counters on diagrams are the letters CT (from English. counter – counter), after symbol put down number, characterizing module accounts (For example, 2 or 10 - ST2, ST10). ***The main operational indicators counter are capacity and performance*** . ***Capacity counter*** , numerically equal coefficient bills, equal number pulses per cycle. $_{The}$ ***counter's operating speed*** is determined by two parameters: resolution T_{times} . and the time of installation of the counter code T_{set} . ***Under the resolution imply*** the minimum time between two input signals, in during which no malfunctions occur. The reciprocal value of $F_{max} = 1/T_{times.}$ it's called maximum counting frequency. ***Code installation time*** T_{set} equal to the time between the moment of receipt input signal And transition counter V new sustainable state. These pa-dimensions depend from performance triggers And method their connections between by yourself.

Counters differ in the number and types of triggers, the methods of connection between them, the code, the accounting organization, and other indicators. ***Digital counters are classified according to the following parameters*** :

– ***counting factor*** : binary (binary); binary-decimal (decadal) or with another counting base; with an arbitrary constant and variable (programmable) counting factor;

– ***direction accounts*** : summing, subtractive And reversible;

– ***method of organizing internal connections*** : with sequential, parallel or combined transfer, ring.

Classification features are independent and can occur in different combinations : For example, summing counters there are How With consistent, So And With parallel transfer, they can have binary, decimal and other counting coefficients.

By introducing additional logical connections – reverse and direct – ***binary counters are transformed V non-binary*** . The greatest spreading received decimal (decadal) counters, working With $To_{the\ score} = 10$ V binary-decimal code (binary - By account code, decimal – by the number of states).

Decimal counters are organized from four-digit binary counters . The redundant six states are eliminated by introducing additional connections. Two possible options constructions schemes: check cyclically is coming from 0000 to 1001 And original The state is 0110 B = 6 D; the counting continues up to 1111 B = 15 D (B, D are the designations of binary and decimal numbers). The first option is used more often in practice.

IN summing counter every input pulse increases on unit a number written into the counter, where the transfer of information from one digit to another, higher one, occurs when the state changes from 1 to 0.

The subtracting counter operates in the opposite way : the binary number stored in the counter is decreased by one with each incoming pulse. The reading counter overflows counter is happening after achievements them zero states. Transfer from The transition from the least significant bit to the most significant bit occurs when the state of the least significant bit changes from 0 to 1.

Reversible counter Maybe work V quality summing And subtractive. These counters have additional inputs for setting the counting direction. The operating mode is determined by control signals at these inputs. In the EWB program, such counters are represented by the 74163 and 74169 ICs (K155IE18, IE17).

Carry-through counters are a chain of flip-flops in which impulses, subject account, are arriving on entrance first trigger, A signal The carry is transferred sequentially from one bit to another.

Main dignity counters With consistent transfer – simplicity diagrams. Increase bit depth is being carried out connection additional triggers To output of the last flip-flop. ***The main disadvantage of counters with serial carry*** is their relatively low speed, since the flip-flops fire sequentially, one after another. Counters of this class in The EWB library is represented by a 6-bit binary counter 4024 (176IE1).

The maximum counting frequency is determined by the operating mode . If the state reading counter should happen after each input impulse, How This has place , for example, when counting to a given number, then the maximum frequency is equal to $F_{max} = 1/[(m-1)T_{set} + T_{avg}]$, Where m - number discharges; T_{back} - delay switching one trigger; T_{sr} - response time of an external element or reading circuit.

Schemes four-digit binary counters sequential type on library D-triggers are shown in Fig. 1. Pulses from the clock signal output of the word generator, which are generated when the STEP key is pressed again, are fed to the counter inputs. Every trigger counters carries out division on 2, signal transfer transmitted consequently from one discharge To to another: For summing (rice. 1, A) - With straight outputs, for the subtractor (Fig. 1, b) - from the inverse ones. The states of the counter bits in binary code are indicated logical samplers, A V decimal - seven-segment indicator. As can be seen from Fig. 39, the number of pulses registered by the summing counter is $5 = 2^0 + 2^2$, and for the subtracting counter, the number of pulses to be subtracted is $6 = 2^1 + 2^2$.



a) b)

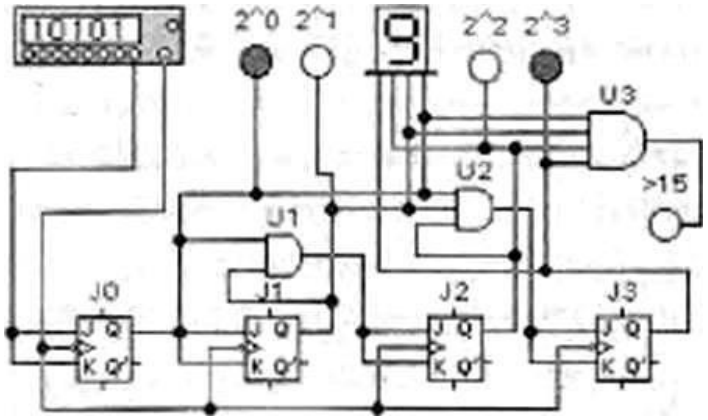
Rice. 1 - Counters sequential type

Counters With parallel transfer consist from synchronous triggers. Counting pulses are applied simultaneously to all clock inputs, and each of the triggers in the chain serves only as a source of information signals in relation to the subsequent ones. ***The triggers of the parallel counter operate synchronously*** , and the switching delay total counter equal delay one trigger. IN such counters JK- are used and D-triggers. Their circuit design is more complex than that of counters with serial carry. These counters typically have a small number of digits (4...6), since the number of internal logic connections increases rapidly as the number of digits increases.

Parallel-carry counters are used in high-speed devices . They have higher noise immunity, since in the pauses between pulses triggers counter blocked. ***TO their disadvantages follows take away*** Lower load capacity of individual bits due to the additional load from internal connections. The cascade preceding the counter must have sufficient power to drive the inputs of multiple flip-flops.

Counters with parallel carry (they are more often called synchronous) in the EWB library are represented by counters 74160, 74162, 74163 and 74169 (analogues - K155IE9, IE11, IE18, IE17 respectively).

Schematic of a four-bit parallel-carry counter using library JK triggers (rice. 2) contains additional logical elements For formations carry signals : U1 – at code 0011, U2 – at 0111, U3 – at 1111.



Rice. 2 – Parallel carry counter

In a parallel-serial carry counter , the flip-flops are grouped together so that individual groups form parallel carry counters, while the groups are connected in series. The groups can be there are also ready-made counters. Counters of this type, How rule, multi-digit. General coefficient accounts equal work counting coefficients of all groups. In terms of performance, they occupy an intermediate position.

Counter-dividers , designed as standalone components, are included in many series of integrated circuits. The range of counters is extremely diverse. Many of them have universal properties and allow you to control the counting coefficient and direction, enter a starting number before the start of a cycle, stop counting on command, and increment number discharges And etc. WITH help ready counters Can decide most practical tasks, emerging before developers equipment. If arises need V counters With atypical characteristics, That V this case They are being created from individual triggers and logic elements.

Designing a counter comes down to determining the number of triggers and organizing connections between them And logical elements, A Also calculation resolving counter capacity (maximum counting frequency).

At the first design step, the given counting (division) coefficient is transformed V binary code. Number discharges binary numbers shows, How many triggers must

have a counter, and the number of ones determines the number of inputs of the logical element. The inputs of the element are connected to the direct outputs Q of those triggers that correspond to the ones of the binary number. It should only be taken into account that the first input trigger displays the least significant discharge numbers. Exit logical element connects With entrances installations zero (inputs R) everyone triggers, from which made bends, A Also those, which directly for they are followed.

The design results are applicable to triggers of different types of logic, but the real schemes at this can differ V details. Because forced setting the R input to zero in some types of triggers is carried out by logical zero signals (TTL), at others - signals logical units (CMOS), V first case must be when applied logical element AND-NOT, in second AND. Except Togo, V summing counter overturning each subsequent trigger should happen Then, When signal on the output of the previous trigger changes from 1 to 0, so the order of connecting the triggers between is important by yourself. If V counter are applied triggers With straight management (By front $0 \rightarrow 1$), their inputs are connected to the inverse outputs of the preceding ones. In the case of flip-flops with inverse - control, the inputs are connected to the direct outputs. By adding a few additional elements to the original circuit, its capabilities can be expanded – creating a counter with a self-stopping (single-shot) function or providing a short-term pulse at the output of the last flip-flop in division mode.

Content practical work, performed students during the lesson

Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

- operating system Microsoft Windows,
- text CPU Microsoft Office Word or OpenOffice.org Writer,
- program circuit design modeling Electronics Workbench EWB 5.12.

Plan execution practical works:

Base level:

1) Research internal structure And logic functioning sequential three-bit counter using a word generator and a logic analyzer

2) To investigate the internal structure and operating logic of a modulo 5 counter using a word generator and a logic analyzer.

3) Research logic functioning binary reversible counter With the possibility of parallel recording of the initial code based on the 74169 IC (K155IE17) using a word generator and a logical analyzer.

Increased level

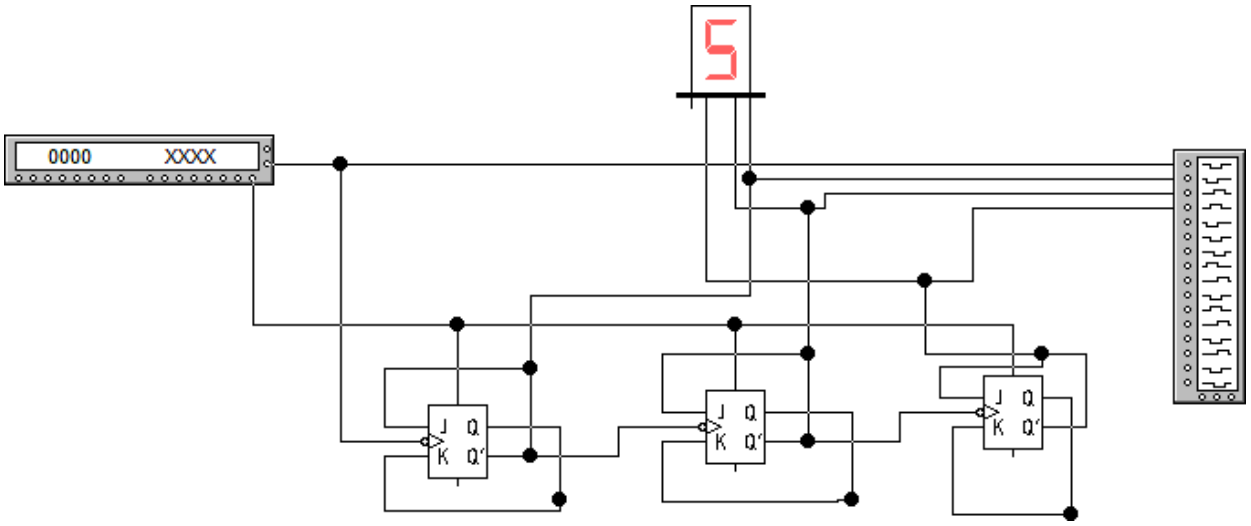
4) Conduct a study of the internal structure and operating logic of the counters contained in a given logic microcircuit.

Order execution works:

Exercise 1. Research internal structure And logic functioning a serial three-bit counter using a word generator and a logic analyzer.

To do this, follow these steps: actions:

1) Collect diagram research counter, depicted on rice 3.



Rice. 3 - Scheme research sequential three-digit counter

2) Analyze the internal structure counter, determine on the basis which trigger is the counter synthesized from?

3) For provision work counter sync pulses V generator words set the internal oscillator frequency to 1 kHz.

4) To reset the counter to its initial zero state, write the code 0001 into the word generator cell with address 0000, and leave the code 0000 in the remaining cells.

5) Organize a long cycle in the word generator, ending with the cell with the address 0099, set the word generator to the step-by-step mode.

6) IN logical analyzer install frequency internal generator, equal 4 kHz, to do this, press the Set button, and after setting, press the Accept button.

7) Launch being researched diagram V work V step by step mode, sequentially Press the Step button.

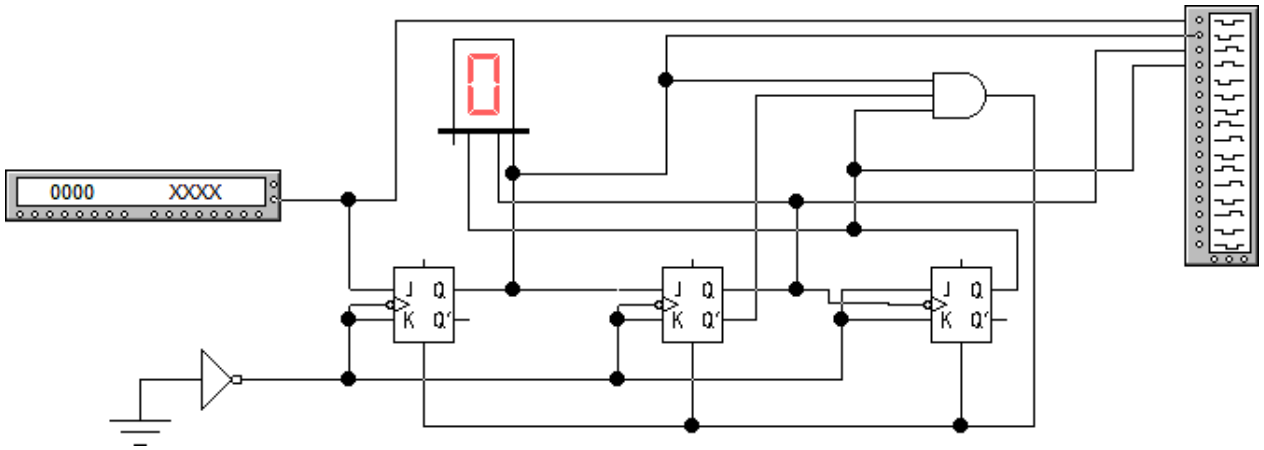
8) Analyze the timing diagrams of the meter's operation, display them in a report, and determine its counting coefficient.

9) Do it conclusions By results work done .

Exercise 2. Research internal structure And logic functioning modulo 5 counter using a word generator and a logic analyzer.

To do this, follow these steps: actions:

1) Assemble the counter research circuit shown in Fig. 4. The basis of the circuit is a T-trigger, implemented on the basis of a JK-trigger from the EWB library, located in Digital components.



Rice. 4 – Scheme of the counter research according to module 5

2) Analyze the internal structure counter, determine why additional logical elements are introduced into the circuit.

3) For provision work counter sync pulses V generator words set the internal oscillator frequency to 1 kHz.

4) Organize a long cycle in the word generator, ending with the cell with the address 0099, writing the code 0000 into all cells, set the word generator to the step-by-step mode.

5) Launch being researched diagram V work V step by step mode, sequentially Press the Step button.

6) Analyze the timing diagrams of the meter's operation, display them in a report, and determine its counting coefficient.

7) Do it conclusions By results work done .

Task 3. To investigate the operating logic of a binary reversible counter with the ability to record the initial code in parallel based on the 74169 (K155IE17) IC using a word generator and a logic analyzer.

To do this, follow these steps: actions:

1) Collect diagram research counter, depicted on rice 52.

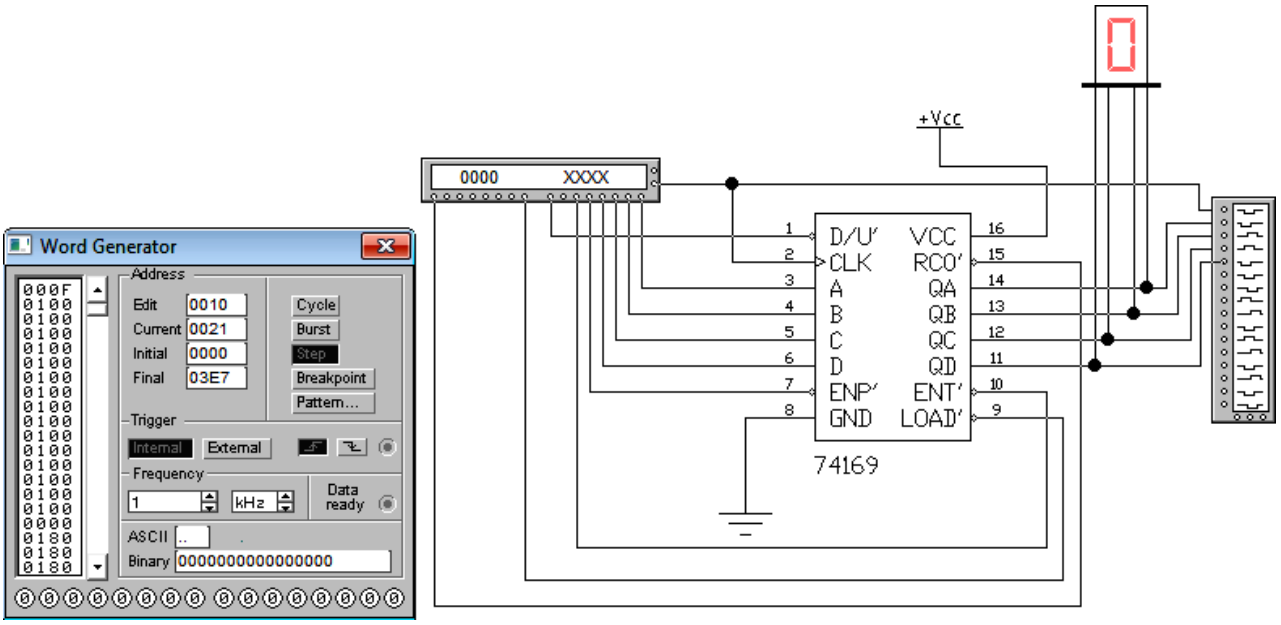
Peculiarities management IMS 74169 (K155IE17), located V Digital components in the additional panel 123… (Counters) are as follows:

– parallel loading V counter initial code is produced at filing on input LOAD' logical zero, while the low-level voltage received at the input of the parallel downloads LOAD, stops check And permits prepared on entrances A, IN, C, D data boot up V counter V moment parish next positive difference clock pulse (from low to high level or when transitioning from 0 to 1);

– counting is performed when there is a low level voltage (logical zero) at the inputs permissions accounts ENP' And ENT', intended Also For synchronous cascading several microcircuits to increase the counting coefficient;

– The counting direction is controlled by the D/U' input; when a logical one is supplied to this input, the microcircuit operates in the summing counter mode, and when a logical zero is supplied, it operates in the subtracting counter mode;

– reset counter is produced at filing on entrance RCO' logical unit.



Rice. 5 – IMS connection diagram 74169 (K155IE17)

2) Program the word generator by writing codes into its cells that ensure the execution of the following operations:

- initial loading V counter code 1111;
- subtractive check to 0000;
- initial loading V counter code 0101;
- summing check from 0101 to 1111;
- reset the counter.

3) Organize V generator words long cycle, providing sequential execution of all the listed operations, set the word generator to step-by-step mode.

4) Launch being researched diagram V work V step by step mode, sequentially Press the Step button.

5) Analyze the timing diagrams of the meter's operation, display them in a report, and determine its coefficients in the summing and subtracting counting modes.

6) Do it conclusions By results work done .

Task 4. Conduct a study of the internal structure and operating logic of the counters contained in a given logic microcircuit (high level).

Exercise 4 increased level is being carried out students on one's own By given options given in Table 1.

Table 1 - Table options For tasks 4

No. boil anta	**IMS**	**No. boil anta**	**IMS**
1.	74160 (K155IE9)	2.	7490 (K155IE2)
3.	74162 (K155IE11)	4.	7492 (K155IE4)
5.	74163 (K155IE18)	6.	7493 (K155IE5)
7.	74169 (K155ИЕ17)	8.	4017 (K561ИЕ8)
9.	74190 (KP1533ИЕ12)	10.	4024 (K561IE1)
11.	74191	12.	4040 (K1561ИЕ20)
13.	74192 (KP1533IE6)	14.	4510
15.	74293	16.	4516 (K561ИЕ11)
17.	74393	18.	4518
19.	7469	20.	4520 (K561ИЕ10)

IN this task necessary execute next actions:

1) Find the data sheet for a given microchip online. For this, you can use the website "Microchips..." – URL: https://www.microshemca.ru

2) Using the microcircuit's passport data, understand its purpose , operating principle, and typical application, and include in the lab report a description and internal structure of the microcircuit, and a table of its states.

3) Draw up a methodology for studying the microcircuit in such a way as to check its internal structure and operating logic specified in the passport data, and also to check all the given options for using the microcircuit.

4) Collect diagram research given logical microcircuits, having found her V EWB library , located in the Digital components (Digital nodes), using all the signal sources and measuring devices necessary for the study .

5) Conduct study internal structures And logic functioning for this logical microcircuit using the developed technique.

6) Do conclusions By results research.

Content report about work

IN In the report, please provide:

- topic And target work work ,
- plan work;
- brief abstract theoretical material;
- designs ;
- results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, voltage diagrams, etc.;
- conclusions O done work.

Control questions For preparation To report protection :

1) List and characteristics of sequence (accumulative) digital devices.
2) Order research internal structures And logic functioning sequential three-digit counter With help generator words And logical analyzer.
3) The procedure for studying the internal structure and operating logic of a modulo counter using a word generator and a logic analyzer.
4) The procedure for studying the logic of operation of a binary reversible counter With opportunity parallel records initial code on basis IMS 74169 (K155IE17) using a word generator and a logic analyzer.

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 18

Subject: **STUDY OPERATIONAL AND CONSTANT IN MEMORY, DEVICES INPUT- OUTPUT**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of sequential digital devices using universal packages applied computer programs;

– conduct study sequential digital devices on basis their circuit models,

– synthesis of sequential digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

TRAINING AND MATERIAL SUPPORT:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study operational And constant memory.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study devices input- output.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENT LABORATORY CLASSES

Brief theoretical or reference and information materials

Random access memory (RAM) ***is*** an integral part of personal computers for various purposes; ***they are divided into two classes*** : static and dynamic. In static RAM memorization information is produced on triggers, A V dynamic - on capacitors capacity order 0.5 pF. Duration storage information V static

RAM Not limited, Then How V dynamic she limited time self-discharge capacitor , which requires special regeneration means and additional time costs for this process (about 5... 12% of the system's operating time).

The evolution of dynamic RAM chips is closely linked to the evolution of personal computers. In the first IBM PCs, RAM was implemented on chips with a capacity of 16 Kbit each. A year later, performances IBM PC/XT (first PC) appeared microcircuits capacity 64 Kbit, Moreover , one such microcircuit was cheaper than four 16 Kbit ones. In 1984, another step was taken By increase volume memory V one body - appeared 256-kilobits The microchips that were installed on the first IBM PC/AT. Then, 1-Mbit microchips were developed , and later, dynamic RAM components began to appear in other designs, with a continuous trend toward increasing capacity.

Structurally, any RAM consists of two blocks - a matrix of storage elements and an address decoder. For technological reasons, the matrix most often has a two-coordinate decryption addresses - By lines And columns. On rice. 3 shown 16-bit static RAM matrix: it consists of 16 memory cells ***mem_ i*** , the diagram of which is shown in Fig. 4.

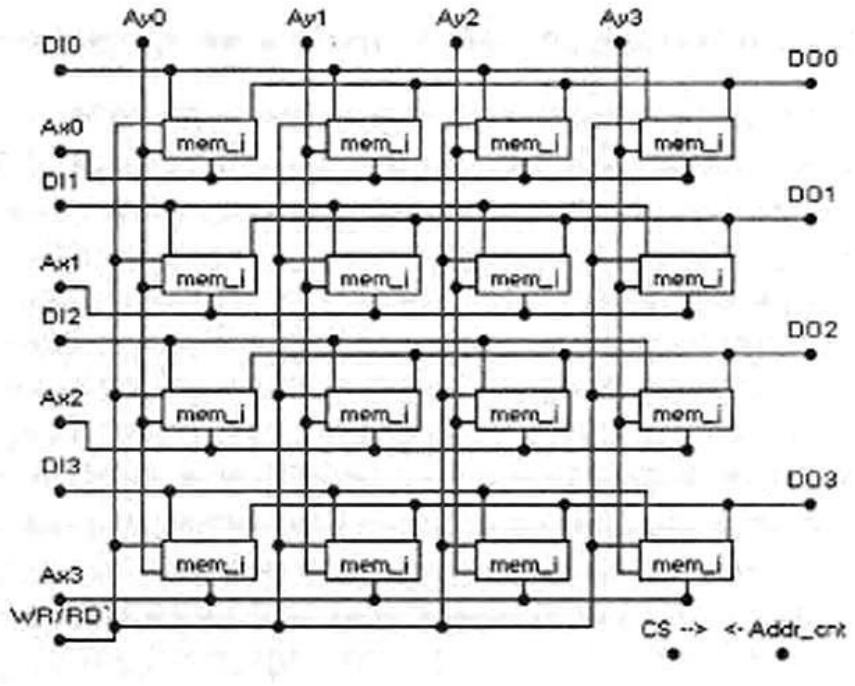
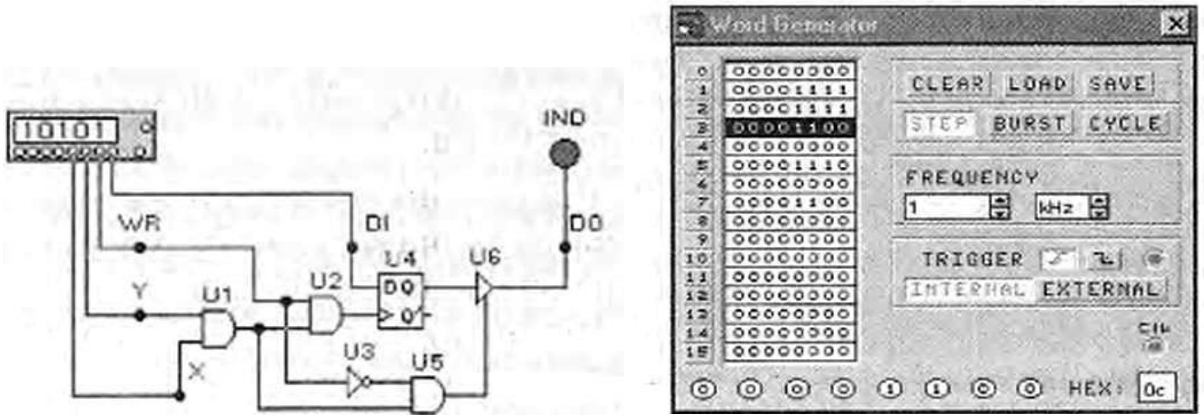


Fig. 3 – 16-bit RAM matrix

Each one cell memory addressed By entrances X, Y by way choice decoders address lines By lines Ah0...Ah3 And By columns Ay0...Ay3 (cm. rice. 4) And filing By selected lines signal logical units. At this V selected cell memory it works two-input AND element (U1), preparing the read-write circuits for information on the input DI0...DI3 or output DO0...DO3 bit buses. The enable signal for outputting the address is CS (chip select - choice crystal), which is served on entrance permissions chick's bill addresses (Addr_cnt) or such same entrance decoders, connected To exits counter. When records V cell memory (cm. rice. 4) on corresponding discharge tire data 1 or 0 is set, at the input WR/RD' – signal 1 and after strobing the counter or decoders addresses signal CS are triggered elements 2I U1, U2. Positive difference The signal from element U2 is fed to the clock input of D-trigger U4, as a result of which 1 or 0 is written into it depending on the signal level at its D-input.

When reading from a memory cell, the WR/RD' input is set to 0, and the following are triggered: elements U1, U3, U5 And on entrance permission exit buffer element U6 arrives

enable signal, as a result of which the signal from the Q output of the D-trigger is transmitted to the DO0...DO3 data bit bus. A word generator is used to check the functioning of the memory cell (Fig. 4).



Rice. 4 - Scheme cells memory mem_i With facial panel generator words With installed kami For cells memory

access memory (***SRAM) devices*** are characterized by high performance and are used sparingly in microprocessor systems due to their relatively high cost . In such systems, they are used only as so-called cache memory **.** (stock) means fast-acting buffer memory between processor And basic memory, employee For partial compensation differences V speed processor And main memory - the most frequently used data is stored in it. When the processor first accesses a memory cell, its contents are copied into the cache in parallel, and in case of repeated appeals Maybe be With much greater speed from her extracted. At When writing to memory, information is put into the cache and simultaneously copied into memory (Write Through scheme ***)*** or copied after some time (Write Back scheme) - ***reverse recording***). At reverse records, called Also buffered with through write, information is copied into memory in the first free cycle, and with delayed write, when there is no free area to place a new value in the cache ; at this V main RAM are being displaced relatively rarely used data. Second Paradise scheme more effective, But And more complicated for check necessity maintenance correspondence between the contents of the cache and the main memory.

Cache memory consists of from areas data , broken on blocks (lines), which are the elementary units of information when the cache is running, and the tag ***area*** describes the state of the lines (free, busy, marked for rewriting, etc.). They are mainly ***used two schemes organizations cache*** : ***With straight display*** (direct mapped), when everyone address memory Maybe cache only one line (V this case number The number of lines is determined by the least significant bits of the address, and n ***-way associative*** , when each address can be cached by several lines. Associative caches are more complex, but allow for more flexible caching; four-way associative cache systems are the most common.

Microprocessors 486 And higher have Also interior (Internal) cache volume 8... 16 KB. It is also designated as Primary or L1 (Level 1) in contrast to the external one (External), located on the board and designated Secondary. or L2. ***IN most processors interior cache works By scheme With direct recording*** , A V 486 (CPU Intel P24D And latest DX4-100, AMD DX4-120, 5x86) And Pentium can also work with write-back. The latter requires special support from systemic boards, to at exchange By DMA (direct appeal To memory input/output devices) Can was support consistency data V memory And internal

cache. ***Processors Pentium Pro And higher have Also built-in cache second level*** volume 256, 512 or 1024 Kbytes With own controller And local 64-bit data bus operating at the internal frequency of the microprocessor; additional internal optimization is used, accelerated Job conveyor And degree parallelism, improved system branch prediction (Dynamic & Speculative Execution).

IN microprocessor systems V quality RAM more often total are used Dynamic RAM with a storage capacitor , which are distinguished by a wide variety. We will provide data on the most common types of such RAM.

In dynamic random access memory (***DRAM***), cells are made from charge accumulation areas, which occupy a much smaller area than flip-flops and consume virtually no energy when storing information. When a bit is written to such a cell, an electric charge is generated in it, which is retained for several milliseconds; For permanent preservation charge cells necessary regenerate (rewrite) its contents. ***The cells of dynamic memory chips are also organized in the form of a rectangular matrix*** : when accessing the chip, its inputs at the beginning is served address lines matrices, accompanied signal ***RAS*** (Row Address Strobe – ***row address strobe***), then, after some time – column address, followed by signal ***CAS*** (Column Address Strobe - ***strobe addresses column***). At each When accessing a single cell, all cells in the selected row are regenerated, so to completely regenerate the matrix, it is sufficient to iterate through the row addresses. Dynamic memory cells have a relatively low performance (tens to hundreds of nanoseconds), but a high specific density (on the order of several megabytes per unit) and lower power consumption.

Conventional RAM is often referred to as asynchronous , as address setting and control signaling can occur at arbitrary points in time; only the timing relationships between these signals must be maintained. They include so-called guard intervals, which are necessary for signal establishment. Synchronous memory also exists, receiving an external clock signal whose pulses are rigidly tied to the timing of address setting and data exchange: these types of memory allow for more complete use of internal pipelining and block access.

FPM DRAM (Fast Page Mode DRAM – ***dynamic memory with fast page access***) differs from conventional dynamic memory in that after selecting a matrix row And deductions signal RAS allows multiple installation addresses column, strobed by the CAS signal, as well as fast regeneration using the " ***CAS before RAS*** " scheme. The first allows for faster block transfers when the entire data block or part of it is located within one row of the matrix, called a page in this system, and the second allows for a reduction in the time spent on memory regeneration.

EDO (Extended Data Out ***)*** is actually represent by yourself ordinary microcircuits FPM, on exit which installed Data latch registers. During paging, such chips operate in a simple pipeline mode: they hold the contents of the last selected cell at the data outputs, in That time How on their entrances already is served address next selectable cells. This This memory speeds up the reading of sequential data arrays by approximately 15% compared to FPM. With random addressing, this memory is no different from conventional memory.

BEDO (Burst EDO - EDO With block access) - ***memory on basis EDO, not working single, A packaged cycles read/write*** . Modern processors thanks to the internal and external caching teams And data exchange With basic memory primarily blocks words maximum width. At availability memory BEDO There is no need to constantly supply sequential addresses to the inputs of microcircuits while maintaining the required time delays; it is sufficient to strobe the transition to the next word with a separate signal.

SDRAM (Synchronous DRAM - synchronous dynamic memory) - ***memory With synchronous access*** , working faster than the usual asynchronous (FPM/EDO/BEDO). In addition to synchronous access, SDRAM uses internal partitioning of an array memory on two independent jar, What allows combine sample from one jar With installation addresses V other. SDRAM also supports block exchange. ***The main advantage of SDRAM is*** the support of sequential access in synchronous mode, where no additional bars expectations. At random access SDRAM works practically With that one same speed , the same as FPM/EDO.

RV SRAM (Pipelined Burst SRAM - static memory With block conveyor (Access memory) is ***a type of synchronous SRAM with internal pipelining*** , which approximately doubles the speed of data block exchange.

DDR SDRAM (Double Data Rate SDRAM ***)*** - initially, this type of memory was used in video cards, but later support for DDR SDRAM appeared from chipsets. Memory DDR SDRAM operates at frequencies of 100, 133, 166 and 200 MHz, its full access time is 30 and 22.5 ns, and the operating time is cycle - 5; 3.75; 3 And 2.5 ns. So How frequency synchronization lies V within from 100 to 200 MHz, and data is transmitted 2 bits per clock pulse, both on the front and on the edge of the clock impulse, That effective frequency transmissions data lies V within from 200 to 400 MHz. Such memory modules are designated DDR200, DDR266, DDR333, and DDR400.

DR DRAM (Direct Rambus DRAM) is ***a type of synchronous memory; it is equipped with a special interface firms Rambus*** , For connections With controller memory A special high-speed Rambus Channel bus is used, which allows the use of a clock frequency of 400 MHz and exchange on both pulse edges, i.e. exchange with a frequency of 800 MHz, which corresponds to a throughput of 1.6 Gbit/s; with the maximum possible number of channels 4, the throughput increases to 6.4 Gbit/s.

DDR2 SDRAM – a structurally new type of RAM DDR2 SDRAM was released V 2004 year. Based on on technologies DDR SDRAM, this type memory for check technical changes shows higher performance and is intended for use on modern computers. Memory Maybe work With clock frequency tires 200, 266, 333, 337, 400, 533, 575 And 600 MHz. At this effective frequency transmissions data correspondingly

The corresponding frequencies will be 400, 533, 667, 675, 800, 1066, 1150, and 1200 MHz. Some memory module manufacturers, in addition to standard frequencies, also produce samples that operate at non-standard (intermediate) frequencies. These are intended for use in overclocked systems. Where required stock By frequency. Time complete access - 25; 11.25; 9; 7.5 ns And less. The duty cycle time is from 5 to 1.67 ns.

DDR3 SDRAM - this type memory founded on technologies DDR2 SDRAM with twice as much increased frequency transmissions data By tire memory. It is different reduced power consumption compared to its predecessors. The bandwidth frequency ranges from 800 to 2400 MHz (record frequencies – more 3000 MHz), What provides big throughput compared to all predecessors.

Except main RAM, ***device memory supplied And device display information - videographic system*** . Such memory ***it's called video memory and is located on the video adapter board*** .

Video memory is used to store images . The maximum performance depends on its volume. possible permission video cards - A X IN x C, Where A - quantity points By horizontal, B – vertical, C – the number of possible colors for each pixel. For example, for a resolution of 640 x 480 x 16, 256 KB of video memory is sufficient, for 800 x 600 x 256 – 512 KB, For 1024 x 768 x 65536 (other designation - 1024 x 768 x 64k) - 2 MB And etc. Since an integer number of bits are allocated for storing colors, the number of colors is always an integer power of 2 (16 colors - 4 bits, 256 - 8 bits, 64k - 16, etc.).

IN video adapters are used the following types of video memory .

FPM DRAM (Fast Page Mode Dynamic RAM ***)*** is the primary type of video memory, identical to that used in motherboards. It was widely used until 1996. The most common FPM DRAM chips are four-bit DIP and SOJ, as well as sixteen-bit SOJ.

VRAM (Video RAM) is the so-called ***dual-port DRAM with support simultaneous access with sides video processor And central processor computer .*** Allows for the simultaneous display of images on the screen and their processing in video memory, which reduces delays and increases operating speed.

EDO DRAM (Extended Data Out DRAM - dynamic RAM With extended output data retention time) – ***memory with pipelining elements*** , which allows to speed up the exchange of data blocks with video memory.

SGRAM (Synchronous Graphics RAM - ***synchronous graphic RAM***) - option DRAM with synchronous access, When All managers signals are changing simultaneously With system clock signal, which helps reduce time delays.

WRAM (Window RAM ***)*** is EDO VRAM in which the window through which the video controller accesses is made smaller than the window for the central processor.

MDRAM (Multibank DRAM (***Dual-Bank Random Access Memory***) is a variant of DRAM organized as multiple independent banks of 32 KB each, operating in a pipelined mode.

Increasing the speed of the video processor's access to video memory , in addition to increasing the adapter's throughput, allows for an increase in the maximum ***image regeneration frequency*** , which reduces operator eye fatigue.

Microchips memory have four main characteristics - type, volume, structure and access time. ***The type indicates*** static or dynamic memory, ***the volume shows*** general capacity memory, A ***structure*** - quantity cells memory And bit depth each cell. For example, 28/32-pin DIP SRAM chips have an 8-bit structure (8K x 8, 16K x8, 32K x 8, 64K x 8, 128K x 8), cache volume 256 Kbytes consists of from eight 32K x 8 microcircuits or four 64K x 8 microcircuits (we are talking about the area (data, additional chips for storing features may have a different structure). Two 128K x 8 chips cannot be installed, since a 32-bit data bus is required, which can only be provided by four chips. Common 100-pin PQFP SRAMs have a 32-bit structure (32K x 32 or 64K x 32) and are used in pairs or fours in Pentium boards.

30-pin SIMMs have an 8-bit structure and are used with 286 processors, 386SX And 486SLC By two, A With 386DX, 486DLC And ordinary 486DX - By four. 72-pin SIMMs have a 32-bit structure and can be used with the 486DX one at a time, and with the Pentium and Pentium Pro - two at a time. 168-pin DIMMs have a 64-bit structure and are used V Pentium And Pentium Pro By one. Installation modules memory or microcircuits A cache in an amount greater than the minimum for a given system (motherboard) allows for faster work with them using the interleave principle.

Time access characterizes speed work microcircuits And usually indicated in nanoseconds after dash V at the end names. On more slow microcircuits can only the first digits are indicated (7 instead of 70, 15 instead of 150), on faster static ones "15" or 20 means real time access To cell. Often on microcircuits the minimum of all possible access times is indicated, for example, it is common to mark 50 EDO DRAM instead of 70, or 45 instead of 60, although such a cycle is achievable only in block mode , and in single mode the chip still has an access time of 70 or 60 ns. Similar situation has place And V marking RV SRAM: 6 instead of 12 And 7 instead of 15. SDRAM chips are typically labeled with block mode access times of 10 or 12 ns.

IMS memory are being implemented V buildings the following types:

DIP (Dual In-line Package ***)*** – classic microcircuits , applied V blocks basic memory IBM PC/XT And early PC/AT, Now are used in cache memory blocks.

SIP (Single In-line Package) is a microcircuit with one ***row*** of pins, installed vertically.

SIPP (Single In-line Pinned Package ***)*** is a memory module that fits into a panel like a DIP/SIP chip; it was used in early IBM PC/AT.

SIMM (Single In-line Memory Module) – a memory module with ***one row of contacts*** memory, insertable V clamping connector; applies in everyone modern boards, As well as in many adapters, printers, and other devices, a SIMM has contacts on both sides of the module, but they are all connected together, forming a single row of contacts. SIMMs currently primarily use FPM/EDO/BEDO chips.

DIMM (Dual In-line Memory Module) – a ***memory module with two rows of contacts*** memory, similar on SIMM, But With separate contacts (usually 2 x 84), for check which increases the bit depth or the number of memory banks in the module. DIMMs are equipped with EDO/BEDO/SDRAM/DDR chips. SDRAM memory modules are the most common V view 168-pin DIMM modules, memory type DDR SDRAM - V view 184-pin modules, and DDR2, DDR3 modules are 240-pin modules.

CELP (Card Edge Low Profile – ***a low card with a blade connector on the edge***) – module external cache memory, assembled on microcircuits SRAM (asynchronous) or RV SRAM (synchronous). By external view similar on 72-pin SIMM, has capacity 256 or 512 KB. Another name is COAST (Cache On A STick).

SO-DIMM (Small outline DIMM) – analogues of DIMM modules in a compact design to save space, intended for portable and compact devices (Mini-ITX form factor motherboards, laptops, notebooks, tablets, etc.), as well as printers, network and telecommunications equipment.

RIMM (Rambus In-line Memory Module) - module memory For DR DRAM. They are - presented in 168- and 184-pin varieties, and on the motherboard such modules must be installed only in pairs, otherwise special dummy modules are installed in empty slots (this is due to the design features of such modules).

In addition to the main memory cells, ***dynamic memory modules may have additional cells for storing*** parity bits for data bytes; such SIMMs are sometimes called 9- and 36-bit modules (one parity bit per data byte). Parity bits are used to verify the correctness of data reading from the module, allowing for the detection of some errors. Modules with parity bits make sense only in applications that require increased reliability. Carefully tested modules without parity bits are also suitable for routine applications, provided that the system board supports these types of modules.

Easier total define type module By marking And quantity microcircuits memory on it: for example, if on a 30-pin SIMM there are two microcircuits of one type and one of another , That two first are main (each - By four discharge), A third intended for storage bits parity (she single-digit). IN 72-pin SIMM With twelve Eight of the chips store data, and four store parity bits. Modules with 2, 4, or 8 chips do not have memory for storing parity bits.

Sometimes modules are equipped with a so-called parity simulator—a microchip that always outputs the correct parity bit when reading a cell; it is intended for installation in boards where parity checking cannot be disabled.

72-pin SIMMs have four special PD lines (Presence Detect – detection availability), on which at help jumpers Maybe be installed to 16 combinations signals. Lines PD are used V some maternal boards For definitions

availability modules memory V connectors And their parameters (volumes And performance). IN most universal boards production "third firms", How And released by them SIMM, PD lines are not used.

IN modules DIMM V in accordance with specification JEDEC technology PD is realized when help rewritable ROM With consistent access (Serial EEPROM) And is called Serial Presence Detect (SPD). The ROM is an 8-pin chip located V corner boards DIMM, A his content describes configuration And parameters module .

Constant memorizing devices (ROM) are divided pa four type :

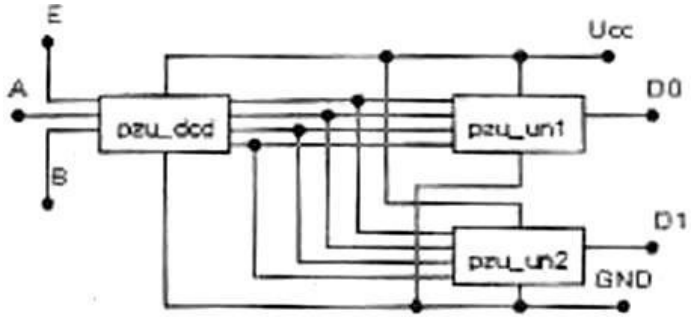
1) masked, programmable on at the manufacturer's plant With application special masks;

2) one-time programmable consumer by way burning out nichrome or polysilicon jumpers;

3) repeatedly programmable consumer with erasure recorded information by ultraviolet radiation;

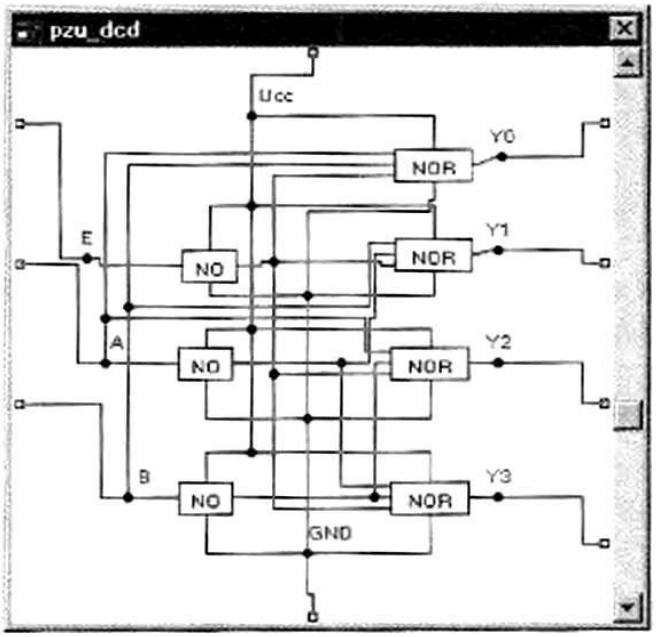
4) repeatedly programmable consumer With electric erasure information-tions.

Let's consider ***ROM second type*** , which ***consists of from*** decoder ***n X 2 n*** And connect-OR circuits connected to its outputs with fusible jumpers (Fig. 5). The ROM contains a 2x4 decoder in the form of a ***pzu_dcd subcircuit*** (A, B are code inputs, E are enable inputs, an active high-level signal), to the outputs of which four 4OR elements with additional devices. On rice. 5 shown two such element, completed V As separate subcircuits ***, pzu_ur.l*** and ***pzu_un2*** . Although these elements are identical, copying them onto the circuit is impossible due to the presence of fuseable jumpers: if there are subcircuits with the same name, burning a jumper in one subcircuit will automatically burn the same jumper in the other. Since the program does not allow copying subcircuits with renaming, they must all be implemented separately. In the circuit, D0 and D1 are the outputs of the least significant and first digits.

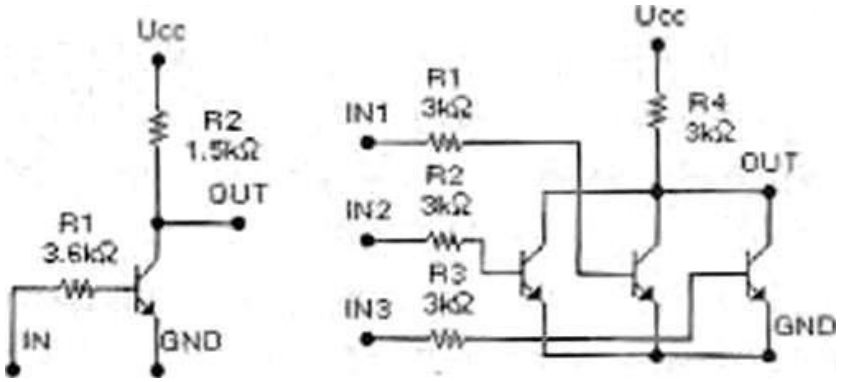


Rice. 5 - Scheme two-bit ROM

The decoder pzu_dcd (Fig. 6) is implemented on three NOT elements and four elements ZIL-NOT on transistors (Fig. 7).



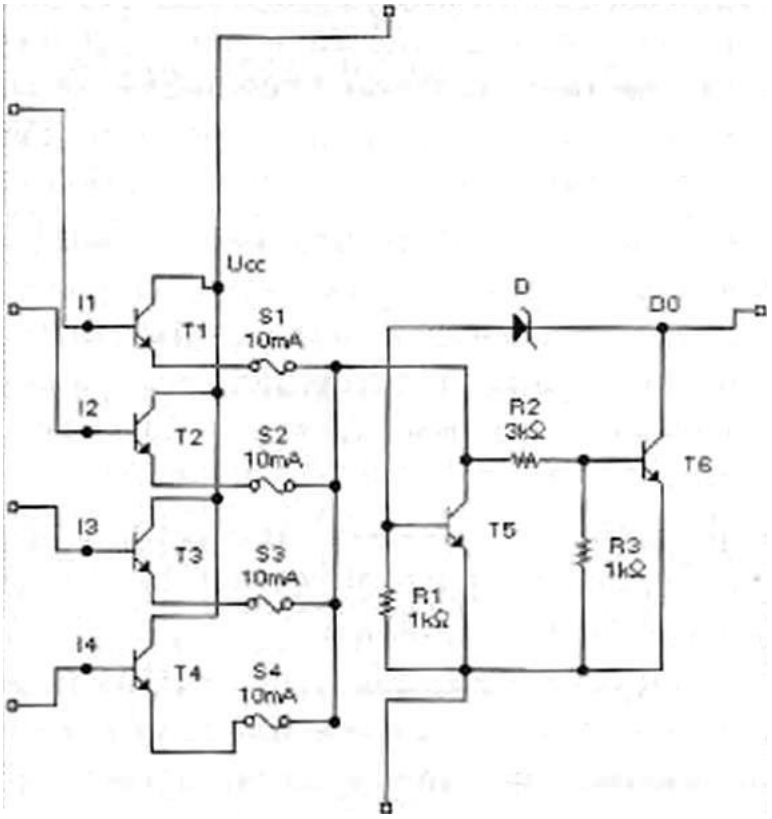
Rice. 6 - Internal structure decoder subcircuits



a) b)

Rice. 7 - Schemes elements NO (A) And OR-NOT (b)

Necessity execution elements decoder on transistors is explained by the fact that used V program EWB models digital IMS Not Always allow connect conventional transistor circuits to them, and in particular, the memory cells used in the ROM under consideration in the form of the pzu_uni subcircuit. Its internal structure is similar to the cell structure memory, used V ROM K155RES (rice. 8). IN difference from IMS K155RES, V in which a multi-emitter transistor is used as an OR element, in Fig. 9.51 separate transistors T1...T4 are used, the emitters of which are connected through blown jumpers S1...S4 (simulated by 10 mA fuses) to the driver on transistors T5, T6 and zener diode D. Transistor T5 and zener diode D are used only in the mode programming And V working mode Not provide influences on work weekend cascade on transistor T6 (cascade with an open collector), since transistor T5 is closed by a low potential at its base (the breakdown voltage of the zener diode D is chosen to be slightly higher voltage nutrition transistor T6, served in second subcircuit V point D0 or D1 through a load resistor).



Rice. 8 - Internal structure cells memory two-digit ROM

Cell ROM works next way . IN original condition transistors T1 ... T4 And T6 closed, And at connected To T6 load on his exit D0 is being formed logical signal units (near + 5 IN). At filing on entrances A, IN decoder given code combination, A on entrance permissions E - signal logical units, one from transistors T1 ... T4 will open and a logical zero signal will be generated at the output D0. For example, when A=B=1 will open transistor T4 And signal logical units With his emitter through jumper S4 will arrive on divider on resistors R2, R3, transistor T6 will open, And on his exit is formed signal logical zero. Obviously, What And at any another binary The combination will continue to do the same until the corresponding jumper is destroyed .

Burning out the jumpers is the essence of programming and is carried out separately for each digit (each cell) as follows :

– a binary combination is fed to inputs A, B (see Fig. 5), corresponding to the address of the fuse jumper in the programmable bit (in the ***pzu_unx cell*** , where x is the cell number);

– to the output of the Dx cell through a load resistor (its resistance for specific ICs is indicated in the documentation, for K155REZ it is about 300 Ohm), a 12.5 V voltage source is connected, V as a result of which the zener diode D breaks down and the transistor T5 opens;

– a logical one signal is applied to the enable input E for a short time, while a current sufficient to burn out the corresponding jumper flows through one of the open transistors T1...T2 and T5 (the duration of the enable signal at the input E in industrial programmers can automatically increase after several unsuccessful attempts to program the same cell);

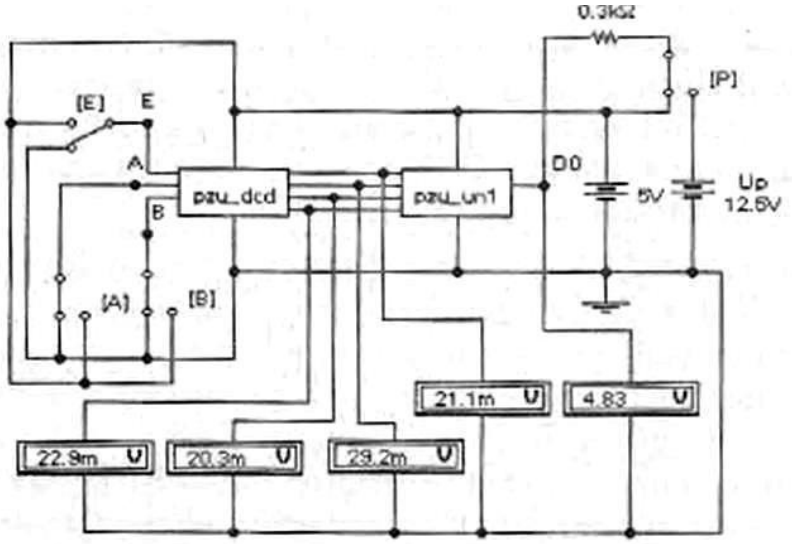
– the 12.5 V source is disconnected; after opening the corresponding subcircuit, you can verify that the jumper is actually destroyed (in industrial programmers this process comes down to To verification records programmable cells And at negative result

re-programming is performed with a longer duration of the enabling signal).

The final stage of programming serial ROM chips in industrial conditions is electrothermal training, which is being carried out cup total V for 168 hours at an elevated temperature, after which additional monitoring of the recorded data is carried out information. If at this is discovered error, allowed repeated about programming. If the error recurs, the chip is rejected.

To simulate the programming process, additional elements must be connected to the programmable circuit . It is advisable to begin the simulation with a single-bit ROM (Fig. 9).

It should be noted that the considered ROM model (both in Fig. 9 and Fig. 9) is quite capricious And at some combinations input signals modeling Not is being performed . A sign that modeling is impossible is the absence of a table with indication of time intervals to the left of the power switch (in the upper right corner of the screen). After some time, a recommendation to change the setting may be issued. errors modeling (By default she equal 1%). It is advisable set it to the maximum possible (10%) in the Circuit menu (Analysis Options command, Tolerance parameter). It is also advisable to vary the resistances of the input resistors and resistors loads elements NOT And OR-NOT (rice. 7), A Also try change transistor parameters. In extreme cases, you can limit yourself to the simplest case – do without a decoder And use only one cell memory (cm. rice. 8), having connected To exit And to one of its inputs additional element as shown in Fig. 9.



Rice. 9 - Model ROM With additional elements

ROM With burnt-out jumpers are used more often total V quality specialized decoders, for example, for the selection of explosives.

UV-erasable ROMs are used in microprocessor systems to store control programs, in particular to house ***the BIOS*** (Basic Input/Output System, hence its full name – ROM BIOS). BIOS is a set of programs for checking and servicing hardware. computer And performs role intermediary between operating rooms system (OS) and the PC hardware. BIOS takes control when the motherboard is turned on, tests myself fee And main blocks computer - video adapter, keyboard, controllers disks and I/O ports, configures the board's chipset and loads the external OS. When running DOS/Windows 3.x/95/98, the BIOS controls the main devices; when running under OS/2, Unix, Windows NT BIOS practically Not is used, performing only initial testing and setup.

Usually, the motherboard only has ***a ROM with the system*** (Main System) ***BIOS*** , which is responsible for the board itself and the FDD (floppy disk) and HDD (hard disk) controllers. ports And keyboards; V system BIOS practically Always enters System Setup - System setup program . Video adapters and HDD controllers with ST-506 (MFM) and SCSI interfaces have their own BIOS in separate ROMs; other boards, such as intelligent disk and port controllers, network cards, etc., may also have them.

Usually BIOS For modern systemic boards is being developed one from specialized firms: Award Software, American Megatrends (AMI), less often: Phoenix Technology, Microicl Research. Some manufacturers boards (For example, IBM, Intel And Acer) ourselves are being developed BIOS For them. Sometimes For one And that one same boards there are versions BIOS different In - this case, it is permissible to copy firmware or replace ROM chips; in general, each BIOS version is tied to a specific board model.

Previously, BIOS was placed in one-time programmable ROM or ROM UV -erasable; currently, most boards are manufactured ***with electrically erasable ROM*** (flash ROM), which allows the BIOS to be reprogrammed directly from the board itself. This allows for correcting factory errors in the BIOS, changing factory default settings, programming custom screensavers, etc.

Type ROM chips usually Can define By marking : 27xxxx - Regular ROM, 28xxxx or 29xxxx – reprogrammable. If the 27xxxx chip has a transparent window on the housing, it's a UV-erasable ROM; if not, it's a one-time programmable ROM, which can only be replaced with another one.

Video ROM (Video ROM) - permanent memorable device, V which video BIOS, screen fonts, service tables, etc. are recorded. ROM is not used by the video controller directly, it is accessed only by the central processor as a result of execution programs, recorded V volume same ROM. On many modern video cards lips are filled with tears electrically reprogrammable ROM (EEPROM, Flash ROM), allowing rewriting by the user under the control of a special program included with the card.

ROM is only required for the initial launch of the video adapter and operation ; in mode DOS, Novell Netware And others OS, functioning predominantly V text mode; Windows, OS/2 and similar operating systems that operate through their own video drivers do not use ROM to control the adapter or use it only when running DOS programs.

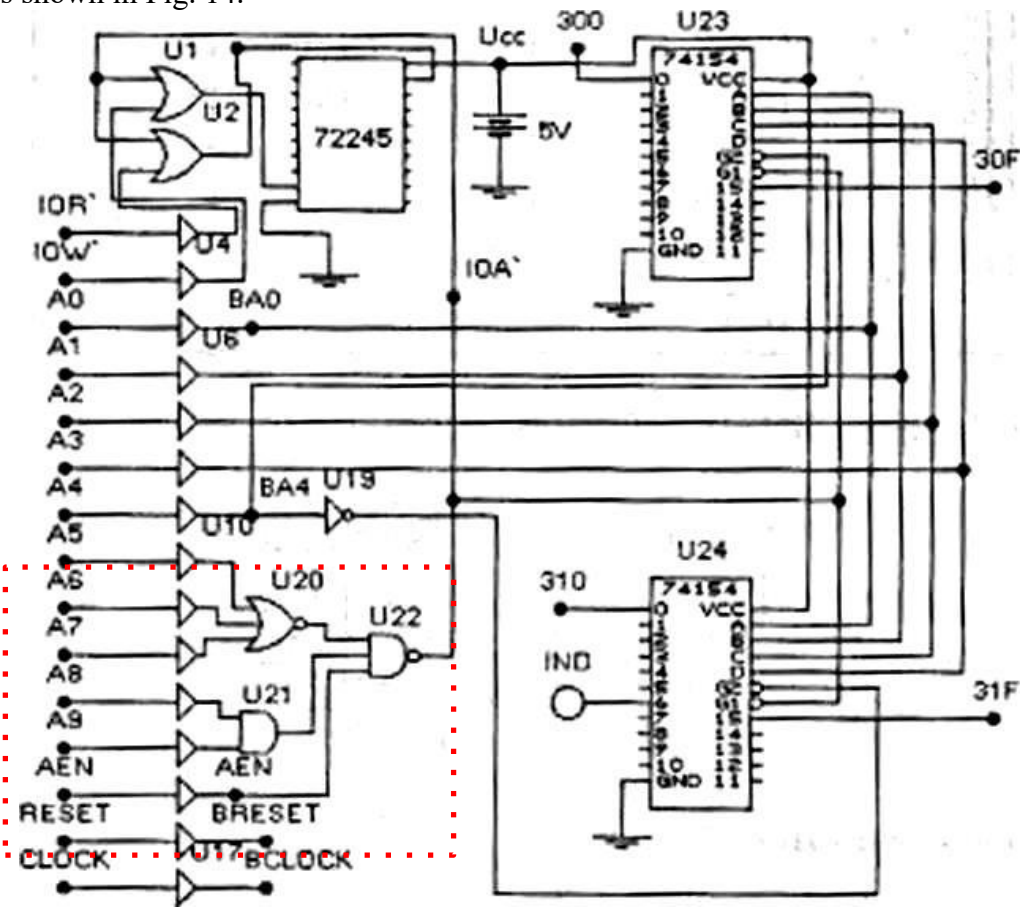
When creating a video BIOS, all developers adhere to the recommendations of VESA and VBE. VESA (Video Electronics Standards Association) – an organization that issues various standards in the field of electronic video systems And their software provision. VBE (VESA BIOS Extension - extension BIOS V VESA standard) – additional video BIOS functions in relation to the standard video BIOS for VGA, allow query the adapter for a list of supported video modes and their parameter (permission, color, methods addressing, scan And etc.) And change these parameters For approvals adapter With specific monitor. By in essence, VBE is unified software interface standard with VESA-compatible cards, when working through video BIOS He allows get by without specialized drivers video cards.

Devices input- output

Usage microprocessor techniques V systems automatic management primarily related to the organization of input-output. ***One of the most common methods of input-output*** is software-controlled, in which the interfacing of external devices with the processor is carried out through the system bus by a set of hardware funds, providing selection devices input-output (processor COMPUTER. IN In a popular personal computer (PC) from IBM, 32 addresses (from 300 $_{N)}$ are reserved in the input-output address space. up to 31F $_{H}$ in hexadecimal code) to enable their use at conducting various experiments By application PC V quality

control computer. For such purposes, various companies, including IBM, manufacture so-called breadboards with ISA-type blade connectors. Their design allows for the placement of ICs with varying numbers of pins and then connecting them with wiring. Some boards already contain buffer elements, address selectors, and bus formers.

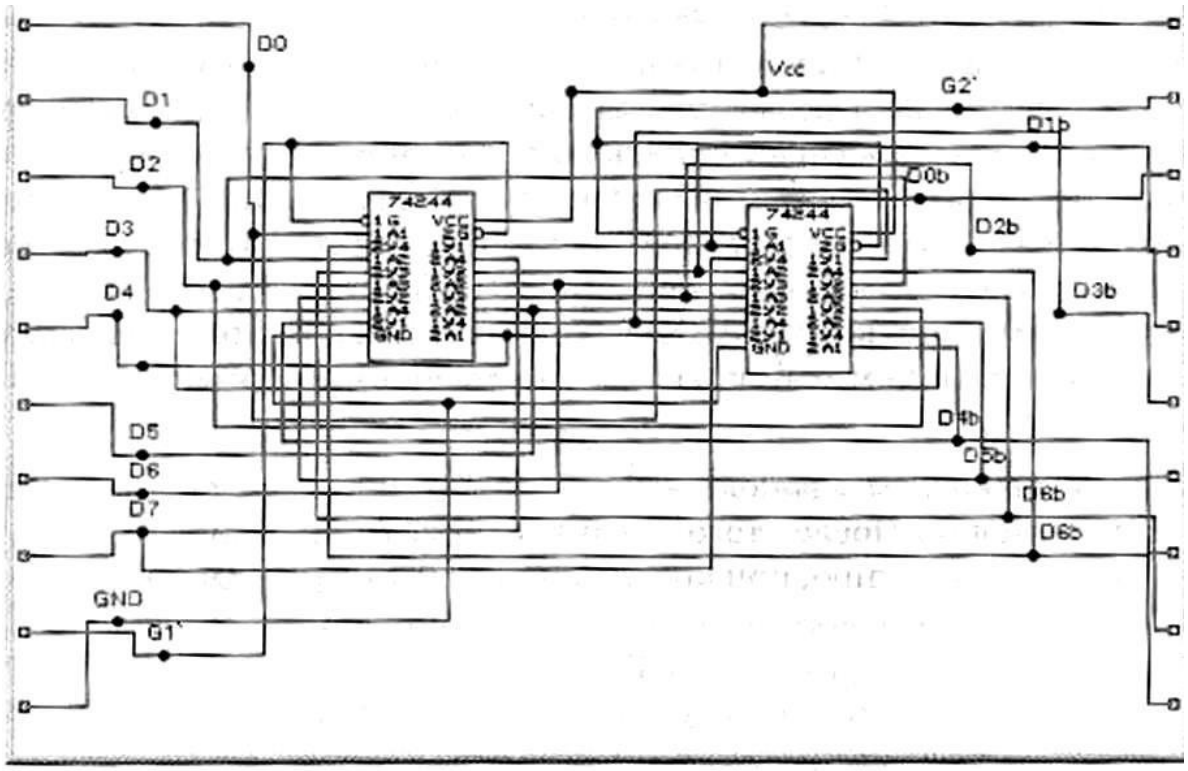
The diagram of the input-output device, which allows for two-way communication with 32 I/O devices, is shown in Fig. 14.



Rice. 14 - Scheme devices input-output For IBM PC

Scheme some changed, because V library programs EWB absent microcircuit tire shaper 74245; she replaced subcircuit from two IMS 74244 (designated as 72245), as a result of which the control circuit (logical elements U1, U2) has also been changed. The second difference is the replacement of two 74244 ICs, used in the original as unidirectional buffers, with single buffer elements U3...U17, which caused by extremely unsuccessful location conclusions IMS 74244. This flaw generally characteristic For everyone digital IMS from libraries EWB. Enough take a look on Torah decoder U23, U24 (domestic analogues of K1ZZIDZ, K1533IDZ And etc.), Where entrances A, IN, C, D, G1 and G2 are located on the right side, while it is common to place them on the left. In other ICs, the inputs and outputs are located alternately on both sides (including the 74244). Third difference consists of V replacement 8-bit comparator 74688, absent V EWB library , for a combination of logical elements U20, U21, U22.

The circuit diagram of the 72245 subcircuit (subblock) is shown in Fig. 15; it can also be implemented using three-state buffer elements.



Rice. 15 - Internal structure subcircuits 72245 The

purpose of the IBM PC system bus signals is as follows:

IOW', IOR' - signals records And readings With active low level For conclusion And input during exchange with UVV;

A0 ... A9 - signals address tires;

D0 ... D7 – data bus signals (in subcircuit 72245), during the write cycle in the UVV microprocessor gives out these signals before signal IOW', A in time cycle readings port input must provide signals to the data bus before the IOR' signal;

AEN - signal permissions choice addresses, is being formed controller direct access to memory (PDP) maternal boards IBM PC, V flow cycle PDP appeal To ports input/output is prohibited, since at this time the IOW', IOR' signals may be activated;

CLOCK (OSC) - systemic clock signal synchronization, is used By necessary , in the diagram in Fig. 15 it is not used;

RESET - signal installations everyone functional nodes systems V original the state after turning on the power or pressing the Reset button on the system unit, synchronized by the OSC pulse.

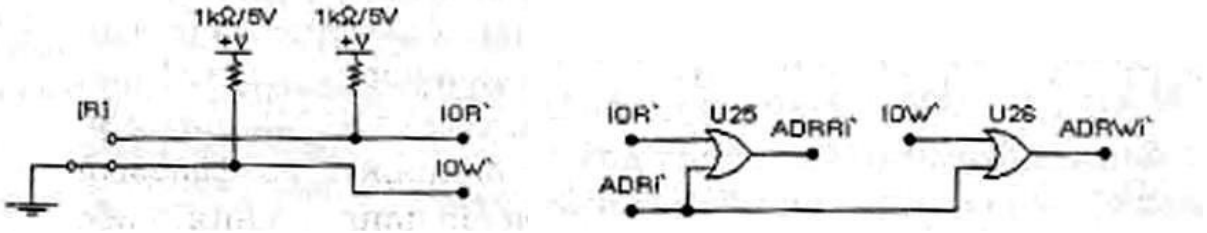
After these signals are transmitted through the buffer elements, the prefix B is added to their name, i.e. BIOW', BD0, BRESET. The IOA' signal – permission to select the address of the I/O port – is formed address selector on IMS U20, U21, U22 at permitting condition AEN signal for which the active signal level is low.

At the outputs 0...15 of decoders U23, U24, address signals of 32 input-output ports (from 300H to 31FH) with an active low level are generated.

To indicate the status of outputs V in the simplest case LED can be used IND (on scheme connected only To one exit). Entrances Gl decoders, G2 resolving, at filing on them signals low level (logical zero) allowed formation signal on exit decoder, determined binary code on address inputs A, B, C, D.

Job With UVV on rice. 14 allows get acquainted With hardware means program input-output and develop skills in diagnosing and localizing faults in digital control systems.

The circuit for simulating the IOR' and IOW' signals is shown in Fig. 16, a). In the position of switch R shown there, a write signal is generated (reading is prohibited, since the IOR' input is a logical one signal, prohibiting this mode). When the key is pressed , R is being formed signal readings from UVV, connected By chosen address, at this entry prohibited By specified higher reasons. EMF source voltage For IMS series 155 is selected equal 5 IN, A his internal resistance - approximately equal output resistance of the base element of the 155 series.



Rice. 16 - Scheme imitations signals read/write (A) And scheme splitting one addresses by two (b)

From Fig. 15 it can be seen that the control inputs G1' of the 72245 bus driver (write permission in the I/O bus) and G2' (read permission from the I/O bus) are connected to the outputs of the two-input logic elements OR U1 And U2 respectively, which are implementing functions two-input AND elements for active inverse signals at the inputs, i.e.:

G1' = IOW' · IOA' (mode recordings), G2' = IOR' · IOA' (reading mode).

If one UVV works only to receive information (for example, an indicator device), A second - only on transmission (For example, survey sensor, That They can be connected To alone address, those. To alone exit decoder U23 or U24, With help schemes on rice. 16, b), V which split addresses is produced for check selection signals read-write. Elements OR U25, U26 they work similarly U1, U2. On rice. 16, b) ADRi' - address signal from decoder U23 or U24, ADRRi' – address signal of only the transmitting I/O device, ADRWi' – of only the receiving I/O device.

Described V this section signals systemic tires IBM PC relate To first models these computers - IBM PC XT. Architecture systemic tires such computer It was called XT BUS and is currently an integral part of more advanced architectural solutions.

Content practical work, performed students during the lesson

Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

– operating system Microsoft Windows,
– text CPU Microsoft Office Word or OpenOffice.org Writer,
– program circuit design modeling Electronics Workbench EWB 5.12.

Plan execution practical works:

Base level:

1) Study cells statistical operational memory.
2) Study cells dynamic operational memory.
2) Study 4-x bit RAM.
3) Study cells ROM memory .
4) Study chains formations signal permissions choice addresses port UVV.

Increased level

5) Study chains formations addresses devices input- output.

6) Study tire shapers devices input- output.

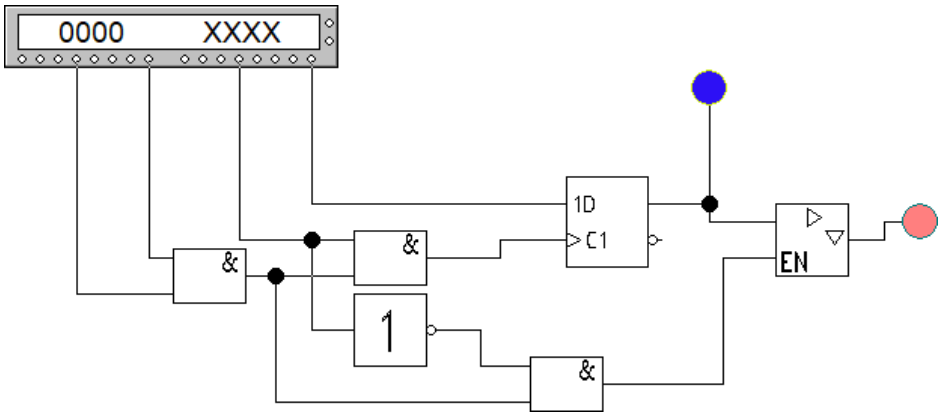
7) Study devices input- output.

Order execution works:

Exercise 1. Research internal structure And logic operation of a static random access memory cell using a word generator.

To do this, follow these steps: operations:

1) Launch the Electronics Workbench program and in its workspace assemble the research scheme shown in Fig. 10.



Rice. 10 - Scheme research cells static operational memory The word

generator in this circuit simulates a common bus.

2) Program the word generator so that the least significant nibble contains a data bit equal to 1, the next nibble contains the write/read control commands WR/RD', and the two most significant nibbles contain the row and column addresses of the memory cell for the data of the logical circuits simulating the address decoder.

3) Run the word generator in step-by-step mode and perform writing operations and reading. Add the address of this memory cell to the report, indicate the microcircuit select signal CS on the schematic, and determine which element is used to read data from the memory cell.

4) Change the decoder logic circuit by setting it to a different address at your discretion.

5) Repeat points 2 And 3.

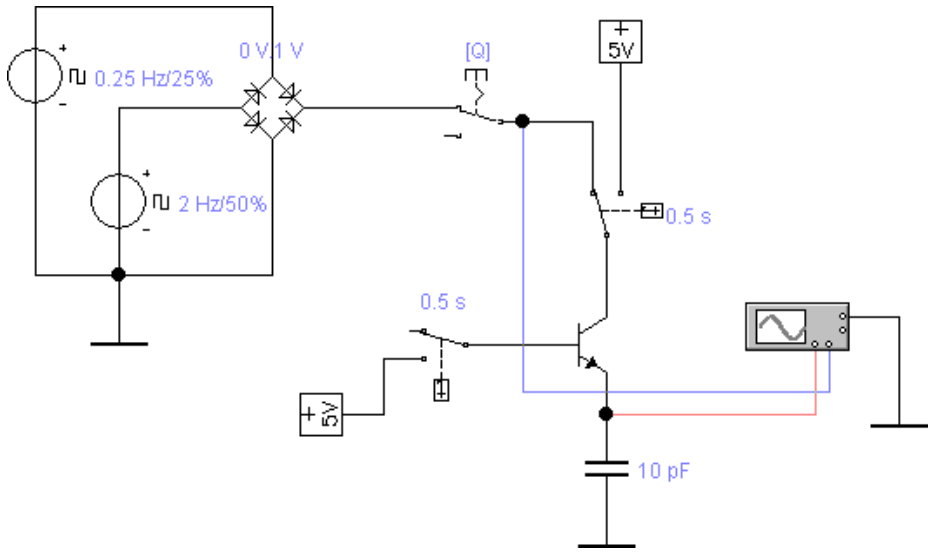
6) Do it conclusions By results work done .

Task 2. Investigate the internal structure and operating logic of a dynamic random access memory cell using an oscilloscope.

To do this, follow these steps: operations:

1) Launch the Electronics Workbench program and in its workspace assemble the research scheme shown in Fig. 11.

This scheme consists of from schemes substitutions cells dynamic operational memory, implemented on a transistor and a capacitor, and a circuit simulating the process of regeneration of recorded data data. Automatic switches intended For modeling the process of writing a logical 1. The circuit breaker located above the transistor simulates the procedure of selecting a memory cell by the address decoder or, more simply, sets the cell address. The circuit breaker located to the left of the transistor simulates the supply of data in the form of a logical 1. The switch controlled by the key Q, intended For connections To cell schemes regeneration data, implemented on two clock pulse generators (CPGs) and an analog switch. The CPG parameters are shown in the diagram (see Fig. 11).



Rice. 11 - Scheme research cells dynamic RAM

2) Install weekend voltage GTI With frequency 0.25 Hz equal 5 IN, A another GTI equal to 15 V.

3) Double click launch oscilloscope And press V him button "Expand". Set the time (horizontal) sweep of the oscilloscope to 1 s/div, the vertical sweep for channel A to 2 V/div, and for channel B to 5 V/div.

4) Disable regeneration scheme, by clicking key Q, And launch scheme in work.

5) After making sure that a logical unit has been written into the memory cell and that the capacitor discharge process has begun, connect the data regeneration circuit.

6) The research scheme and timing diagrams displayed on the oscilloscope should be - included in the laboratory report.

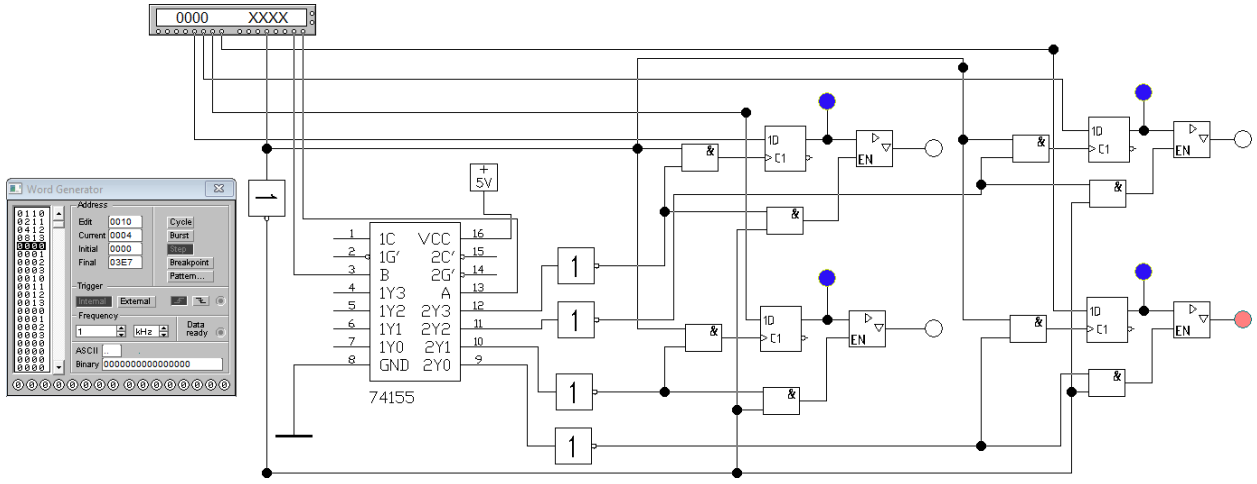
7) Do it conclusions By results work done .

Task 3. Explore the internal structure and operating logic of a 4-bit static RAM using a word generator.

To do this, follow these steps: operations:

1) Launch the Electronics Workbench program and in its workspace assemble the research scheme shown in Fig. 12.

This RAM is built using the 74155 address decoder IC from the EWB library, standard library D-triggers, and logic elements. The static RAM cell is constructed and operates as in Task 3.3.1. The word generator in this circuit simulates a common bus carrying cell addresses, data, and read/write control signals. Logical samples intended For monitoring procedures records And readings .



Figs. 12 – Research scheme The 4-bit static RAM

2) Program generator words, like this in this way, to at the beginning V every A logical 1 was written to each RAM cell sequentially, then each cell was read, and finally, a logical 0 was written to each cell sequentially. The addresses of all four RAM cells must be written in the least significant nibble of the word. teams management writing/reading WR/RD' - V younger discharge next half a byte, and the data to be written into the cells is in the third half-byte of the word.

3) Start the word generator in step-by-step mode and perform sequential write and read operations first of logical one, then of logical zero.

4) Define addresses each cells And designate their on scheme brought in in the report.

5) Define, For what exits decoder connected to inverters.

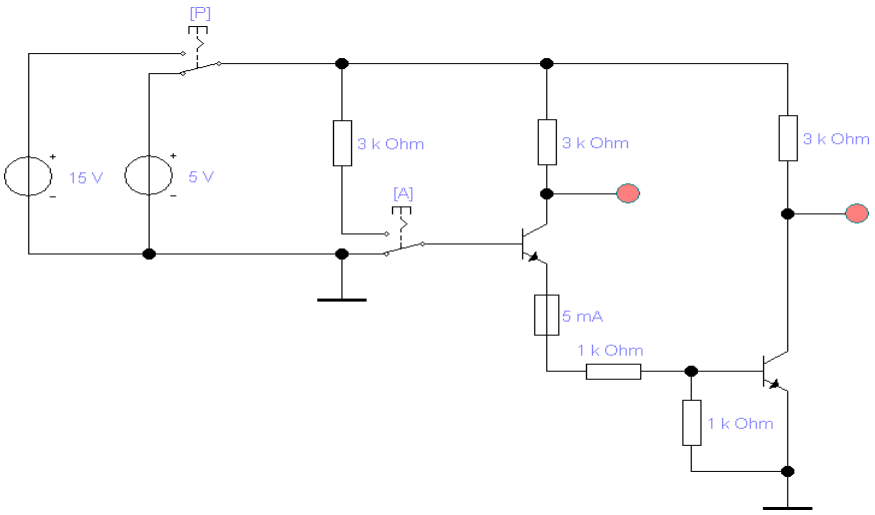
6) Do it conclusions By results work done .

Task 4. Research the internal structure and operating logic of a cell of read-only memory programmed by burning jumpers.

To do this, follow these steps: operations:

1) Launch the Electronics Workbench program and in its workspace assemble the research scheme shown in Fig. 13.

The ROM memory cell is built on a transistor in the emitter circuit, which has a blown jumper (in the simulation circuit - a 5 mA fuse). When selecting this cells memory With decoder addresses on base transistor is served logical unit, V result transistor opens. Electric current small quantities, Passing through the transistor and the jumper with the help of a voltage divider on resistors, it creates a logical 1 signal at the base of the second transistor. The transistor opens, generating a logical 0 signal at the output. To write a logical 1 to the ROM cell, a logical 1 is burned. jumper by way connections programmer V view high-voltage (15 V) voltage source. This leads To increase forces current flowing through the first transistor and burning jumpers. IN result both transistors will always be closed And, therefore, the memory cell will contain a logical unit.



Rice. 13 - Scheme cells memory ROM, programmable by way burning out jumpers

2) Return the circuit to its initial state, as in Fig. 13 – switch P should connect a 5 V battery to the circuit, switch A should be closed to ground (common wire).

3) Turn on diagram V work And make sure V volume, What at short circuit And opening key A, simulating choice this cells memory manager signal decoder addresses, transistors open and close, turning logic probes on and off.

4) Install, Which code Maybe be stored V cell With unburned jumper.

5) Bring the diagram to initial state and switch switch P to other positions , simulating the connection of a programmer to burn a jumper.

6) Connect given cell To programmer, by clicking switch A. Define, What does this procedure lead to? Determine what code can be stored in the cell with the burned-out jumper.

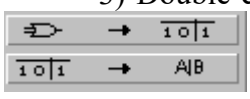
7) Do it conclusions By results work done .

Task 5. Research the internal structure and operating logic of the circuit for generating the address selection enable signal for the I/O port, and identify (localize) the existing error using a logic converter.

To do this, follow these steps: actions:

1) Collect diagram chains, circled on rice. 14 red dotted line. This scheme address selector forms signal IOA' - permission choice addresses port UVV at low active level of the AEN signal state – address selection enable.

2) Place the logical converter icon on the program's working field and attach it to its inputs. A, IN, ..., E, F connect signals A5, A6, ... A9, AEN respectively, A To exit OUT – signal IOA' (output of microcircuit U22).

3) Double-click to expand the logical converter, and press the buttons sequentially. 

Get the truth table and the Boolean expression.

4) After this analyze table truth, having highlighted binary a combination in which IOA' = 0 (column OUT), and in the Boolean expression, the term corresponding to this combination. It is necessary to take into account that A = A5, B = A6, ..., E = A9, F = AEN.

5) Find the error in the circuit and correct it (hint: you need to add a logic element for one of the signals in accordance with its functional purpose given earlier).

6) Please enter V research design necessary element.

7) Check it out With help logical converter right work I'm researching my chains. IN her table truth on exit must be present only one zero V combinations corresponding to the address of a given I/O port with the correct active level of the enable signal.

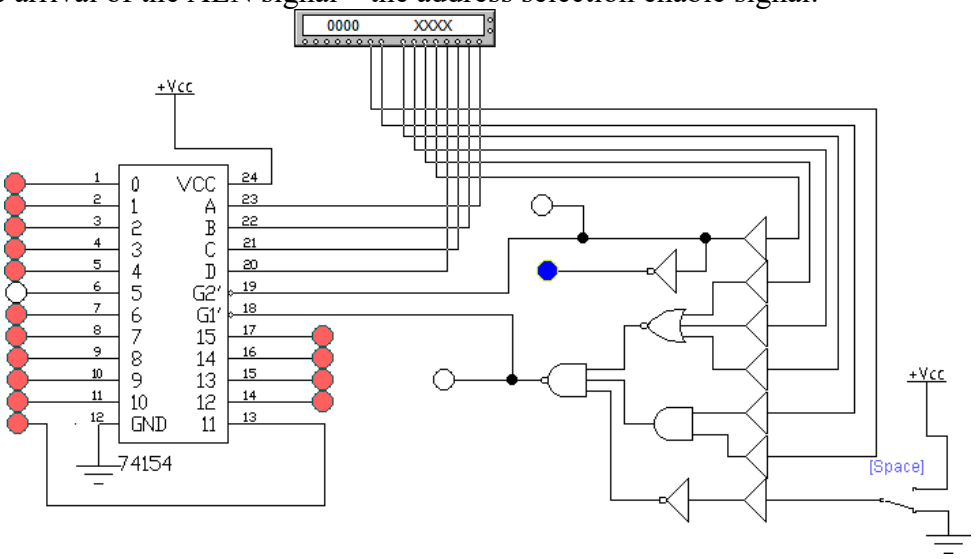
8) Display correct diagram chains V report And be taken aback logic her functioning.

9) Do it conclusions By results work done .

Task 6. Explore the internal structure and logic of the functioning of the formation chain addresses UVV on base IMS 74154 With help generator words And logical probes.

To do this, follow these steps: actions:

1) Collect circuit diagram on base IMS 74154 from the library EWB, given on rice.
17. This circuit simulates the operation of the address generation circuit of the I/O module, which organizes data exchange with 16 external devices. To communicate with all 32 external devices, the actual UVV contains more one IMS decoder addresses. At assembly attentively connect weekend indicator terminals younger (right) half a byte generator words, starting from right younger discharge, respectively With entrances A … D decoder addresses. Signals from younger half a byte generator words correspond signals A0 … A3 address tires on the diagram devices input-output on rice. 14. Next indicator terminals generator words imitate signals A4 … A9 address tires. They connected To chains formations port address selection enable signal. The switch in the diagram simulates the arrival of the AEN signal – the address selection enable signal.



Rice. 17 - Circuit diagram formation of addresses UVV on IMS base 74154

2) Program the generator words. For this first determine the signal states at address inputs A5...A9 in the address range 300 $_{H}$ ...31F $_{H.}$ To do this, it is necessary to convert their hexadecimal code to binary, replacing each hexadecimal digit with a binary tetrad, i.e. 300 $_{H}$ = 0011 0000 0000, 31F $_{H}$ = 0011 0001 1111, from where it is clear, What V specified range addresses A9=A8=1, A7=A6=A5=0 (countdown addresses starts with the least significant, zero digit), while the address A4 is either 0 or 1. From this analysis it is clear that What For this schemes, containing total one decoder addresses, V generator words, only the lower signals A0 … A3 of the address bus should change, so program sixteen various combinations For formations addresses external devices. Besides Togo, program code word For formations addresses external devices using a second (in this case virtual) address decoder, for example 310 $_{H}$.

3) Install word generator V step-by-step mode.

4) Use the switch to simulate an active low level of the AEN signal – the address selection enable signal.

5) By pressing key STEP generator words, V step by step mode look through, And Analyze - the logic of the functioning of the address generation circuit of the UVV by observing the state of the logical probes at the outputs of the address decoder.

6) WITH help switch translate signal AEN V inactive high level, repeat the research procedure.

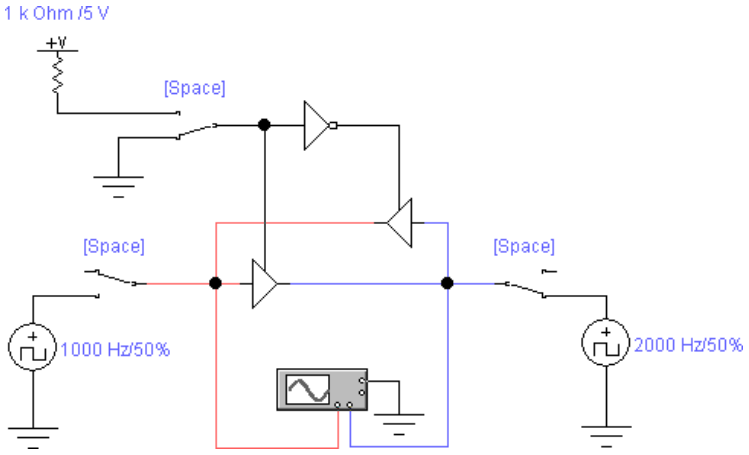
7) In the report, display the circuit under study, describe the logic of its operation, and present the program (sequence of code words) written into the word generator.

8) Do it conclusions By results work done .

Task 7. Research the internal structure and operating logic of a single -bit bus former.

To do this, follow these steps: actions:

1) Collect diagram research, given on rice. 18. Switch imitates recording signals in UVV and readings from UVV. The left one in the diagram is the clock generator. (GTI) with a frequency of 1000 Hz simulates the procedure of data transmission to the UVV, and GTI with a frequency of 2000 Hz simulates the procedure of data transmission from the UVV.



Rice. 18 - Scheme research of a single-bit bus former

2) Double-click to expand the oscilloscope screen and set the Time Base to 1 ms/div.

3) Turn the circuit on and, by changing the switch position, observe the data transfer process.

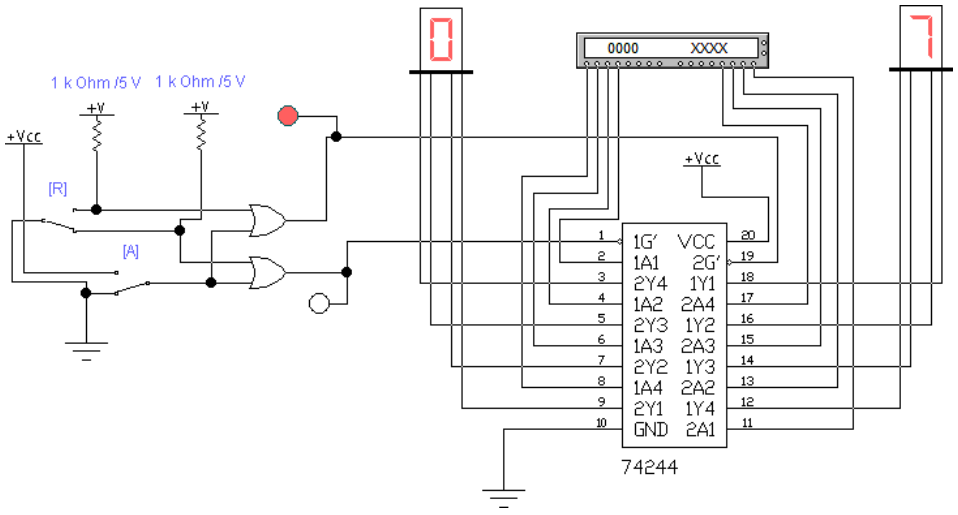
4) Display the research diagram in the report. Describe the operating logic of the bus driver, determining the switch positions that cause data to be written to the I/O bus and read from the I/O bus, as well as the active levels of these signals. Enter these signals into the diagram next to the control input of the corresponding tri- state buffer element.

5) Do it conclusions By results work done .

Exercise 8. Research internal structure And logic functioning four- bit bus former based on the 74244 IC from the EWB library using a word generator and seven-segment indicators.

To do this, follow these steps: actions:

1) Collect diagram research, given on rice. 19.



Rice. 19 - Scheme research four-digit tire shaper on basis IMS 74244

The 74244 IMS is an assembly of eight buffer elements with a tristate output, so it can be used to synthesize a four-bit bus driver . Input/output pairs 1A1 and 1Y1, ..., 1A4 and 1Y4 are intended for writing data to the I/O buffer, provided that an active-low signal is present at the 1G1' input. Input/output pairs 2A1 and 2Y1, ..., 2A4 and 2Y4 are intended for reading data from the I/O buffer, provided that an active-low signal is present at the 2G1' input.

The OR logical elements together with switches A and R simulate the circuits for generating signals for enabling writing to the I/O pin and reading from the I/O pin by pressing the R key when condition, What on entrances elements OR is served short active level signal permission to select the address of the UVV port, the supply of which is simulated by switch A.

2) Program generator words like this in this way, to V his senior The nibble contained data codes written in the UVV, for example from 0000 to 0111, in the least significant nibble - codes data, readable from UVV, For example from 1000 to 1111. At this Write the first eight code combinations sequentially in cells 0000 through 0007, and the second eight combinations in cells 0008 through 000F.

3) Set the word generator to step mode, looping from cell 0000 to 000F.

4) elements using switch A OR And launch generator, words pressing button Step, make sure V volume, What data are not transmitted through the bus former.

5) Switch switch A, allowing the choice of address of this port of the UVV; set the switch R to the recording mode; restart the word generator.

6) By pressing button Step, produce procedure records data from first eight cells of the word generator in the UVV, which simulates the right seven-segment indicator.

5) Translate switch R V mode readings.

7) By pressing the Step button, perform the procedure of reading data from the next eight cells generator words, which imitate memory UVV. IN this case receiver The read data is displayed on the left seven-segment indicator.

8) Display the research scheme in the report. Describe the operating logic of the bus former.

9) Do it conclusions By results work done .

Content report about work

IN In the report, please provide:

– topic And target work work ,

– plan work;
– brief abstract theoretical material;
– designs ;
– results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, voltage diagrams, etc.;
– conclusions O done work.

Control questions For preparation To report protection :

1) Purpose And classification operational memorizing devices.
2) Characteristic internal structures And principles functioning typical random access memory device.
3) Characteristic logic functioning operational memorizing static type devices .
4) Characteristic logic functioning operational memorizing dynamic type devices .
5) Characteristic modern types operational memory.
6) Characteristic video memory.
7) Characteristic modern types IMS operational memory.
8) Purpose And classification permanent memorizing devices.
9) Characteristic And principles functioning cells constant memory, one- time programmable by burning jumpers.
10) Practical application permanent memorizing devices various types.
11) Order research internal structures And logic functioning static random access memory cells using a word generator.
12) Order research internal structures And logic functioning dynamic random access memory cells using an oscilloscope.
13) Order research internal structures And logic functioning 4-x bit static RAM using a word generator.
14) Order research internal structures And logic functioning cells of read-only memory, programmable by burning jumpers.
15) Principles of construction and characteristics of the operating logic of input-output devices.
16) The procedure for studying the internal structure and operating logic of the circuit for generating the enable signal for selecting the address of the I/O port.
17) Order identification (localizations) mistakes V logical schemes With help logical - converter.
18) The procedure for studying the internal structure and logic of the functioning of the address generation circuit of the UVV based on the 74154 IC using a word generator and logic probes.
19) The procedure for studying the internal structure and operating logic of a single- bit bus former.
20) The procedure for studying the internal structure and operating logic of a four- bit bus former based on the 74244 IC from the EWB library using a word generator and seven-segment indicators.
21) Order synthesis of internal structure And studies of logic functioning of a typical input-output device.

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

PRACTICAL WORK No. 19

Subject: **STUDY DIGITAL-ANALOG AND ANALOG -DIGITAL CONVERTERS**

Time - 4 teaching hours.

TARGET SETTING OF PRACTICAL WORK :

During practical work, students must master the following skills and abilities:

– carry out circuit (computer) modeling of sequential digital devices using universal packages applied computer programs;

– conduct study sequential digital devices on basis their circuit models,

– synthesis of sequential digital devices using universal software packages;

– collection and analysis of information to generate initial data for the design of digital devices.

EDUCATIONAL AND MATERIAL SECURITY:

– program editor schematic modeling Electronics Workbench" (EWB), version no lower than 5.12 or NI Multisim Education version;

– Mathcad Professional, an application for mathematical and engineering calculations, version 15.0 or higher;

– electronic methodological development By laboratory work.

STRUCTURE OF PRACTICAL WORK :

Lesson No. 1	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**75 min**
1. Study digital-to-analog converters.	75 min
The final part	**5 min**
Summing up results	3 min
Exercise students For independent work	2 min
Lesson #2	**90 min**
Introductory Part	**10 min**
Checking students' readiness for practical work	8 min
Introductory Part	2 min
Questions (tasks), subject research:	**55 min**
2. Study analog-to-digital converters.	55 min
The final part	**25 min**
Defense of practical work reports	20 min
Summing up results	3 min
Exercise students For independent work	2 min

CONTENT LABORATORY CLASSES

Brief theoretical or reference materials **Digital-analog converters** intended For transformations digital code N into proportional analog voltage levels U(N), that is, the output signal of the DAC in generally accepted units of current or voltage (mV, V, mA) corresponds to the numerical value of the input code combination.

By principle actions schemes DAC there are: With summation And division voltage, with summation of currents.

Direct conversion ADC

Direct conversion ADCs are the simplest and are often built directly into the circuit. V sensors. The main functional element such ADC is converter of electrical quantities (current, voltage, resistance, capacitance) into time interval or frequency. Example such converter Maybe serve a device that converts a direct positive voltage into frequency (Figure 16.1, b). To convert a time interval or frequency into a digital code, which is essentially the final task of any ADC, a computer is used in the case of an automated control system or an additional device V case autonomous ADC. Example such devices, converting the time interval into code is shown in Figure 16.1, a. In this device temporal interval is being asked software key T, imitating, for example, pulse-pitch modulator (PWM) And defining quantity impulses, arriving at a four-digit counter from the reference frequency generator Us. The device under consideration By being is frequency meter. If transformable magnitude directly proportional period, That respectively additional device should provide period to code conversion .

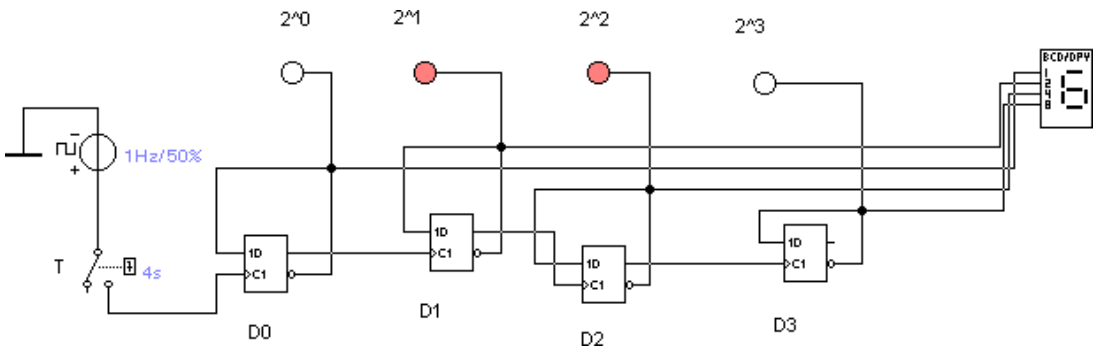
Converter on drawing 16.1, b completed on two OU: amplifier OU1 is used in the integrator, and OU2 is used in the regenerative comparator with hysteresis. When the comparator output voltage Uf has a maximum positive value U_1, the diode VD is biased V reverse direction And voltage Us on exit OU1 (cm. oscillograms on Figure 16.1, V) decreases By linear law with speed, determined amplitude input positive signal Ui, until it reaches the value U_1 R1/R2. At this point, the comparator switches V other state, at which voltage on his exit equal to the maximum negative value of U_2, while the diode VD opens and the output voltage of the integrator quickly increases to the value of U_2 R1/R2, after which the comparator returns to its original state and the cycle repeats.

Since the rise time of the integrator's output voltage is significantly shorter than the fall time, which is inversely proportional to the input signal amplitude, the repetition rate F will be directly proportional to the input voltage. Neglecting the comparator's inherent switching time, the following expression can be written for the output pulse frequency:

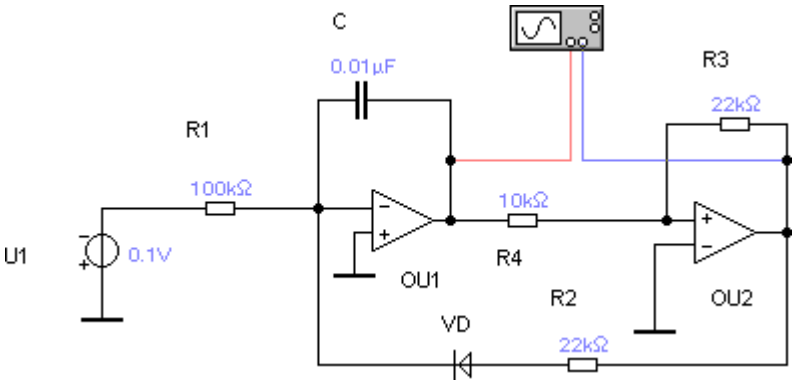
$$F = Ui * R3/[R1 * C * R4(U1 - U2)] \approx 1000 * Ui. \qquad (1)$$

In fact, the voltage swing Us at the output of OU1 is somewhat larger than the value of (R1/R2)($U_1 - U_2$) due to the non-zero value of the comparator switching time, and the frequency is correspondingly less than the value determined by expression (1), and this discrepancy will be especially significant at large amplitudes of the input signal.

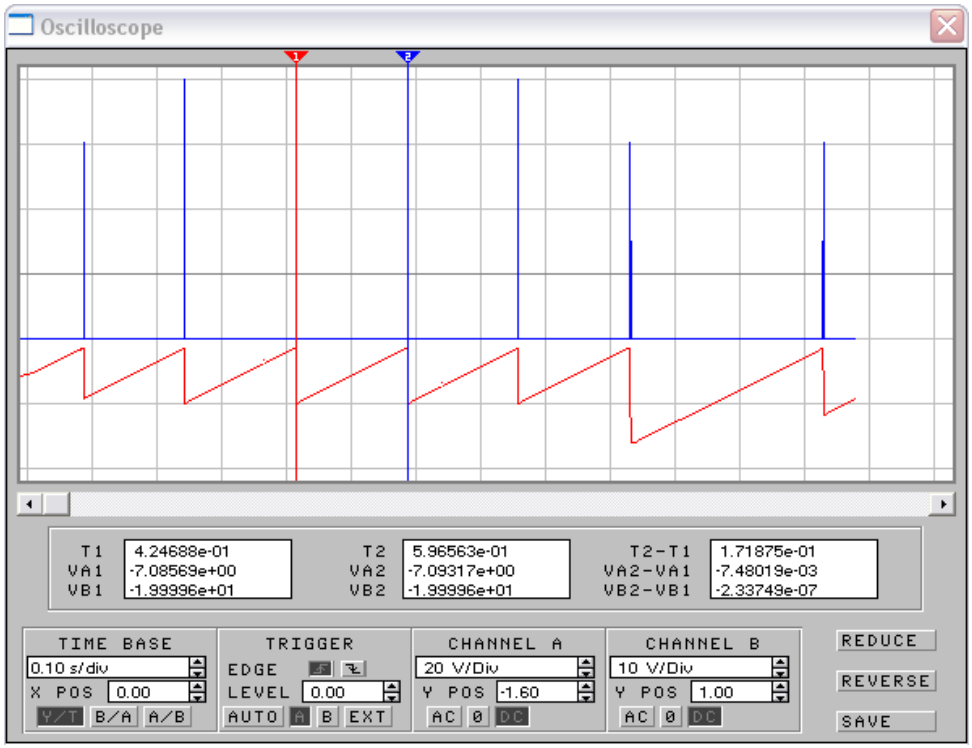
With the element ratings indicated in Figure 16.1,b, the circuit must ensure conversion linearity of no worse than ±1% in the input voltage change range of 20 mV...10 V, while the output pulse frequency F must change from 20 Hz to 10 kHz.



Drawing 16.1, A.

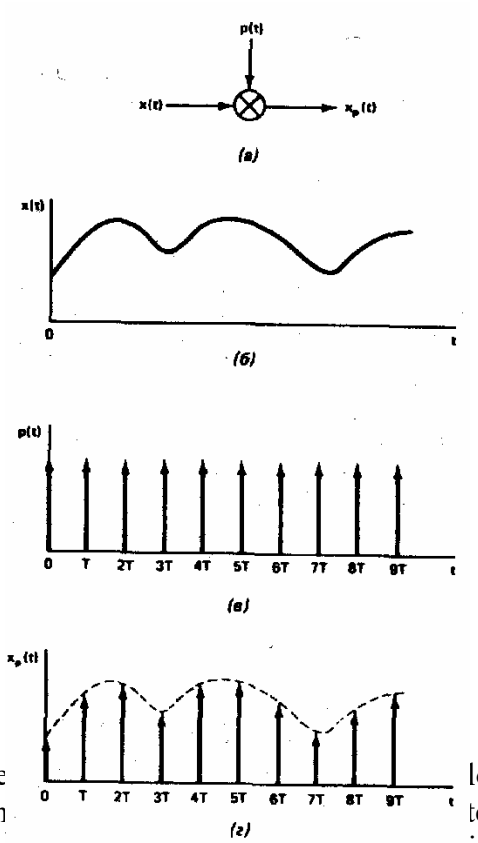


Drawing 16.1, b.



Drawing 16.2 - ADC direct transformations (A) And oscillograms (V) signals on in the course of the integrator (B) and comparator (A) (b)

IN computer should to enter subsequence numbers, equivalent given analog signal. The most ideal would be to process all defined values of the analog variable in a computer. However, due to the finite volume



computer memory we are forced to limit the number of points countdown. Values variable, taken V discrete - moments in time form "samples" (or "counts") of an analog signal. The frequency at which discrete signal values are sampled (frequency discretization), defines accuracy representation of this signal as a discrete-time function .

The sampling theorem states that “under certain conditions, a continuous-in-time signal can be completely represented (reconstructed).

Sampling theorem. For accurate representation and reconstruction of an analog signal, the following conditions must be met:

1) signal must to occupy limited by frequency band;

2) the sampling frequency must exceed the upper border frequency spectrum signal Not less than 2 times.

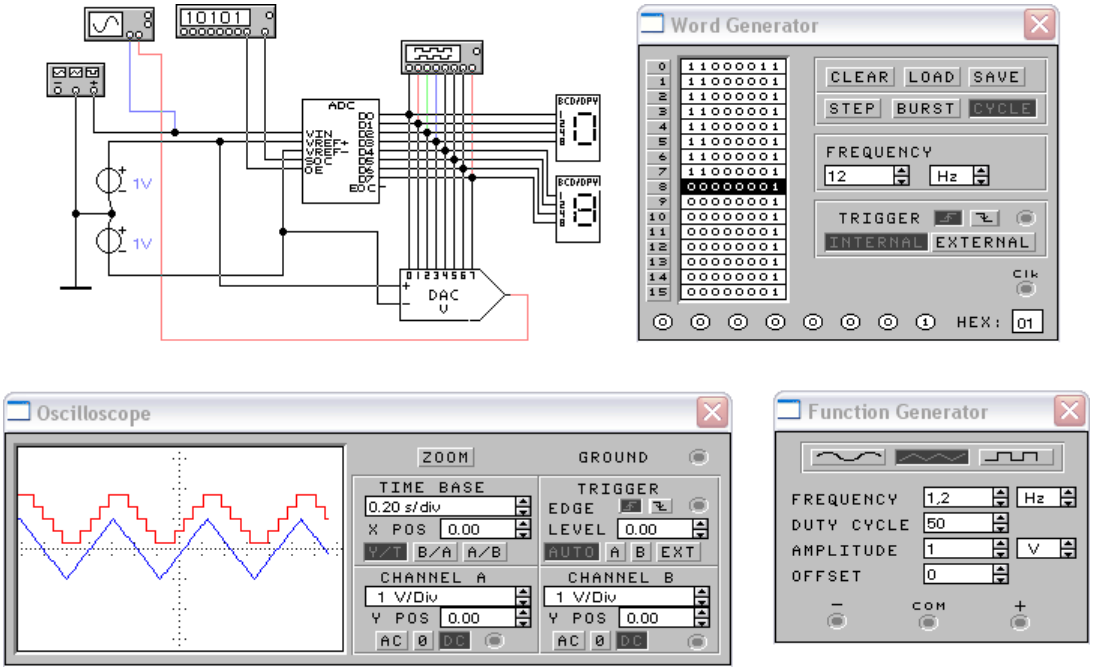
it is sufficient to fulfill these conditions in practice difficult. Signals, coming from sensors, inevitably contain unlimited number harmonics,

and increasing the sampling frequency (caused by the nee log functions) requires increasing the speed and increasing th ter. Consequently, absolutely accurate processing of real signals is impossible , Although emerging errors Can minimize, accepting some additional measures.

On drawing 16.2 is shown scheme ADC that allows record data in file.

The circuit contains the ADC itself, reference voltage sources, a word generator for synchronizing and controlling the ADC output, a function generator as an input signal source U_i, a logic analyzer, a binary converter, and an oscilloscope . The purpose of the ADC pins: VIN – input for the source of the signal to be converted; VREF+, VREF- – input for sources reference voltage; SOC – synchronization input; OE – permission on issuance binary combinations on outputs D0…D7; EOS - signal data readiness (for example, when outputting data from a computer). For a given value of the input voltage U_i, the decimal equivalent of the binary code at the ADC output is determined by the expression: $D = 256\ U_i / [(+U_{op})+(-U_{op})]$.

Received data With ADC Can analyze With help logical analyzer and oscilloscope.



Drawing 16.3 – Wiring diagram library ADC

Content practical work, performed students during the lesson

Description laboratory equipment:

1) Personal computer - Not less 1st on two students;
2) Software :

– operating room Microsoft Windows system
– text CPU Microsoft Office Word or OpenOffice.org Writer,
– program circuit design modeling Electronics Workbench EWB 5.12.

Plan execution practical works:

Base level:

1) Study DAC With weight resistors.
2) Study DAC staircase type.
3) Study four-digit DAC staircase type on base counter 74160.
4) Study 8 discharge DAC.

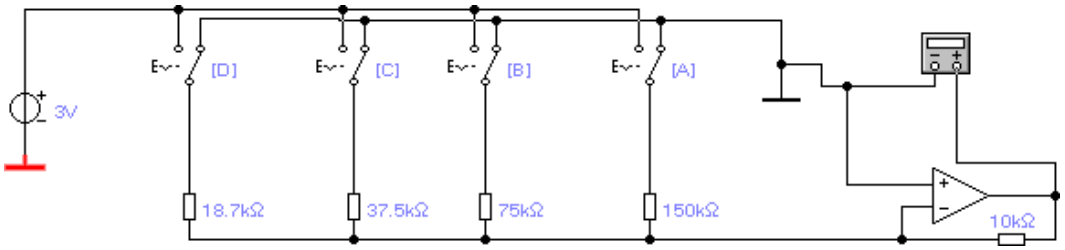
Increased level

5) Study ADC direct transformations.
6) Study dependencies weekend code from sampling frequency .
7) Analysis losses transformations.

Order execution works:

Exercise 1. Study DAC With weight resistors.

Collect diagram according to drawing 15.1.



Drawing 15.1 - DAC With weight resistors

DAC With weight resistors consists of from two nodes: resistive schemes (matrices) on resistors of 18.7 kΩ, 37.5 kΩ, 75 kΩ, 150 kΩ and a summing amplifier with a 10 kΩ feedback resistor. The reference voltage U_{op} (3 V) is connected to the matrix resistors by switches A, B, C, D, controlled by the keys of the same name on the keyboard and simulating the code being converted. The output voltage at the output of the operational amplifier is measured with a multimeter.

A). Determine, By which one law are selected resistance V DAC With weight rubber stores.

Calculate relative And absolute resolving DAC capability .

B). Calculate coefficients gains voltage OU And weekend voltage DAC in scheme For everyone options switches A, B, C, D. Results calculation compare With results obtained on the model.

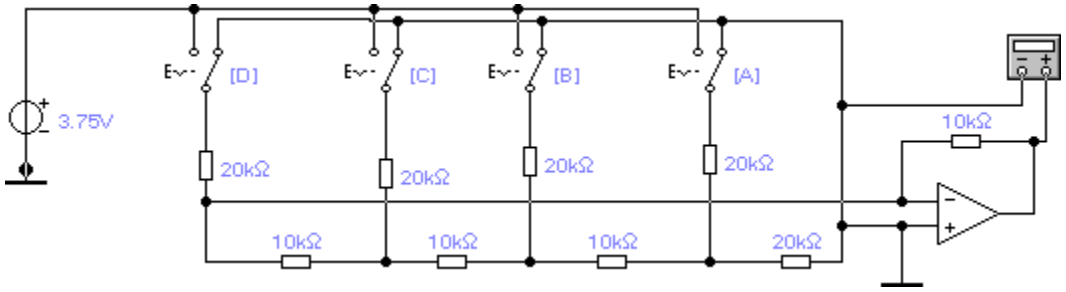
Determine the change in the DAC output voltage upon transition to each successive binary number.

IN). Get it expression For calculation weekend voltage DAC V in general view And check it on the model.

D). Replace switches A, B, C, D with program switches (time relays) simulating the sequential appearance of code signals at intervals of 5 seconds. combinations 0001, 0011, 0111, 1111. Draw it schedule dependencies voltage on DAC output over time.

Exercise 2. Study DAC staircase type.

Collect diagram according to drawing 15.2. Scheme DAC such type consists of from a ladder-like R-2R resistive matrix and a summing amplifier.



Drawing 15.2 – DAC staircase type

A). Conduct a study of this circuit. Calculate the output voltage of the DAC for everyone combinations switches A, IN, WITH, D And compare received results With simulation results . Plot a graph of the DAC output voltage as a function of switch combinations A, B, C, D. To which quadrant do they belong? the readings received?

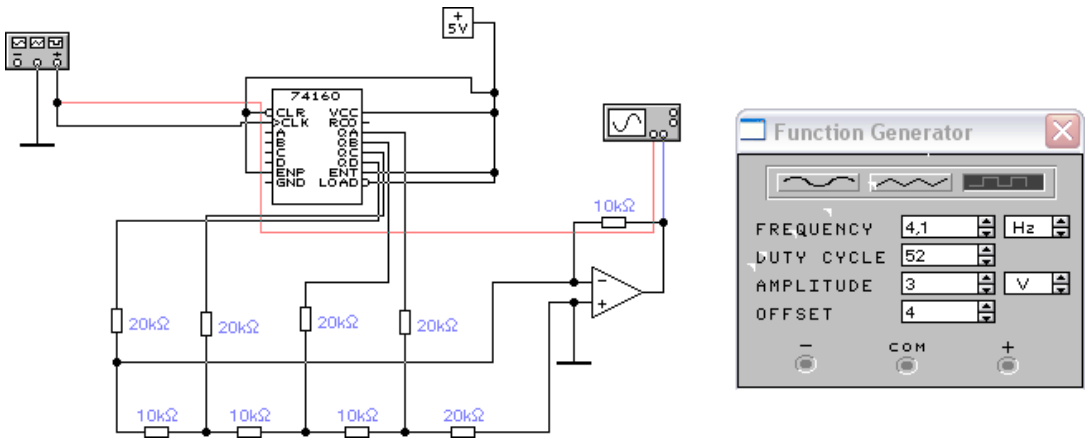
B). Determine the change in the output voltage of the DAC when moving to each successive binary number.

C). Reverse the polarity of the connected source. Plot a graph of the DAC output voltage as a function of switch combinations A, B, C, and D. To which quadrant do the resulting readings belong?

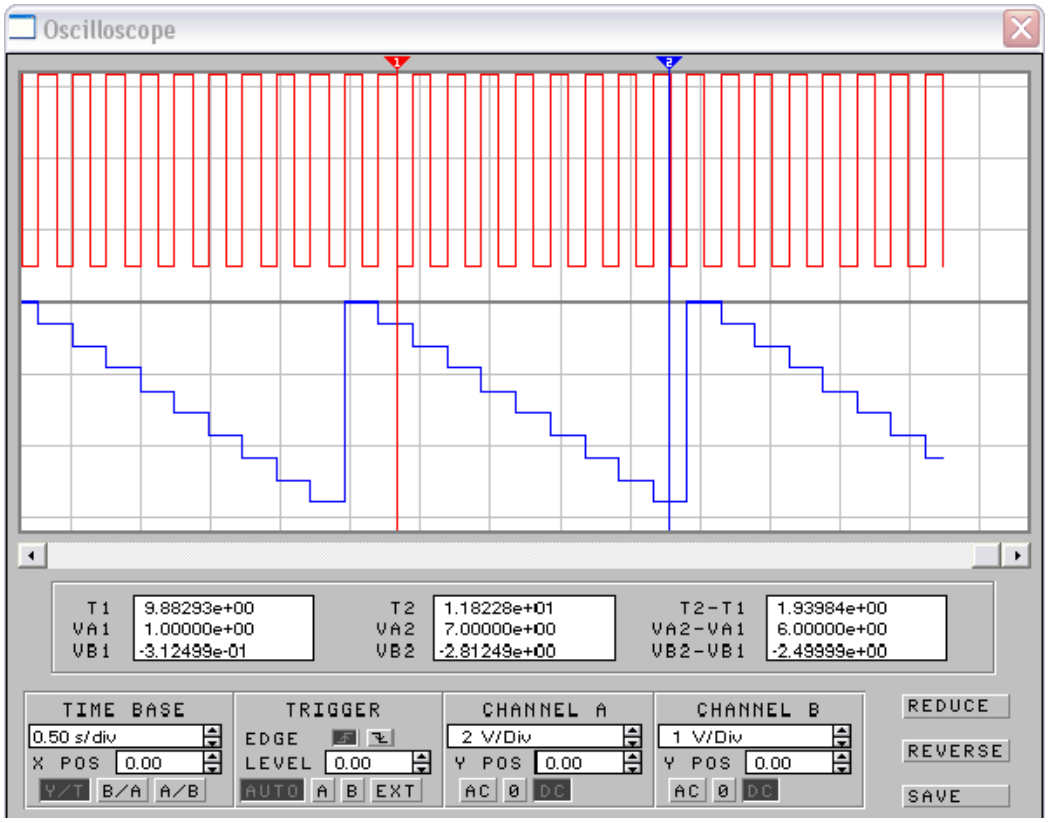
G). Compare DAC With weight resistors And DAC staircase like, do it conclusions.

Exercise 3. Study four-digit DAC staircase type on base Chika's account is 74160.

Collect diagram four-digit DAC staircase type on base counter 74160 according to Figure 15.3.



Drawing 15.3 - DAC on basis binary-coded decimal counter 74160



Drawing 15.4 - Oscillograms signals on counting at the entrance And exit DAC

Obtain oscillograms of the DAC signals at its counting input and output according to Figure 15.4.

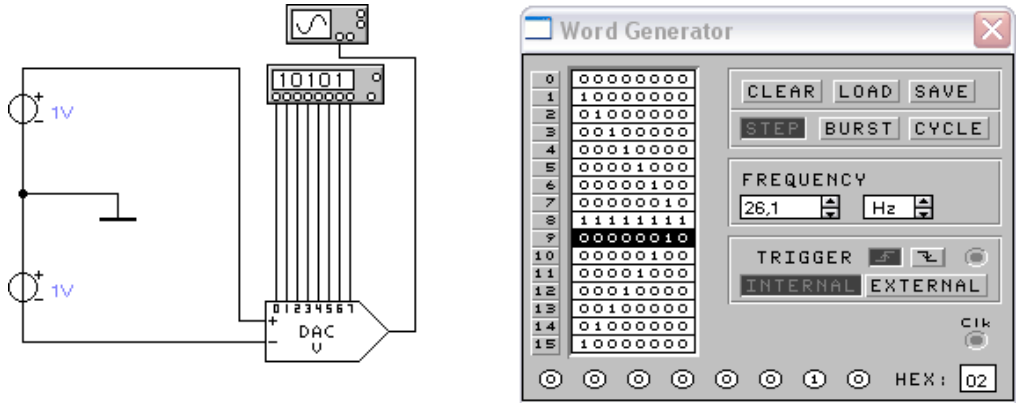
A) By changing the repetition rate of the input pulses 1, 5, 10, 15 Hz get oscillograms at the input and output of the DAC.

B). By changing the parameters of the function generator, investigate the properties of the DAC. Draw appropriate conclusions based on the results obtained.

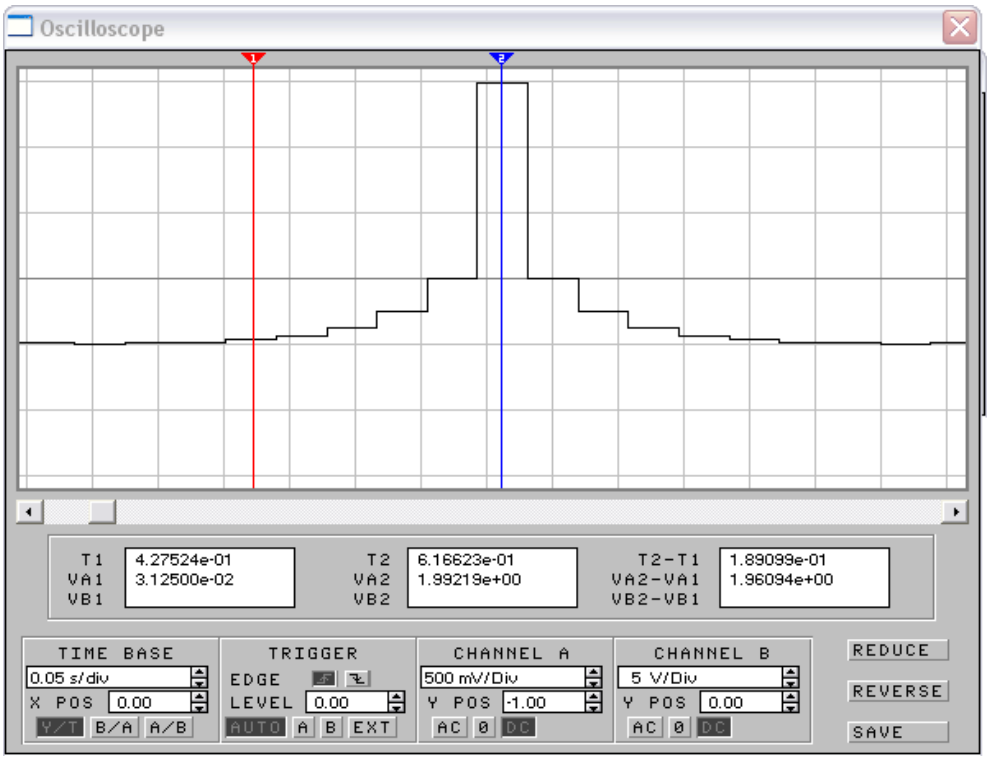
Explore collected diagram And determine main parameters DAC, discussed in the theoretical part of the laboratory work.

Exercise 4. Study 8 discharge DAC.

Collect diagram according to drawing 15.5. Scheme inclusions 8 discharge DAC contains the DAC itself (DAC V), two reference voltage sources +Uop and -Uop, a word generator and an oscilloscope.



Drawing 15.5. – Scheme inclusions 8-bit DAC



Drawing 15.5 - Oscillogram weekend DAC voltage

A). Program the word generator as shown in Figure 5.5 and obtain an oscillogram . weekend voltage DAC (drawing 15.6). Please pay attention attention on That, What The digit numbering is shown on the DAC graphic icon (Figure 15.5). Correspond to the digit number value with the change in the DAC output voltage.

Weekend DAC voltage is determined by the expression:

Uo = D[(+Uop) + (- Uop)]/256,

Where D — decimal equivalent input binary code (For example, at entrance code 00000011 D = 3).

By setting the appropriate code combinations at the output of the word generator, it is possible to use an oscilloscope to measure the maximum output voltage of the DAC, as well as the minimum voltage corresponding to the least significant bit and determining the resolution of the DAC.

B). Explore diagram And receive oscillograms weekend voltage DAC at from change:

various code combinations on exit generator words; values of reference

voltage sources from 1 to 5 volts;

frequencies following code combinations on exit generator words. B). Check

whether the signal at the DAC output depends on the input code.

G). Analyze addiction weekend signal from bit depth DAC. Check what the number of connected DAC inputs affects and which of them are more significant .

5. By to everyone point conducted research draw your conclusions.

6. Make out laboratory work And get ready to defense.

Tasks 5 - 7. (Increased level)

1. Assemble the circuit shown in Figure 16.1 and conduct its investigation, asking various values temporary interval software key T. Results Enter the results of your research into the table. Explain the results obtained and write down your conclusions.

2. Collect diagram, depicted on drawing 16.1,b And conduct her study. Record oscillograms and examine the dependence of the output signal frequency on the input voltage. Investigate the dependence of the output signal frequency on the input voltage in the range of 10 mV...10 V. Explain your results and write down your conclusions.

3. Collect diagram, depicted on drawing 16.2.

A). Explore diagram For different values input signals (sinusoidal, saw-tooth, rectangular). Changing values supporting voltage receive various Decimal equivalents of the binary code at the ADC output. Explain the operating principle of the circuit under study.

B). Explore the qualitative dependence of the output code on the input signal. Check,

depends whether code on exit ADC from input signal. If Yes, That, What Bye-calls code?

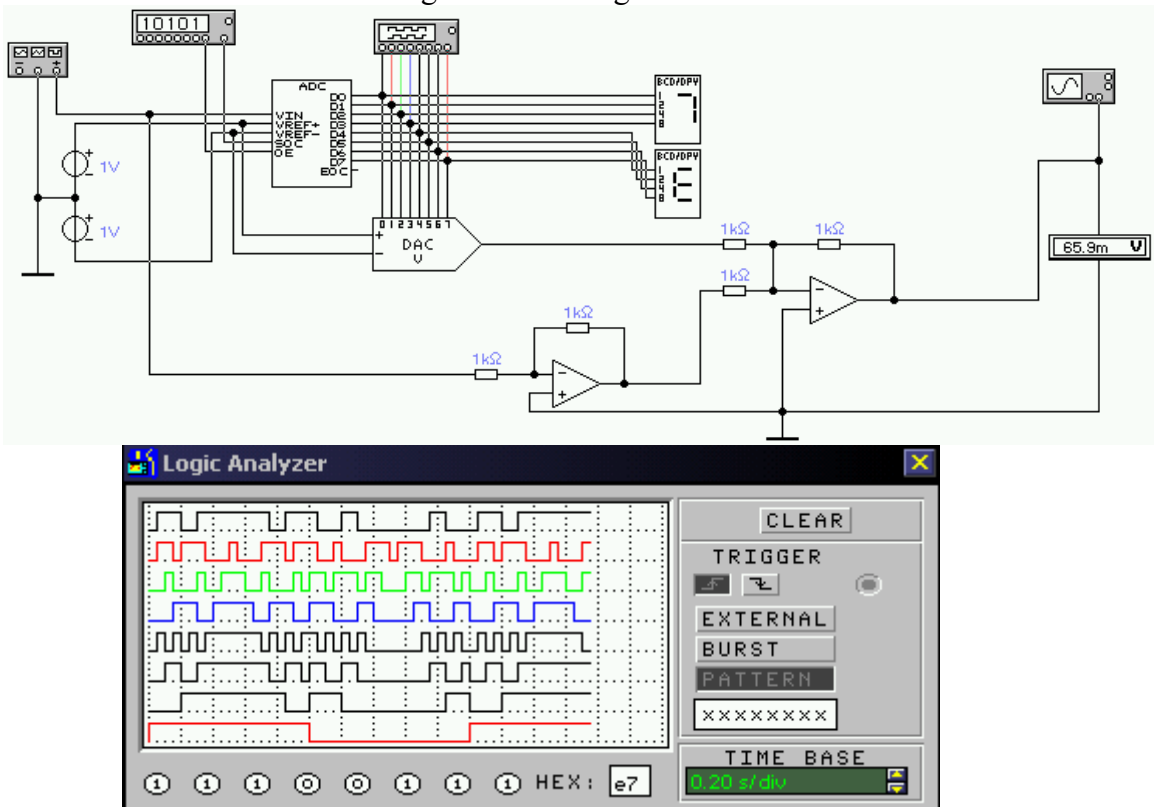
IN). Analyze addiction weekend code from sampling frequency

Changing frequency on generator rectangular impulses, follow up addiction the rate of change of the code at the ADC output from the frequency.

G). Analyze addiction weekend code from ADC bit depth .

Check it out, on What influences quantity connected outputs ADC, And which their them are - more significant.

4. Assemble the circuit according to the drawing 3.



Drawing 16.3 – Scheme ADC

A). Investigate the dependence of the conversion error on the sampling frequency of the input signal

B). Conduct analysis losses transformations. Explain the results obtained results.

Content report about work

IN In the report, please provide:

– topic And target work work ,

– plan work;

– brief abstract theoretical material;

– designs ;

– results execution practical tasks And experiments By to everyone point, including the obtained truth tables, synthesized devices, algebraic transformations, voltage diagrams, etc.;

– conclusions O done work.

Control questions For preparation To report protection :

1) For what intended DAC?
2) Where are applied DAC?
3) What kind main characteristics possess DAC?
4) Which restrictions are superimposed on processed DAC signal?
5) How depends accuracy transformations from frequencies discretization?
6) How depends accuracy transformations from bit depth transformations?
7) How depends time transformations from structures DAC?
8) By which one law are selected resistance V DAC With weight resistors?
9) How differ DAC staircase type from DAC With weight resistors? TO What type of DAC does it belong to?

10) IN how difference 8 discharge DAC from DAC staircase type And With weight resistor-ramie
? 11) For what intended ADC?
12) Where are applied ADC?
13) What kind main characteristics possess ADC?
14) Which restrictions are superimposed on processed ADC signal?
15) Describe appointment conclusions ADC.
16) Describe appointment elements schemes.
17) How depends accuracy transformations from frequencies discretization?
18) How depends accuracy transformations from bit depth transformations?
19) How depends time transformations from structures ADC?
20) What from myself represents ADC direct transformations, V what kind devices his it is appropriate use?
21) Which additional devices necessary connect To scheme on drawing 1b to get a digital reading of the measured voltage?

The practical work was developed by an associate professor of the Department of Digital Robotic Systems and Electronics of the Institute of Advanced Engineering, Candidate of Technical Sciences, Associate Professor, Professor of the Russian Academy of Natural Sciences

V.I. Nikulin

MINISTRY SCIENCES AND HIGHER EDUCATION RUSSIAN FEDERATION FEDERAL STATE AUTONOMOUS EDUCATIONAL INSTITUTION OF HIGHER EDUCATION "NORTH CAUCASIAN FEDERAL UNIVERSITY"

METHODOLOGICAL INSTRUCTIONS

By organizations And conducting independent work

By discipline

Analog Electronic Technology

for students in the field of study

11.03.02 Infocommunication technologies And systems connections Direction (profile)

"Intellectual processing data V "communication systems and networks"

Stavropol 2026

TABLE OF CONTENTS

INTRODUCTION 3
1. GENERAL CHARACTERISTIC INDEPENDENT WORKS 10
2. METHODOLOGICAL RECOMMENDATIONS FOR THE STUDY OF THEORETICAL MATERIAL 15
3. METHODOLOGICAL INSTRUCTIONS BY IMPLEMENTATION LABORATORY WORKS 16
4. SELF-STUDY INTERVIEW QUESTIONS LITERATURE 17
5. COMPUTER TESTS FOR SELF-TESTING, PREPARATION FOR TESTING 22
6. A SET OF MULTI-LEVEL TASKS FOR COMPUTER MODELING WITH USE GRAPHIC EDITORS 27
8. QUESTIONS 35

INTRODUCTION

1. Target And tasks development discipline (module)

The purpose of mastering the discipline : to develop students' professional competencies in the field of modern circuit design of analog and digital telecommunication devices.

Tasks mastering the discipline :

1) Systematization fundamental knowledge V principles constructions And functioning of typical (basic) devices of analog and digital circuitry.

2) Formation skills Right use received knowledge For the correct choice of circuit design solutions when developing telecommunication devices and systems .

3) Acquisition skills V design analog And digital circuit devices;

4) Formation basic circuit design preparations, necessary For successful mastery of professional disciplines, as well as for subsequent project activities.

2. Place disciplines (module) V structure educational programs

The discipline "Analog electronic technology" refers to the disciplines of part, Block 1 of the Discipline (modules).

3. Scroll planned results training By discipline (module), correlated with the planned results of mastering the educational program

1. GENERAL CHARACTERISTIC INDEPENDENT WORKS

All types of independent work on the subject given V table "Technological map independent work." The basis of students' independent work in the discipline is taking notes from lectures and recommended sources, preparing for computer testing of knowledge, preparing and defending reports on laboratory work, and completing multi-level assignments. individual tasks V in the course laboratory works. By each type of independent work provided certain forms reporting, which students present to the teacher V in the course laboratory classes or V watch individual consultations.

Table 1 - Technological map independent work

Code evaluation vayem com-petitions, indicator (ov)	Stage form-rovaniye kom-petitions (No. topics) *(V so-responsibility with work program disciplines)*	Funds And technologies assessments	View control, at-testing *(current-intermediate/interme diate (ny)*	Type control *(oral, writing or using calling technical funds)*	Named-assessment medium-state
PC- 2 ID-1 $_{PC-2}$	Topics No. 1–12	Interview, grade answers By questions for-data those	current	oral	questions For sobe-sedan
	Topics No. 1–12	Testing using computer testing tasks	current	With using technical means	computer test tasks
	Topics No. 1–4, 6, 8–11	Passable task-nie (control-naya dot), You-completion indie-vidual (group) for-Danium from Lab-ratornykh works	current	writing	set once-no-level tasks
	Topics No. 13–20	Interview, evaluation of answers questions given topics	current	oral	interview questions

	Topics No. 13–20	Testing using computer testing tasks	current	With using technical means	computer test tasks
	Topics No. 13–20	Test task (checkpoint), execution individual (group) for-data from laboratory works	current	writing	A set of multi-level tasks
	Topics No. 1–20	Protection course project	intermediate	Writing / oral	Evaluation tools for a course project

To successfully master the discipline, it is necessary to complete the types of independent work indicated in Table 1, using the recommended sources of information.

Scroll basic literature:

1 Galochkin V.A. Circuitry of Analog and Digital Devices Electronic resource: study guide / V.A. Galochkin; ed. S.N. Eliseev. - Samara: Volga Region State University of Telecommunications and Informatics, 2016. - 441 p. - The book is in the basic version of the IPRbooks electronic library system. - ISBN 978-5-904029-51-7.

2 Galochkin V.A. Circuitry telecommunications devices. Part 2. Circuit design of digital electronic devices Electronic resource: Textbook / V.A. Galochkin; ed. WITH. N. Eliseev. - Samara: Volga region state university Telecommunications and Informatics, 2016. - 280 p. - The book is in the premium version of the IPR BOOKS electronic library system. - ISBN 2227-8397.

3 Novikov Yu.V. Introduction V digital circuit design Electronic resource: educational manual / Yu.V. Novikov. - Introduction V digital circuit design, 2019-12-01. - Moscow: Internet University Information Technologies (INTUIT), 2016. - 392 c. - Book located V basic version of the electronic library system IPRbooks. - ISBN 5-94774-600-X.

4 Bastrakova M.I. Circuitry telecommunications devices: workshop / M.I. Bastrakova, V.V. Pavlov; Volga region state technological university. - Yosh-kar-Ola: Perm State Technical University, 2019. - 52 p.: diagrams, ill. - http://biblioclub.ru/. - Bibliography in the book - ISBN 978-5- 8158-2073-9

5 Galochkin V.A. Circuitry telecommunications devices. Methodological developments By laboratory works. Part 1. Circuitry analog electronic devices

Electronic resource: Educational allowance / V.A. Galochkin. - Samara: Volga region State University of Telecommunications and Informatics, 2016. - 402 p. - The book is in the premium version of the IPR BOOKS electronic library system. - ISBN 2227-8397

6 Durkin V.V. Circuitry analog electronic devices Electronic resource / Durkin V.V., Tyrykin S.V., Belorutsky R.Yu.: educational and methodological allowance. - Novosibirsk: NSTU, 2019. - 88 p. - ISBN 978-5-7782-3937-1

Scroll additional literature:

1 Belous I.A. Circuitry telecommunications devices Electronic resource / Belous I.A.: educational allowance. - Vladivostok: VSUES, 2018. - 56 With. - ISBN 978-5-9736-0516-2. 2 Kravets A.V. Educational allowance By exchange rate "Circuitry analog electronic devices»: educational allowance / A.V. Kravets. - Rostov-on-Don|Taganrog: Publishing house South Federal University, 2018. - 185 pp.: ill. - http://biblioclub.ru/. - Bibliography in the book – ISBN. 3 Tench G.I. Circuitry telecommunications devices: textbook allowance: / G.I. Linets, A.V. Veligosha; North Caucasus federal University, Part 1, Analog circuitry. - Stavropol: NCFU, 2015. - 198 p.

4 Loskutov E.D. Circuit design of analog electronic devices Electronic resource: Educational allowance / E.D. Patchwork. - Saratov: University education, 2016. - 264 With. - The book is available in the premium version of the IPR BOOKS electronic library system. ISBN 2227-8397.

5 Mikushin A.V. Digital circuitry Electronic resource: monograph / V.I. Sedinin / A.V. Mikushin. - Novosibirsk: Siberian state university Telecommunications and Informatics, 2016. - 319 p. - The book is in the basic version of the IPRbooks electronic library system. - ISBN 978-5-91434-036-7.

6 Educational and methodological allowance By discipline Circuitry Telecommunication devices Electronic resource / compiled by: V.V. Logvinov, O.V. Matveeva. - Moscow: Moscow Technical University of Communications and Informatics, 2016. - 46 p. - The book is in the premium version of the IPR BOOKS electronic library system. - ISBN 2227-8397.

7 Chervyakov N.I. Digital circuit engineering: Tutorial / N.I. Chervyakov, A.I. Galushkin; North-Caucasian fed. - Stavropol: SKFU, 2015. - 198 p.

A system for assessing knowledge, skills, and abilities that characterize stages formations competencies

Intermediate certification in the form of an exam provides for a mandatory examination procedure.

2. METHODOLOGICAL RECOMMENDATIONS BY STUDY OF THEORETICAL MATERIAL

At independent studying those lectures classes And given Students are recommended to read the following literature:

— on the day of the class, work through the educational material covered in the class notes. At this necessary highlight questions, on which follows turn More attention during further study of the current topic. After working through the educational material, you must answer the recommended control questions;

— With purpose high-quality fastening studied material V subsequently The course material should be studied in more detail using the recommended literature. Students are advised to highlight questions that require more detailed study with the help of the teacher;

— On the eve of the lecture, the student is advised to review previously studied theoretical material and prepare questions that require clarification from the teacher.

Recommendations By organizations work With literature

To master, consolidate and systematize knowledge, students are recommended to study independently. Job With recommended literature And notes lectures. At When working independently with recommended literature, students are advised to take notes on the educational material presented in the recommended sources.

Note-taking of sources is carried out during a detailed study of the topic, and students are advised to:

— Supplement the lecture notes by expanding them on the most important issues discussed in the lesson. Taking notes on sources involves supplementing the notes with the following provisions:

— main definitions And their physical meaning;

— main mathematical relationships with revealing them physical meaning;

— conclusions By educational questions, studied topics classes.

Control this species independent work is being carried out on educational classes by checking the lecture notes and interviewing the teacher.

At note-taking sources students should proceed from rational volume of the material being summarized. The summary should be brief and understandable when used after studying the current topic.

When taking notes from sources, it is recommended to highlight individual drawings, their most important fragments, and the most important formulas in color. When taking notes in class, it is recommended to fill two-thirds of the notebook page vertically, and use the remaining space to supplement the notes on the topic being studied.

To successfully master the course, you must independently and thoroughly study the presented topics using the recommended sources of information.

Source summaries are graded as satisfactory or unsatisfactory. Source summaries are graded as satisfactory if:

— the notes contain a sufficient amount of detail on the topic being studied, ensuring the specified level of mastery of the theoretical material of the discipline;

— abstract decorated carefully, studied material outlined sequentially V in accordance With in order study of the discipline, contains generalizing conclusions By each topic.

The work on summarizing sources is assessed as unsatisfactory if the requirements for a satisfactory assessment are not met.

3. METHODOLOGICAL INSTRUCTIONS BY PERFORMANCE OF PRACTICAL WORK

When completing practical training in a discipline (laboratory work), in order to achieve a basic level of competence development, the student must be able to apply basic knowledge By sections disciplines, own skills independent solutions educational basic level tasks.

When completing practical training in a discipline (laboratory work), in order to achieve an advanced level of competence development, the student must be able to apply advanced knowledge in the sections of the discipline and possess the skills to independently solve advanced level educational problems.

Guidelines for preparation for practical work

Preparation To laboratory work recommended conduct V next sequences :

— to understand topic And target, upcoming laboratory work;

— study theoretical material V in accordance With theme laboratory work (it is recommended to use the recommended literature, lecture notes, textbook (laboratory work workshop);

— familiarize yourself with the equipment and materials used in laboratory work (if using specialized equipment or software, it is necessary to study the procedure and rules for its use).

Guidelines for performing practical work

When performing laboratory work, students must strictly adhere to established safety requirements.

At execution laboratory work students recommended:

— to understand target, performed tasks And methods their decisions;

— tasks, specified V laboratory work fulfill V that one sequences, in which they are indicated in the laboratory practical;

— when completing practical assignments and studying theoretical material, use the help of a teacher;

— design report By laboratory work;

— answer on control questions.

Guidelines for preparing for the defense of practical work

At preparation To protection laboratory work Students are advised to:

— prepare report By laboratory work;

— prepare justification, made conclusions;

— to consolidate knowledge of theoretical material on the topic of laboratory work (it is recommended to use test questions);

— know order conducting calculations (of the research being conducted);

— be able to show and explain the procedure for conducting research using specialized equipment or software.

The defense of the laboratory work is carried out through an interview between the student and the teacher. During the interview, the student submits a report on the laboratory work for review. Interview with student, claiming on assessment "Great" is being carried out By questions and practical assignments of the advanced level of study. An interview with a student who is not aiming for an "excellent" grade is conducted on questions and practical assignments of the basic level of study.

4. QUESTIONS FOR INTERVIEWS BY INDEPENDENT STUDY OF LITERATURE

3rd semester

Base level:

Topic 1. Basic technical indicators and characteristics of analog electronic devices. Principles of electrical signal amplification.

1) Main definitions. Classification amplifying devices.
2) Main technical indicators amplifier.
3) Main technical indicators amplifier.

Topic 2. Principles constructions amplifying devices.

4) Typical functional stages of a semiconductor amplifier: circuits for switching on, applying bias, and stabilizing the position of the operating point.

Topic 3. Reverse connection V amplifiers.

5) General intelligence about reverse connections V amplifiers.
6) Amplifiers With consistent negative reverse communication By current And By tension .

Topic 4. Typical amplification cascades .

7) Amplifying cascade With common emitter (With common source).
8) Amplifiers cascades With general base And With common collector. Topic 5. Amplifying stages with correction.
9) Methods increases coefficient gain.
10) Low frequency correction.
11) Simple parallel high-frequency Correction. Topic 6. Power amplifiers.
12) General principles gains power.
13) Transformerless cascades.
14) Transformer Cascades. Topic 7. Multi-cascade amplifiers.
15) General Provisions about multi-stage amplifiers.
16) RC-coupled amplifiers. Topic 8. Operating amplifiers.
17) General intelligence, parameters, characteristics and equivalent scheme operational amplifier.
18) Schemes turning on operational amplifiers.

Topic 9. Functional schemes on based on operational amplifiers.

19) Adder stresses. Differentiator and integrator.
20) Schemes multiplication capacity And resistance transformations .
21) Amplifier variable current. Comparator.

Topic 10. Active RC filters on operational amplifiers.

22) General information about active filters.
23) Analysis of passive RC filters.
24) Generalized description filter.

Topic 11. Signal generators.

25) Terms and conditions self-excitation modes .
26) Generators With resonant chains.

Topic 12. Analog electronic devices on integral microcircuits.

27) General intelligence about integral microcircuits. Peculiarities analog integrated circuit technology.

Increased level:

Topic 1. Basic technical indicators and characteristics of analog electronic devices. Principles of electrical signal amplification.

28) Main characteristics amplifier.

29) Principles gains electric signal.

Topic 2. Principles constructions amplifying devices.

30) Aperiodic amplifying cascades V mode small signal. Topic 3.

Feedback in amplifiers.

31) Amplifiers with parallel negative current and voltage feedback. Combined negative feedback.

32) Multi-cascade amplifiers with negative reverse connection. Parasitic feedback in multi-stage amplifiers.

Topic 4. Typical amplification cascades .

33) Gain pulse signals.

34) Transformer amplifying Cascades. Topic 5.

Amplifying cascades with correction.

35) High frequency correction for check consistent negative current feedback (Z-type).

Topic 6. Amplifiers power.

36) Methods improvements indicators weekend amplifiers.

Topic 7. Multi-stage amplifiers.

37) DC Amplifiers. Topic 8.

Operating amplifiers.

38) Static errors operating amplifiers.

Topic 9. Functional schemes on based on operational amplifiers.

39) Logarithmic amplifier And exponential generator.

40) Analog multipliers And dividers on operating amplifiers. Topic 10.

Active RC filters using operational amplifiers.

41) General information about active filters.

42) Implementation active filters.

43) Devices formations Frequency response: gyrators, regulators timbre And

Equalizers. Topic 11. Signal generators.

44) RC generators.

45) Examples implementation generators signals on operating amplifiers. Topic 12.

Analog electronic devices on integrated circuits.

46) Amplifiers on integrated circuits.

6th semester

Base level:

Topic 13. Introduction to digital circuit design: Basic concepts of digital circuit design. Laws of logic and minimization of logical functions.

1) Levels performances digital devices.
2) Technologies digital microcircuits, characteristic their entrances and outputs.
3) Basic conventional graphic symbols on diagrams. Series and housings of digital microcircuits.

Topic 14. Logical elements And their application. Elements transistor logic.

4) Logical elements: inverters; repeaters And buffers.
5) Basic logical elements: elements AND, AND-NOT, OR, OR- NOT.
6) Logical element Exclusive OR.
7) Combined logical elements. Topic 15.

Combination circuits:

8) Decoders.
9) Encryptors.
10) comparators .
11) Adders.

Topic 16. Triggers and schemes for their application.

12) Basics constructions And classification of triggers.

13) Operating principles of typical triggers.

Topic 17. Registers And schemes their applications.

14) General information about registers.
15) Parallel registers, triggered along the front.
16) Parallel registers, triggered By level. Topic 18. Counters and their application circuits.
17) General intelligence O counters.
18) Asynchronous counters.
19) Synchronous counters With asynchronous transfer.

Topic 19. Memory: permanent and operational.

20) General information about memory.
21) General intelligence O permanent memorizing devices (ROM).
22) General intelligence about operational memorizing devices (RAM).
23) RAM For temporary storage of information.

Topic 20. Digital-analog And analog-to-digital converters.

24) General information, classification and parameters of analog-to-digital converters (ADC).
25) Parallel And serial-parallel ADCs.
26) General information, classification and parameters of digital-to-analog converters (DAC).

Increased level:

Topic 13. Introduction to digital circuit design: Basic concepts of digital circuit design. Laws of logic and minimization of logical functions.

27) Laws digital logic.
28) Minimization logical functions

Topic 14. Logical elements And their application. Elements transistor logic.

29) triggers .
30) Elements transistor logic. Topic 15.

Combination circuits:

31) Multiplexers.
32) Converters codes.
33) Monostable multivibrators And generators.

Topic 16. Triggers and schemes for their application.

34) Main schemes enabling triggers.
35) Encoder Manchester code on triggers. Topic 17.

Registers and their application schemes.

36) Application parallel registers V computers.
37) Shear registers And schemes their applications.

Topic 18. Counters and their application diagrams.

38) Application synchronous counters With asynchronous transfer.
39) Synchronous counters And their application. Topic 19. Memory: constant And operational.
40) ROM How universal combinational chip. Firmware ROM-based machines.
41) RAM How informational buffer.

Topic 20. Digital-to-analog And analog-to-digital converters.

42) Consistent and integrating ADCs.
43) Serial DACs.
44) Parallel DAC.

Criteria assessments competencies:

Grade "Great" is exhibited to a student, If student gave full, expanded answer to delivered question, at this shown totality conscious knowledge By topic disciplines, evidentially revealed main provisions question; V answer can be traced A clear structure and logical sequence reflecting the essence of the concepts being explored. The answer is presented in literary language using technical terminology. There may be admitted shortcomings V definition concepts, corrected student on one's own in the process of answering. The situational task on the topic was solved correctly.

Grade "Fine" is exhibited to a student, If student gave full, expanded answer to the question posed, demonstrating the ability to identify essential and non-essential features, cause-and-effect relationships. Answer clearly structured, logical, presented in literary language using technical terminology. 2-3 may be allowed inaccuracies or insignificant mistakes, corrected student With help teacher. Situational task the topic has been resolved that's right, but with her the decision was made no more than one error.

A "satisfactory" grade is given to a student if the answer is insufficiently complete or detailed. The logic and consistency of presentation are flawed. Errors were made in the clarification of concepts and the use of terms. The student is unable to independently identify essential and nonessential features and cause-and-effect relationships. The answer lacks conclusions. Ability to reveal the significance of generalized knowledge Not shown. Speech design requires amendments, corrections. Situational The problem on the topic was solved correctly, but no more than two mistakes were made in solving it.

Grade unsatisfactory is exhibited to a student, If answer represents The knowledge is fragmented and contains significant errors on the issue. The presentation is fragmentary and illogical. The student does not understand the connection between the issue under discussion and other issues. topics. None conclusions, specification And evidentiality presentation. Speech illiterate, terminology Not is used. Additional And clarifying questions The teacher's comments do not lead to the student's answer being corrected, or the answer to the question is completely missing, or the student refuses to answer. The situational problem on the topic is solved incorrectly.

Description of the rating scale

Grade for answers on questions V in the course interviews is determined V in accordance With tab-
lyceum.

Grade	Grade for theoretical-Czech question basic level	Grade for theoretically sky question advanced level	Note
Great	Great (Fine)	Great	Grade Fine only allowed By basic level question
Fine	Good (satisfactory)	Fine	Grade satisfactory acceptable only By in- I'll ask basic level
satisfactorily	Satisfactorily	Satisfactorily	
unsatisfactory	By alone or two questions received an unsatisfactory grade		

Methodological materials defining the procedures for assessing knowledge, skills, and abilities and (or) experience of activities characterizing the stages of formation of competencies

The procedure for conducting this assessment event includes an interview By two theoretical questions from numbers listed. One question refers to To basic level, and the second one – to the advanced level. During the interview, the student has the right to use his own notes.

The questions offered to the student allow for testing professional competencies PC-2. Fundamental differences tasks basic level from increased consist in the complexity of questions according to the level of training “understanding”.

To prepare for this assessment event, 13.5 hours are required in the 5th semester. *(approximately 1 hour on every topic*) And 9 hours V 6th semester (approximately 1 hour on each topic). The student must prepare written answers to the listed theoretical questions . V view notes educational material And on their basis prepare To specified V methodological materials questions For discussions.

When assessing the assignment, the following are assessed: active participation in the work; confident mastery of the material; the ability to clearly and logically express one's thoughts; the ability to creatively approach the main issues of the topic; independent thinking, full compliance of the notes with the established requirements; independent oral speech that fully reveals the essence of the interview issues.

Evaluative sheet

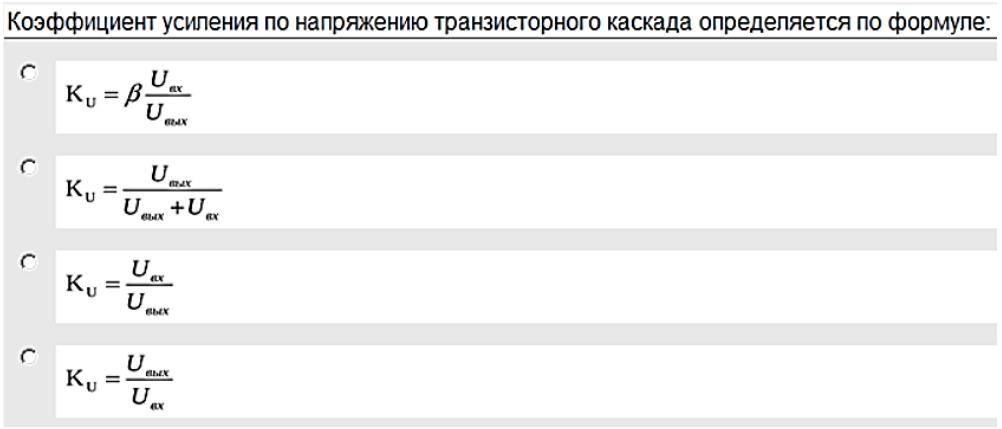
Item No.	Last name, first name of the student.	Type of work						Result
		Working with additional sources of information formations	Answers to intermediate questions	Logic and scientific presentation	Formulating conclusions and evidence	Presentation of the results of the work	Participation in discussion, skill conduct a dialogue	
1								
2								
…								

5. COMPUTER TESTS FOR SELF-TESTING, TEST PREPARATION

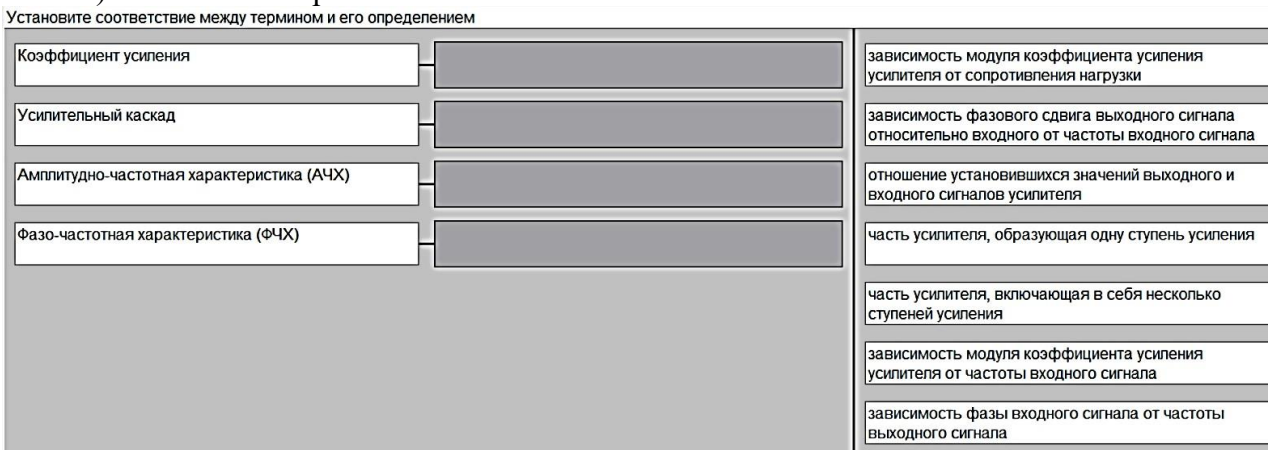
5th semester

The test tasks are designed as two tests in the Iren program, each with 100 tasks. 200 test tasks different level: on choice answer; on input answer; on compliance; for classification.

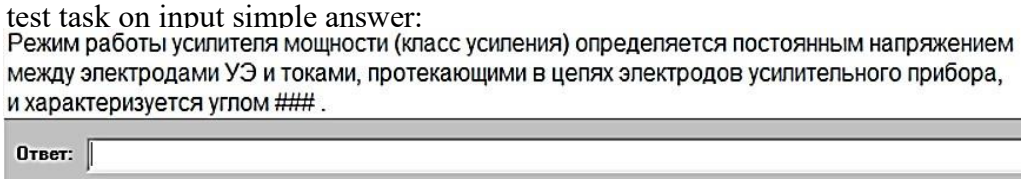
Examples test tasks basic level: a) test task to choose the answer:



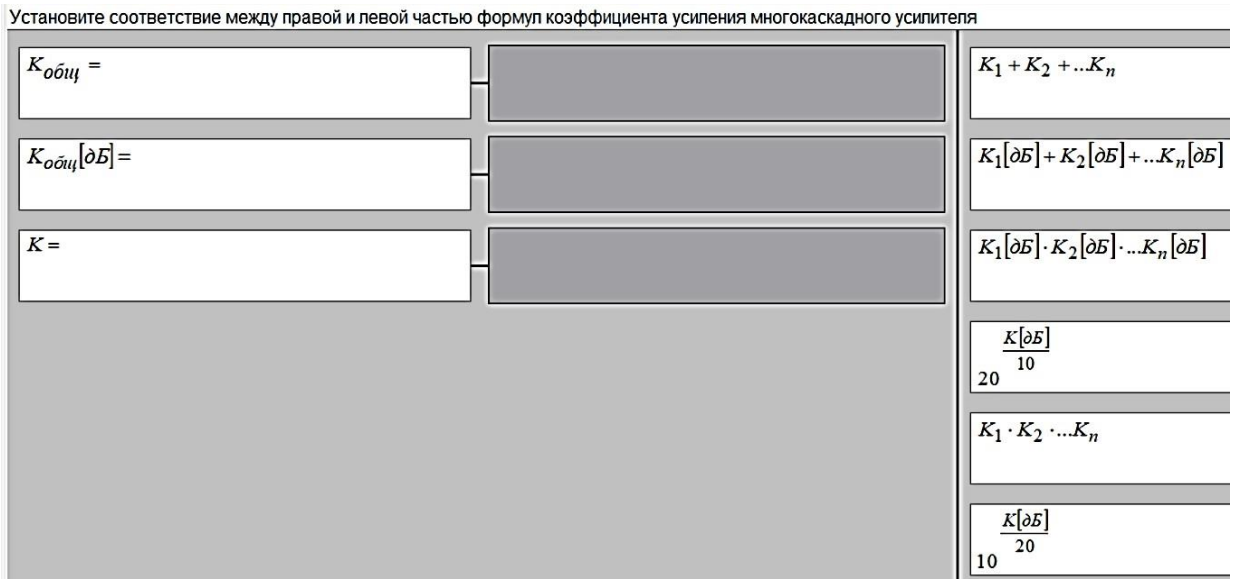
b) test task on simple match:



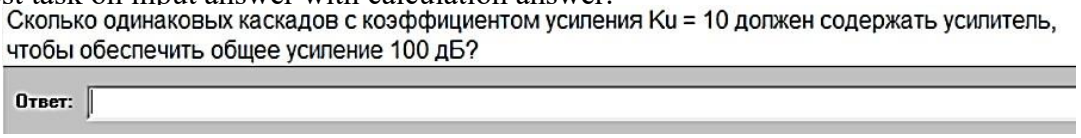
V) test task on input simple answer:



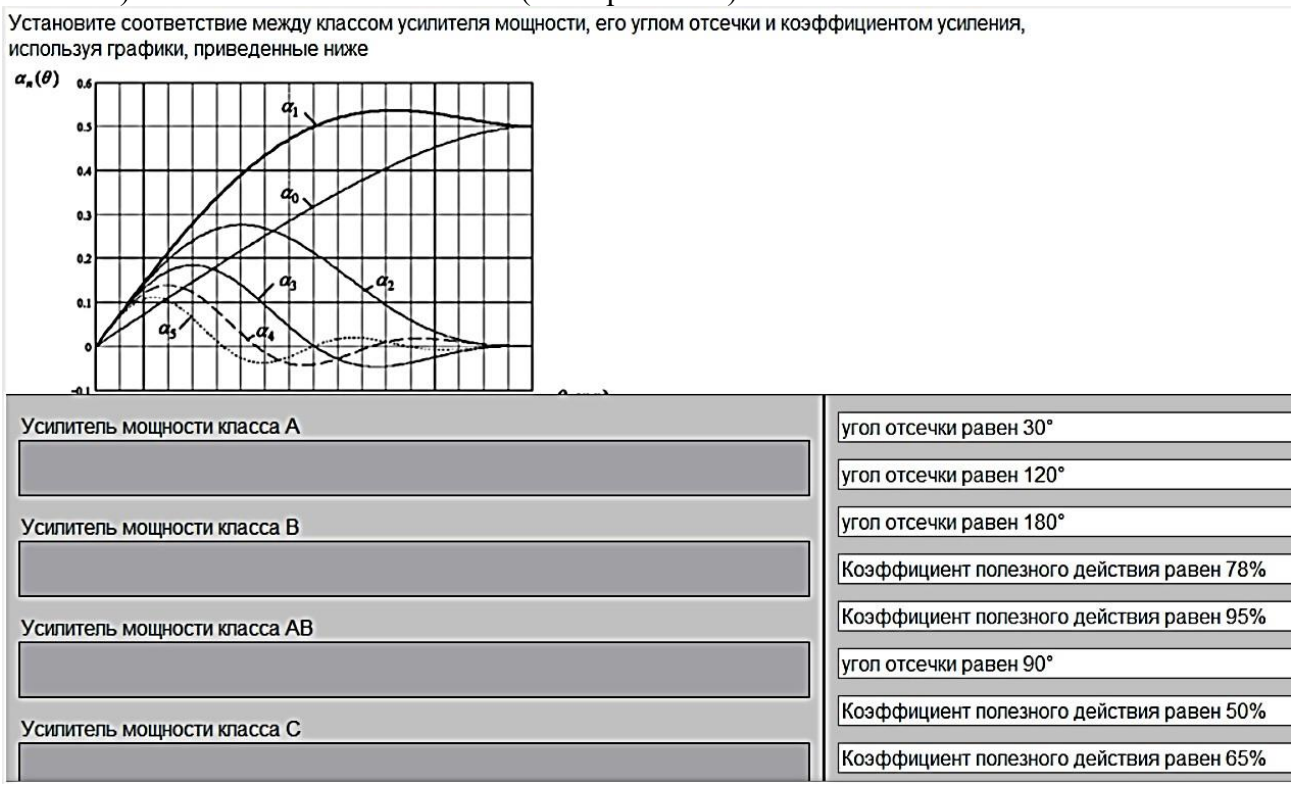
Examples test tasks increased level: a) test task for complex matching:



b) test task on input answer with calculation answer:



V) test exercise on classification (correspondence):



6th semester

The test tasks are designed as two tests in the Iren program, each with 100 tasks. 200 test tasks different level: on choice answer; on input answer; on compliance; for classification.

Examples test tasks basic level: a) test task to choose the answer:

Полный одноразрядный сумматор это комбинационное устройство, содержащее

- 2 входа и 2 выхода
- 3 входа и 3 выхода
- 3 входа и 2 выхода
- 2 входа и 1 выход
- 1 вход и 1 выход

b) test task on simple match:

Соответствие между таблицей истинности и соответствующим ей логическим элементом

0¤	1¤	
1¤	0¤	

0	0	0
0	1	0
1	0	0
1	1	1

0	0	1
0	1	0
1	0	0
1	1	0

0	0	0
0	1	1
1	0	1
1	1	0

И-НЕ

ИЛИ-НЕ

ИСКЛЮЧАЮЩЕЕ ИЛИ

И

НЕ

V) test task on input simple answer:

Мультиплексор состоит из ____ и селектора (ввести слово строчными буквами)

Ответ:

Examples test tasks increased level: a) test task for complex matching:

Соответствие между цифровым устройством и его таблицей истинности

0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

0	0	X_0	X_1	X_2	X_3	X_0
0	1	X_0	X_1	X_2	X_3	X_1
1	0	X_0	X_1	X_2	X_3	X_2
1	1	X_0	X_1	X_2	X_3	X_3

0	0	X	X	-	-	-
0	1	X	-	X	-	-
1	0	X	-	-	X	-
1	1	X	-	-	-	X

дешифратор 2x4

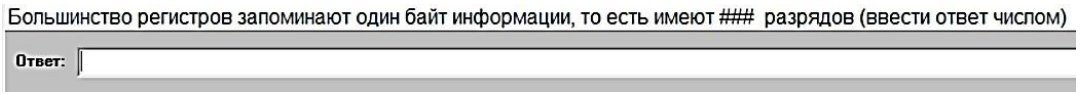
полусумматор

шифратор 4x2

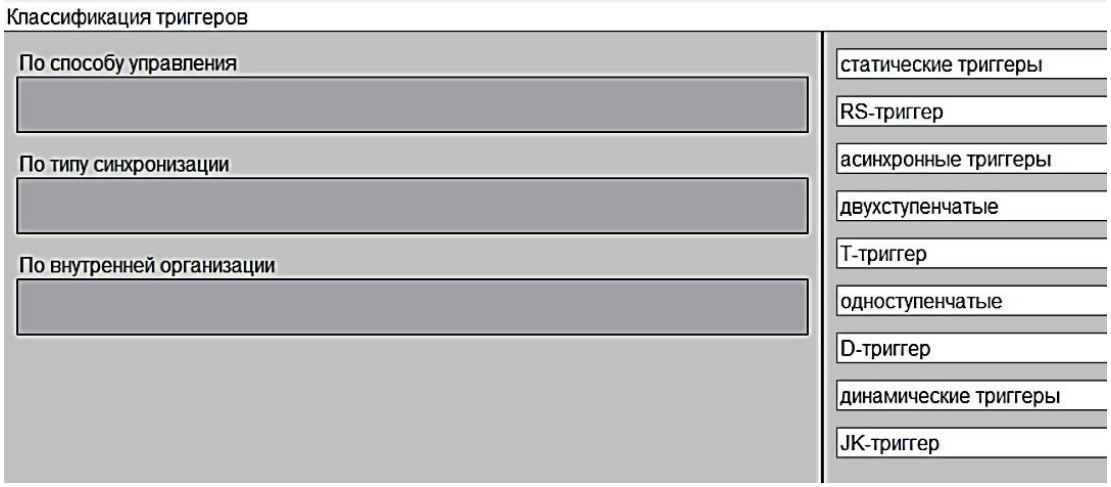
демультиплексор 1x4

мультиплексор 4x1

b) test task on input answer with calculation answer:



V) test exercise on classification (correspondence):



Description rating scales computer testing

One basic-level test assignment is worth 1 point, and one advanced-level test assignment is worth 2 points. The Iren program randomly selects the number of test assignments specified by the teacher (usually 15-20 assignments).

General quantity points for the test is determined according to the formula:

$$TO = \frac{m_b + 2 \cdot m_p}{n_b + 2 \cdot n_p} \cdot 100\% \text{ at this } n_b + n_p = N$$

where m_b – the number of correct answers to basic level test tasks, m_p - quantity correct answers on test tasks increased level, n_b – quantity given test tasks basic level, n_p - quantity given test tasks advanced level, N is the total number of test tasks.

The current test is considered passed if the student received no. less 53 % from established For this control maximum points. Rating the score awarded to a student for the current test, submitted by the student within the timeframe established by the schedule of test activities, is determined as follows:

Level execution control tasks	**Rating score (V % from maximum points for the test task)**
Great	**Not less 88**
Good	**from 72 up to 87**
Satisfactory	**from 53 to 71**
Unsatisfactory	**less 53**

Methodological materials, defining procedures assessments knowledge, skills, abilities and (or) experience of activities characterizing the stages of formation of competencies Procedure conducting this evaluative events includes V myself computer testing With help test programs "Iren". This program By random law you- chooses from general list tasks, indicated teacher number tasks By each topic disciplines . As a rule one test contains 15-20 test tasks. To answer for one task provided 1 - 2 minutes.

TO test questions basic level relate questions With choice answer, questions With input answer and simple questions on establishment compliance. To the test questions increased-

The level includes complex questions on establishing correspondence, tasks with calculation and input answer, questions on classification And ordering actions (operations).

Suggested student questions allow check professional competencies PC-2.

For preparation To given evaluative event necessary 13.5 hours V 5th semester *(6.75 hours on every test*) And 9 hours V 6th semester (*4.5 hours on each test*).

The student must prepare for computer testing by mastering the tests and conducting self-testing. Self-testing is produced With help exe files With training test tasks, issued students V beginning semesters training.

Evaluative sheet

No. p/p	Surname, student's name .	Quantity test tasks	Number of correct answers	Typed points	Total grade
1					
2					
…					

6. SET MULTI-LEVEL TASKS FOR COMPUTER MODELING USING GRAPHIC EDITORS

5th semester

Base level

Laboratory Job 1. Study parameters And characteristics amplifying device based on its circuit model for the variable component of the signal.

1) Develop a circuit model of an amplifying device in the form of a hybrid U-shaped equivalent circuit using a computer simulation software package.

2) Conduct check performance And debugging models amplifying device-state.

3) Conduct analysis developed circuit design models amplifying device-state.

Laboratory Job 2. Study amplifiers voltage on bipolar transit-stores.

4) Perform a theoretical calculation of the main parameters of an amplifier using a common emitter circuit.

5) Collect V software package computer modeling schematic model of an amplifier using a common emitter circuit.

6) Conduct check performance And debugging models amplifier By scheme With common emitter.

7) Conduct study main parameters And characteristics amplifier By common emitter circuit.

8) Perform a theoretical calculation of the main parameters of an amplifier using a common collector circuit.

9) Collect V software package computer modeling schematic model of an amplifier using a common collector circuit.

10) Conduct check performance And debugging models amplifier By scheme With common collector.

11) Conduct study main parameters And characteristics amplifier By common collector circuit.

Laboratory work 3. Study of the influence of negative feedback on the characteristics of amplifying devices.

12) Assemble a basic electrical circuit diagram of a common emitter amplifier with various types of negative feedback using a computer simulation software package.

13) Conduct check performance And debugging models amplifier With common emitter and with various types of negative feedback.

14) To investigate the beneficial properties of negative feedback in a common emitter amplifier.

15) Conduct a study of the influence of negative feedback on the amplification properties and frequency characteristics of an amplifier with a common emitter.

Laboratory Job 4. Study aperiodic amplifying stages.

16) Produce calculation And modeling aperiodic amplification stage.

17) Conduct a performance test and debugging of the aperiodic amplifier cascade model.

Laboratory Job 5. Study amplifiers power.

18) Assemble a basic electrical circuit diagram of a push-pull power amplifier using a computer simulation software package, test its performance, and debug it.

19) Conduct analysis characteristics two-stroke amplifier power. Lab 6.

Study of operational amplifiers.

20) Assemble a basic electrical circuit diagram of an amplifier using an operational amplifier in a computer simulation software package, test its performance and debug it.

21) Conduct study parameters operating amplifier By permanent current.

22) Collect V software package computer modeling principled electrical circuit of a non-inverting amplifier based on an operational amplifier, check its performance and debug it.

23) Conduct a study of the operating principles, parameters and characteristics of a non-inverting amplifier.

24) Assemble a circuit diagram of an inverting amplifier using an operational amplifier using a computer simulation software package, test its performance, and debug it.

25) Conduct a study of the operating principles, parameters and characteristics of an inverting amplifier.

Laboratory work 7. Research of functional circuits based on operational amplifiers.

26) Assemble a basic electrical circuit diagram of an adder and subtractor on an operational amplifier using a computer simulation software package, test their performance and debug them.

27) Conduct study principles work And parameters adder, subtractor on an operational amplifier.

28) Assemble the basic electrical circuit in a computer modeling software package diagram differentiator on operating amplifier, produce check its performance and debugging.

29) Assemble a basic electrical circuit diagram of an integrator on an operational amplifier in a computer simulation software package, test its performance and debug it.

Laboratory Job 8. Study active filters on operating strengthen-Pole.

30) Calculate parameters ARC filter lower frequencies second order.

31) Collect V software package computer modeling principled electrical diagram ARC filter lower frequencies second order, produce check its performance and debugging.

32) Conduct study characteristics ARC filter lower frequencies second By-row.

33) Calculate parameters ARC filter top frequencies second order.

34) Collect V software package computer modeling principled electrical diagram ARC filter top frequencies second order, produce check its performance and debugging.

35) Conduct study characteristics ARC filter top frequencies second By-row.

Laboratory Job 9. Research of autogenerators.

36) Collect V software package computer modeling principled electrical diagram autogenerator on an op-amp with a Wien bridge, produce checking its functionality and debugging.

37) Conduct a study of the operating principles, parameters and characteristics of an op amp generator with a Wien bridge.

38) Assemble the basic electrical circuit in a computer modeling software package diagram RC generator on OU With phase-shifting chain "R-parallel" - carry out a check of its functionality and debugging.

39) Conduct a study of the parameters of an RC generator based on an op-amp with an "R-parallel" phase-shifting circuit.

Increased level

Laboratory work 1. Study of the parameters and characteristics of an amplifying device based on its circuit model for the variable component of the signal.

40) Study of frequency properties of the amplifier model (amplitude-frequency and phase-frequency characteristics, range reinforced frequencies) And emerging frequency distortions .

41) Study amplitude characteristics models amplifier, his sensitivity, dynamic range and the resulting nonlinear distortions.

Laboratory work 2. Research of voltage amplifiers on bipolar transistors .

42) Perform a theoretical calculation of the main parameters of an amplifier using a common base circuit.

43) Collect V software package computer modeling schematic model of an amplifier using a common base circuit.

44) Conduct check performance And debugging models amplifier By scheme With common base.

45) Conduct study main parameters And characteristics amplifier By common base scheme.

Laboratory work 3. Study of the influence of negative feedback on the characteristics of amplifying devices.

46) Conduct a study of the influence of negative feedback on the input and output resistance of an amplifier with a common emitter.

Laboratory Job 4. Study aperiodic amplifying cascades.

47) Conduct a study of the aperiodic amplifier stage, determining its gain (transmission) factors and constructing the amplitude-frequency characteristic (AFC) of the aperiodic amplifier stage and assessing its range properties.

48) Conduct research into an aperiodic amplifying stage, determining the influence of resistance values on the position of the transistor operating point, on the parameters and quality indicators of the amplifying stage.

Laboratory Job 5. Study amplifiers power.

49) Assemble a basic electrical circuit diagram of a power amplifier with transformer coupling in a computer simulation software package, conduct its performance test and debugging.

50) Conduct analysis characteristics amplifier power With transformer communication.

Laboratory work 6. Study of operational amplifiers.

51) Assemble the basic electrical circuit in a computer modeling software package diagram differential amplifier on operating amplifier, check its functionality and debug it.

52) Conduct a study of the operating features and parameters of a differential amplifier.

53) Assemble a basic electrical circuit diagram of a comparator on an operational amplifier in a computer simulation software package, test its performance and debug it.

54) Conduct study comparators on base operating amplifiers.

Laboratory work 7. Research of functional circuits based on operational amplifiers.

55) Conduct study principles work And parameters differentiator on operational amplifier.

56) Study principles work And parameters integrator on operating amplifier .

Laboratory Job 8. Study active filters on operating strengthen-
Pole.

57) Collect V software package computer modeling principled
electrical diagram ARC filter lower frequencies fourth order, produce checking its functionality and debugging.

58) Conduct study characteristics ARC filter lower frequencies fourth By-
row.

59) Collect V software package computer modeling principled
electrical diagram ARC filter top frequencies fourth order, produce checking its functionality and debugging.

60) Conduct a study of the characteristics of a fourth-order high-pass ARC filter .

61) Assemble the basic electrical circuit in a computer modeling software package diagram striped ARC filter second order, produce check his performance and debugging.

62) Conduct study characteristics striped ARC filter second order. Laboratory work 9. Study of autogenerators.

63) Assemble the basic electrical circuit in a computer modeling software package diagram RC generator on OU With phase-shifting chain "C-parallel" - carry out a check of its functionality and debugging.

64) Conduct a study of the parameters of an RC generator on an op amp with a phase-shifting chain “C-parallel”.

6th semester

Base level

Laboratory work 10. Study of the basics of Boolean logic. Minimization of logical functions.

1) Confirmation commutative law Boolean algebra With help circuit simulation programs.
2) Confirmation associative law Boolean algebra With help circuit simulation programs.
3) Confirmation law repetitions Boolean algebra With help programs circuit simulation.
4) Confirmation law double inversions Boolean algebra With help circuit simulation programs.
5) Confirmation of the laws of the universal and zero sets of Boolean algebra using a circuit simulation program.
6) Confirmation distribution law Boolean algebra With help programs for circuit simulation.
7) Confirmation of De Morgan's Law of Boolean Algebra using a circuit simulation program.
8) Confirmation of the laws of complementarity, absorption and gluing of Boolean algebra using a circuit simulation program.

Laboratory Job 11. Study basic logical elements.

9) Conduct analysis logical ventilator on transistor.
10) Conduct analysis logical element NOT (inverter).
11) Conduct analysis buffer element.
12) Conduct analysis features work buffer element on three states.
13) Conduct analysis logical elements AND, AND- NOT.
14) Conduct analysis logical elements OR And OR- NOT.

Laboratory Job 12. Study combinational digital devices: sum-
tori.

15) Conduct a study of the internal structure and operating logic of a half adder using a logic converter and a word generator.

16) Conduct a study of the internal structure and operating logic of a full adder using a logic converter and a word generator.

17) Conduct study logic functioning 4-x discharge adder With using a word generator.

Laboratory Job 13. Study combinational digital devices: encoders and decoders.

18) Synthesize And research logic functioning decoder 3x8 With using a logical converter and a word generator.

19) Research logic functioning decoder 4×16, realized V in the form of IMS 74154 (K155ID3) using a word generator.

20) Synthesize and investigate the operating logic of an 8x3 encoder using a logic converter and a word generator.

21) Research logic functioning encoder 8×3, realized V in the form of IMS 74148 (KM555IV1) using a word generator.

Laboratory work 14. Research of combinational digital devices: multiplexers and demultiplexers.

22) Synthesize and investigate the operating logic of a 4-channel multiplexer using a logic analyzer.

23) Research the operating logic of an eight-channel selector-multiplexer, implemented in the form of an IMS 74151 (KM155KP7) using a logic analyzer.

24) Synthesize And research logic functioning 4-x channel demultiplexer using a logic analyzer.

Laboratory Job 15. Research of triggers.

25) Research internal structure And logic functioning simplest RS trigger using a word generator.

26) Research internal structure And logic functioning synchronous single-stage RS trigger using a word generator.

27) To investigate the operating logic of a synchronous two-stage JK trigger With straight clock entrance And entrances presets With help generator words and a logic analyzer.

28) To investigate the operating logic of a counting T-trigger using a word generator and a logic analyzer.

29) To investigate the operating logic of a two-stage D-trigger using a word generator and a logic analyzer.

30) Research logic functioning And methods applications trigger Schmitt. Laboratory work 16. Study of registers.

31) To explore the internal structure and logic of the functioning of the sequential four-digit register shift With help generator words And logical analyzer .

32) Explore the internal structure and logic operation of a parallel four-bit register using a word generator and a logic analyzer.

33) To investigate the logic of operation of the universal register on the 74195 (K155IR12) IC using a word generator.

Laboratory Job 17. Research of counters.

34) To investigate the internal structure and operating logic of a sequential three-digit counter using a word generator and a logic analyzer.

35) To investigate the internal structure and operating logic of a modulo-5 counter using a word generator and a logic analyzer.

36) To investigate the operating logic of a binary reversible counter with the possibility of parallel recording initial IC based code 74169 (K155IE17) using a word generator and a logic analyzer.

Laboratory work 18. Research of operational and permanent memory, input-output devices.

37) To investigate the internal structure and operating logic of a static random access memory cell using a word generator.

38) To investigate the internal structure and operating logic of a dynamic random access memory cell using an oscilloscope.

39) To investigate the internal structure and operating logic of a single-bit bus former.

40) To explore the internal structure and operating logic of a four-digit tire shaper on base IMS 74244 With help generator words And seven-segment indicators.

Laboratory Job 19. Study digital-analog And analog-to-digital converters .

41) Synthesis And study DAC With weight resistors.

42) Synthesis And study DAC staircase type.

43) Synthesis And study four-digit DAC staircase type on base counter 74160.

44) Synthesis And study ADC direct transformation.

Increased level

Laboratory Job 10. Study basics Boolean logic. Minimization logical-ical functions.

45) Synthesize logic devices based on a given Boolean function using the Electronics Workbench circuit simulation program.

46) Minimize SDNF With using laws algebra logic.

47) Minimize given logical function With using cards Carnot. Laboratory work 11. Study of basic logic elements.

48) Conduct an analysis of logical elements exclusive OR and equivalence. Laboratory Job 12. Study combinational digital devices: sum-tori.

49) Conduct study logic functioning adder given discharge-sti With help generator words.

50) Synthesize the given adder-subtractor and conduct its study. Laboratory Job 13. Study combinational digital devices: cipher-tori And decoders.

51) Synthesize given fragment schemes encoder keyboards And explore the logic of its functioning.

Laboratory work 14. Research of combinational digital devices: multiplexers and demultiplexers.

52) Synthesize And research logic functioning given By variant of the multiplexer on the IC.

Laboratory Job 15. Research of triggers.

53) Synthesize a circuit of a given trigger in the OR-NOT basis and conduct a study of the logic of its operation.

54) Conduct a study of the internal structure and operating logic of the triggers contained in a given logic microcircuit.

Laboratory Job 16. Research of registers.

55) Conduct a study of the internal structure and operating logic of the register contained in a given logic microcircuit.

56) Synthesize diagram given register And conduct study logic its functioning.

Laboratory Job 17. Research of counters.

57) Conduct a study of the internal structure and operating logic of the counters contained in a given logic microcircuit.

Laboratory work 18. Research of operational and permanent memory, input-output devices.

58) Synthesize And conduct study 4-x bit RAM.

59) Synthesize And conduct study cells ROM memory .

60) Synthesize And conduct study devices input- output.

Laboratory Job 19. Study digital-analog And analog-to-digital converters .

61) Synthesize And conduct study 8 discharge DAC.

62) Synthesize And conduct study ADC, allowing record data V file.

Criteria assessments:

Criteria assessments competencies:

Grade "Great" is exhibited, If student demonstrated high skill apply received knowledge on practice through execution specific tasks advanced level, coped with the assigned task freely and without difficulty, demonstrating mastery of various techniques and skills for its implementation, and did not make any mistakes or inaccuracies.

A grade of “good” is given if the student has demonstrated the ability to apply the acquired knowledge in practice by solving a specific advanced level task and has completed it With delivered task, showing ownership necessary techniques And skills its implementation, at this allowed Not more one mistakes, corrected after instructions teacher .

A grade of “satisfactory” is given if the student has demonstrated mediocre skill apply received knowledge on practice through solution specific advanced level tasks, coped with the task with difficulty, while making no more than two mistakes, corrected after instructions teacher, or successfully completed setting a basic level.

The grade “unsatisfactory” is given if the student has not demonstrated the ability to apply the acquired knowledge in practice by solving a specific basic task. level, Not coped With delivered task or allowed at her execution serious mistakes.

Description of the rating scale

The current test is considered passed if the student received no. less 60% from established For this control maximum points. Rating the score awarded to a student for the current test, submitted by the student within the timeframe established by the schedule of test activities, is determined as follows:

Level execution control for-Denmark	Rating score (in % from maximum score for the test task)
Great	100
Good	80
Satisfactory	60
Unsatisfactory	0

Methodological materials defining the procedures for assessing knowledge, skills, abilities and (or) work experience, characterizing the stages of competence development

Procedure conducting this evaluative events includes V myself:

— performance designed report By laboratory work With completed multi- level tasks;

— protection by way execution specified teacher multi-level tasks, Moreover, the level of the task being completed is determined by the student independently.

Suggested student tasks allow check professional competencies PC-2.

For preparation To given evaluative event student is allocated V 5 semester 27 hours V framework his independent work, A V 6 semester - 15 hours.

At preparation To answer student provided right use report By laboratory work.

Evaluative sheet

No. p/p	Last name, first name of the student.	Type of work						Result
		Proficiency in the methodology for completing the task	Correctness of circuit modeling	device perform ance	Accuracy measurement s and correctness of calculations parameters and characteristic s teristic	Correctness of design of diagrams, characterist ic graphs stick	Formulation conclusions, their compliance with theory	
1								
2								
…								

8. QUESTIONS TO EXAM

Questions For checks level of training

Base level

1) Classification of amplifier devices. Main technical indicators and characteristics of the amplifier.
2) Principles gains electric signal.
3) Typical functional cascades semiconductor amplifier.
4) Aperiodic amplifying cascades V mode small signal.
5) General information about feedback in amplifiers. Amplifiers with series negative current and voltage feedback.
6) General intelligence about reverse connections V amplifiers. Amplifiers With parallel negative feedback on current and voltage.
7) Amplifying cascade With common emitter (With common source).
8) Amplifiers cascades With general base (with a shutter) And With common collector (drain).
9) Gain pulse signals.
10) Transformer amplifying cascades.
11) Methods increases coefficient gain. Low frequency correction gain.
12) Simple parallel high-frequency gain correction .
13) High frequency correction gains for check consistent negative current feedback (Z-type).
14) Multi-cascade Amplifiers. General Provisions.
15) Multi-cascade amplifiers With RC connections.
16) Multi-cascade amplifiers permanent current.
17) General intelligence, parameters, characteristics and equivalent scheme operational amplifier.
18) Operational amplifier circuit diagrams. Static errors of operational amplifiers.
19) Voltage adders, differentiators and integrators on operational amplifiers .
20) Logarithmic amplifier And exponential generator, schemes multiplication of capacitance and transformation of resistance on operational amplifiers.
21) Amplifier variable current on operating amplifier. Comparator.
22) Multipliers And dividers on operating amplifiers.
23) Conditions And modes self-excitation of generators.
24) Generators With resonant chains.
25) RC generators on operational amplifiers.

Increased level

1) Levels performances digital devices. Technologies digital microcircuits, characteristics of their inputs and outputs.
2) Basic logical elements: inverters; repeaters And buffers, elements AND, AND- NOT, OR, OR-NOT.
3) Elements Exclusive OR. Combined logical elements. Schmitt triggers .
4) Combinational circuits: decoders And encoders.
5) Combinational circuits: multiplexers And comparators codes.
6) Combinational schemes: adders And converters codes.
7) Monostable multivibrators And generators.
8) Basics constructions And classification triggers. Principle work typical RS triggers.

9) Principle work typical JK flip-flops And D- triggers.

10) Main schemes inclusions triggers: synchronization signals, delay lines .

11) Main schemes inclusions triggers: formers signals, filtration And Manchester code encoder.

12) General intelligence O registers. Parallel registers, triggered By front.

13) Application parallel registers V computers.

14) General intelligence O registers. Parallel registers, triggered By level.

15) General information about registers. Shift registers and schemes for their application.

16) General information about counters. Asynchronous counters. Applications of asynchronous counters.

17) General intelligence O counters. Synchronous counters With asynchronous transfer.

18) Application synchronous counters With asynchronous transfer. Interval and pulse train formers.

19) Application of synchronous counters with asynchronous carry. Time interval and pulse frequency meters.

20) General information about counters. Synchronous counters.

21) Application synchronous counters. Controlled frequency divider .

22) General intelligence O permanent memorizing devices (ROM).

23) ROM How universal combinational chip. Firmware ROM-based machines.

24) General intelligence about operational memorizing devices. RAM For temporary storage of information.

25) RAM How informational buffer.

Practical tasks For checks level of training

1) Collect V software package computer modeling a circuit model of an amplifying device in the form of a hybrid U-shaped equivalent circuit, and conduct research into its characteristics.

2) Collect V software package computer modeling circuit model of an amplifier using a common emitter circuit, and conduct a study of its main parameters and characteristics.

3) Collect V software package computer modeling schematic model amplifier By scheme With common collector, conduct study his main parameters and characteristics.

4) Use a computer simulation software package to construct a schematic diagram of a common-emitter amplifier with various types of negative feedback. Research the beneficial properties of negative feedback.

5) Assemble in a computer simulation software package a basic electrical circuit diagram of an amplifier with a common emitter and with different types of negative feedback connections. Conduct study influences OOS on amplifying properties And frequency characteristics of the amplifier.

6) Simulate V software package computer modeling aperiodic amplifier stage, check its performance, perform DC tuning, conduct a study of the main parameters and characteristics.

7) Simulate V software package computer modeling aperiodic amplifier stage, check its performance, carry out adjustments for alternating current, conduct a study of the main parameters and characteristics.

8) Assemble the circuit diagram of an operational amplifier using a computer simulation software package, test its performance, and conduct a study of its DC parameters.

9) Assemble the basic electrical circuit in a computer modeling software package diagram non-inverting operating amplifier, check his performance, conduct a study of its parameters and characteristics.

10) Assemble a basic electrical circuit diagram of an inverting operational amplifier using a computer simulation software package, test its performance, and conduct a study of its parameters and characteristics.

11) Assemble a basic electrical circuit diagram of a differential operational amplifier using a computer simulation software package and conduct a study of its operating features and parameters.

12) IN software package computer modeling conduct analysis logical elements: NOT (inverter), buffer element for three states, AND, AND-NOT, OR And OR-NOT.

13) IN software package computer modeling conduct analysis logical elements exclusive OR and equivalence, Schmitt trigger.

14) To simulate in a computer simulation software package and investigate the internal structure and operating logic of a half adder and a full adder using a logic converter and a word generator.

15) To simulate in a computer simulation software package and investigate the operating logic of a 4-bit adder using a word generator.

16) To simulate in a computer simulation software package and investigate the operating logic of a 4×16 decoder, implemented in the form of an IC 74154 (K155ID3) using a word generator.

17) To simulate in a computer simulation software package and investigate the operating logic of an eight-channel selector-multiplexer, implemented in the form of an IC 74151 (KM155KP7) using a logic analyzer.

18) Model in a computer simulation software package and explore internal structure And logic of functioning synchronous single stage RS trigger using a word generator.

19) To simulate in a computer simulation software package and investigate the operating logic of a synchronous two-stage JK flip-flop with direct clock input and preset inputs using a word generator and a logic analyzer .

20) To simulate in a computer simulation software package and investigate the operating logic of a counting T-trigger using a word generator and a logic analyzer.

21) To simulate in a computer simulation software package and investigate the operating logic of a two-stage D-trigger using a word generator and a logic analyzer.

22) To simulate in a computer simulation software package and investigate the internal structure and operating logic of a sequential four-bit shift register using a word generator and a logic analyzer.

23) To simulate in a computer simulation software package and investigate the operating logic of a universal register on an IC 74195 (K155IR12) using a word generator.

24) To simulate in a computer simulation software package and investigate the internal structure and operating logic of a modulo 5 counter using a word generator and a logic analyzer.

25) Model in a computer simulation software package and explore logic functioning binary reversible counter With opportunity parallel records initial code on basis IMS 74169 (K155IE17) With help generator words and a logic analyzer.

Criteria assessments competencies

(*V in accordance With results development disciplines* **)**

Criteria assessments For checks level theoretical training *:*

An “excellent” grade is given to a student if he has demonstrated a deep, solid and reasoned mastery of the program educational material, while the question posed is disclosed consistently, clearly and logically, in a full and exhaustive manner, the main categories, concepts and terms the course materials were formulated correctly, no mistakes were made in the answers

A “good” grade is given to a student if he/she has demonstrated a solid knowledge of the program educational material, while the question posed was answered competently and to the point, in sufficiently full volume, the main categories, concepts and terms of the course were formulated correctly, and individual inaccuracies or one mistake were made in the answer.

A “satisfactory” grade is given to a student if he/she has demonstrated knowledge of only the main part of the educational material without its specific details, while the question posed is answered With violation logical sequences, Not V full volume; were Inaccurate formulations of the main categories, concepts and terms of the course were allowed, as well as errors (no more than two) or a number of minor inaccuracies that did not significantly distort the essence of the answer.

Grade unsatisfactory is exhibited to a student, which Not knows A significant portion of the program material contains significant errors (more than two) that significantly distort its essence. A failing grade is also given if the answer to a question is missing or the student refuses to submit it.

Criteria assessments For checks practical training:

An “excellent” grade is given if he has demonstrated a high ability to apply acquired knowledge in practice through solving a specific problem, freely and without difficulty coped with the task at hand, demonstrating mastery of various techniques and skills for its implementation, and did not make mistakes or inaccuracies;

A grade of “good” is given if he has demonstrated the ability to apply the acquired knowledge knowledge on practice through solution specific tasks, coped With delivered task, demonstrating mastery of the necessary techniques and skills for its implementation, while making no more than one mistake;

a “satisfactory” grade is given if he demonstrated a mediocre ability to apply the acquired knowledge in practice by solving a specific problem, coped with the assigned task with difficulty, and made no more than two mistakes;

The grade "unsatisfactory" is given if the student has not demonstrated the ability to apply the acquired knowledge in practice by solving a specific problem, has not completed the assigned task, or has made three or more serious mistakes in solving it.

If student on exam allowed happening violations educational disciplines (cheating, use of mobile communications, personal or tablet computers, audio- or video players, others technical devices), That given student is being removed With exam with an unsatisfactory grade.

Methodological materials defining the procedures for assessing knowledge, skills, and abilities and (or) experience of activities characterizing the stages of formation of competencies

Suggested student tasks allow check professional PC-2 competencies. The student is given 27 hours of independent work to prepare for the exam.

The examination procedure is carried out in accordance with the Regulation on the current monitoring of academic performance and midterm assessment of students in higher education programs at SKFU.

Exam By discipline provided V oral form By tickets. IN The examination ticket includes two theoretical questions and one practical task.

For preparation By ticket is allocated 30 minutes - on theoretical questions, 10 minutes to complete a practical assignment.

When preparing for an answer, the student is given the right to use the course work program and his own lecture notes for no more than 10 minutes.

The practical assignment is completed on a personal computer. When assessing the practical assignment, the following is assessed: right modeling, methods research, accuracy results measurements, error assessment.

9. EVALUATION MEANS FOR COURSEWORK PROJECT

1. Approximate subject matter coursework project *(For each species activities, provided by the educational program of higher education)*

Type of activity	Approximate topics
project	***Base level***
	1 – 5. Design of a pre-amplifier stage according to the circuit with common emitter And autogenerator on operating amplifier (5 options).
	6 - 10. Design weekend amplifying cascade By push-pull circuit and transistor oscillator according to Clapp's circuit (5 variants).
	11. Design decoder D4_16 cascading structures And counter With arbitrary coding.
	12. Design of a single-digit full subtractor on a decoder and a counter with a variable modulus.
	13. Design five input majority element and controlled divider frequencies on counter and multiplexer.
	14. Design pyramidal multiplexer And shaper pulses on the counter
	15. Design majority element on multiplexer and counter By module on the shift register.
	Increased level
	1. Design multi-stage (three-stage) amplifier With RC connections .
	2. Design of functional devices (adder and integrator) based on operational amplifiers.
	3. Design functional devices (adder And differentiator) based on operational amplifiers.
	4. Design analog multiplier And divider on base operational amplifiers.
	5. Design logarithmic And exponential amplifiers on base operating amplifiers.
	6. Design transistor selective amplifier high frequencies.
	7. Design transistor amplifier intermediate frequencies.
	8. Design transistor amplifier low (sound) frequencies.
	9. Design transistor limiter amplitudes high-frequency signals.
	10. Design of transistor frequency converter .
	11. Design detector amplitude-modulated signals.
	12. Design of a frequency detector.
	13. Design of Manchester code decoder.
	14. Design generator pseudo-random sequences.
	15. Design of the detector 3 of 6 on the multiplexer And 5-bit dis-divider bars on based on the ring self-healing register .

2. Project structure

The course project has the following compositional structure: title page, content, introduction, main text, conclusion, list of sources used, appendices .

IN structure project highlight two parts: theoretical And empirical (practically-
(I'll
tell IN theoretical parts project (1st chapter project) is being carried out analysis of principles By-
you).
buildings And work objects research (designed devices) on basis review scientific, scientific information, reference literature.

In the empirical (practical) part, consisting of two sections, the following tasks are carried out respectively: calculation And modeling objects research (designed devices), study of the parameters and characteristics of devices using developed models.

Theoretical part of the project

Results training	Formulation tasks	Controlled competencies, indicator(s)	
Understands And etsya V principles By-buildings and works means of cations And their understands modern technical solutions By implementation analog And digital radio-throne devices, is-program used-noe security.	Exercise 1. Conduct ana-Liz principles built-nia And work objects research (project-controlled devices). Exercise 3. Justify choice package butt-nykh computer pro-gram For modeled-niya.	PC- 2 ID-1 PC- 2	
Reveals And analyzes the benefits And under-stats options pro-ect decisions analog-govykh And digital ra-dioelectronic devices.	Exercise 2. Justify the choice fundamental electrical schemes pro-projected devices.	PC- 2 ID-1 PC- 2	

Empirical (practical) Part project

Results training	Formulation tasks	Controlled competencies, indicator(s)	
Carries out collection is-walking data For pro-design analog and digital means of information communications; expression bats technical solutions By their implementation tions.	Exercise 1. To implement collection original data, necessary For project-tization of specified devices. Exercise 2. Choose those-economic decisions on design given-nykh devices.	PC- 2 ID-1 PC- 2	

Develops circuit design solutions for the components of radio-electronic equipment, selects the element base for the development of circuit design solutions, carries out automated modeling And check technical	Task 3. Select the elemental base for development of circuit solutions for the designed devices. Task 4. Perform circuit simulation of the designed devices V chosen-nom package applied	PC-2 ID-1 PC-2	
characteristics of modernized electronic equipment.	computer prog rams .		
Conducts calculations parameters And characteristics of analog And digital means of infocommunications , analyzes their quality indicators based on radio measurements, using specialized software provision for their design .	Exercise 5. Conduct measurement And calculation parameters And characteristics of the designed devices using specialized software provision . Exercise 6. Conduct analysis results research of parameters and characteristics designed devices, sform-to simulate conclusions.	PC-2 ID-1 PC-2	
Develops design documentation in the form of electrical diagrams and explanatory notes To him V in accordance with standards and technical regulations; develops and presents presentation materials for the project .	Task 7. Prepare and submit design documentation (project report) in the form of electrical circuits of the developed devices and explanatory notes in accordance with ESKD standards. Exercise 8. Develop and imagine presentation-these materials For for the protection of the project.	PC-2 ID-1 PC-2	

2. Description of the rating scale

The main ones assessed elements (indicators) coursework project are:

1) quality reporting documentation: graphic parts GC (drawings devices) And calculation and explanatory note (CER) of the course project:

– semantic content calculation and explanatory notes V in accordance With topic and assignment for the course project;

– documentary (textual and illustrative) design of the calculation and explanatory notes And graphic parts (drawings devices) V in accordance With requirements Unified System for Design Documentation and Methodological Guidelines.

2) Review work supervisor about quality work student.

3) Protection project on meeting examination commissions:

– quality contents report;

– quality presentations (visual performances report);

– quality answers on questions members commissions.

In accordance with the University Regulation “On the organization of the educational process on basis rating systems knowledge students…» grade student for The completed and defended course project (CP) is graded by the examination committee based on the rating points earned for each indicator.

Final grade By KP is determined sum points, recruited for quality completion of the project and reporting documentation, as well as the amount of points for its protection. The maximum amount points for completed And protected work is being installed V 100 points. At this 60 points are taken away on current control (standard control), which is being carried out after submission of the report By work on check And comes down to To assessment quality project And reporting documentation.

40 points are allocated for the midterm assessment, which consists of the student defending a course project.

If the project quality and supervisor's feedback score is less than 33 points, the student is required to defend Not allowed, to those pores, Bye Not will eliminate flaws V explanatory note And will not achieve the required amount of points.

Criterion assessments KP V in general And evaluated her elements is excess the sum of the accumulated rating points of the threshold level.

The structure of rating assessments of work elements and the scale for converting rating points into assessments on a 5-point system.

Evaluated element KP	**Max. rating score**	**Rating score**			
		Grade 5	Grade 4	Grade 3	Grade 2
1 Quality reporting documentation (RPZ And GC):	50	44	35	27	<27
1.1 Semantic content RPC	40	36	28	21	0
1.2 Documentary design RPC And GC	10	8	7	6	0
2 Review manager work	10	10	8	6	0
Total for stage execution KP (current control)	60	Not less 33 points For admission To for protection			
3 Protection completed works:	40	36	30	20	<20
3.1 Content report	10	8	7	6	0
3.2 Presentation	10	8	7	6	0
3.3 Answers on questions	20	20	16	12	0
Total for stage protection KR (final control)	40	Not less 20 points For positive assessment			
Total for execution And protection KR	100	88 - 100	72 - 87	53 - 71	<53

Criteria for assigning rating points for the quality of the semantic content of the explanatory note of the CP

Name criteria	**Quantity points**			
	Grade 5	Grade 4	Grade 3	Grade 2
1 Correspondence content of the RPC task at the command post	Fully corresponds to **10 points**	IN basically corresponds to **8 points**	Partially corresponds to **6 points**	Not corresponds to **0 points**
2 Completeness And depth object analysis And subject research-nia	Full **5 points**	Sufficient **4 points**	Partial **3 points**	Absent **0 points**
3 Correctness and accuracy of calculations using a PC	**5 points**	**4 points**	**3 points**	**0 points**
4 Performance And adek-Wattage of circuit models	**10 points**	**4 points**	**3 points**	**0 points**
5 Availability techniques, the correctness and accuracy of the research results	High **10 points**	Good **8 points**	Satisfactory **6 points**	absent **0 points**
6 Availability justified you-conclusions by sections and at work V in general	There is V in full **5 points**	IN basically there is **4 points**	Partially there is **3 points**	Not there is **0 points**

Criteria for assigning rating points for the quality of documentary preparation of reporting documentation for the CP

Name criteria	**Quantity points**			
	Grade 5	Grade 4	Grade 3	Grade 2
1 Correspondence RPC and GC requirements norm- tive documents	Fully corresponds to **5 points**	IN basically corresponds to **4 points**	Partially corresponds to **3 points**	Not corresponds **0 points**
2 Literacy of presentation and quality of presentation of the report	Designed correctly, there are no errors **3 points**	Overall, it is designed correctly, there are some stylistic errors **2 points**	It is designed with a number of errors, there are stylistic and grammatical errors **1 point**	Designed incorrect, a large number of stylistic and grammatical errors **0 points**
3 Volume of the RPC and GC excluding reference appendices	Fully compliant (25 - 35 p.) **2 points**	Fully compliant (25 - 35 p.) **2 points**	Not deviates significantly (up to 3 pages) **1 score**	Deviates significantly (5 And more than pp.) **0 score**

Criteria for assigning rating points for a supervisor's feedback on the quality of a student's work

Grade By 5-point system	**Rating score**
Great	**10**
Fine	**8**
Satisfactorily	**6**
Unsatisfactory	**0**

Criteria exhibits rating points for quality contents report V in the course for the protection of the command post

Name criteria	**Quantity points**			
	Grade 5	Grade 4	Grade 3	Grade 2
1 Correspondence contents report content KP, completeness his lighting	Fully corresponds to **3 points**	IN basically corresponds to **2 points**	Partially corresponds to **1 score**	Not correspo nds to **0 points**
2 Consistency, reasoning and evidence in achieving goals and solving specific design problems	Observed **3 points**	IN basically observed **2 points**	Partially observed **1 score**	Not observed **0 points**
3 Quality And scientific nature presentation, brevity of the report	Clear, free, And laconic **3 points**	Not enough free, With insignificant errors **2 points**	Attachment To text, tongue-tiedness **1 score**	Low, unscientific **0 points**
4 Time report	Complies with regulations **2 points**	Corresponds regulations **2 points**	Insignificantl y Not complies with regulations **1 score**	Does not correspond regulations **0 points**

Criteria exhibits rating points for quality presentations V in the course protection KP

Name criteria	Quantity points			
	Grade 5	Grade 4	Grade 3	Grade 2
1 Correspondence presentation content content to-treasure And KP	Fully corresponds to **3 points**	IN basically corresponds to **2 points**	Partially corresponds to **1 score**	Not corresponds to **0 points**
2 Structure, clarity and completeness of the material demonstrated	There is **3 points**	IN basically there is **2 points**	Partially available **1 score**	No **0 points**
3 Quality graphics, illustrations	High **3 points**	Good **2 points**	Satisfactory **1 score**	Low **0 points**
4 Quantity slides	sufficient for complete presentation of the report **2 points**	sufficient for complete presentation of the report **2 points**	Insufficient or excessive **1 score**	Lack of slides **0 points**

Criteria for assigning rating points for the quality of answers to questions during the defense of the thesis

Name of criterion	Quantity points			
	Grade 5	Grade 4	Grade 3	Grade 2
Answers on questions from commission members	Not less than 80% full answers, the remaining 20% are incomplete answers **20 points**	Not less 70% complete answers and no more than 10% of erroneous answers **16 points**	Not less 50% complete answers and no more than 30% of incorrect answers **12 points**	Less than 50% complete answers And more than 30% of incorrect answers **0 points**

3. Methodological materials defining the procedures for assessing knowledge, skills, skills And (or) experience activities, characterizing stages formations competencies

Procedure conducting this evaluative events is being carried out V in accordance with the Regulation on the implementation and protection of coursework at SKFU.

Suggested student tasks allow check professional competencies PC-2.

Time completion time – 27 hours.

For execution coursework project By discipline necessary navigate according to the deadlines and literature recommended in the individual assignment for the course project.

At verification project, the following are assessed:

— correspondence contents RPC task on KP;

— completeness And depth object analysis And subject of research;

— right And accuracy calculations With using PC;

— performance And adequacy circuit models;

— availability techniques, right And accuracy results research;

— availability justified conclusions By sections And By work V as a whole;

— correspondence RPC And GC requirements regulatory documents;

— literacy presentation And quality design report;

— volume RPC And GC without accounting reference applications. When defending a project, the following are assessed:

— correspondence contents report content KP, completeness its lighting;

— consistency, argumentation and evidence in achieving goals and solving specific design problems;

— quality And scientific nature presentations, brevity of the report;

— report time ;

— correspondence contents presentations content report And KP;

— structuredness, clarity And completeness demonstrated material;

— quality graphics, illustrations;
— quantity slides;
— quality answers on questions members commissions.