

MINISTRY OF SCIENCE AND HIGHER EDUCATION OF THE RUSSIAN FEDERATION
Federal State Autonomous Educational Institution of Higher Education
NORTH CAUCASIAN FEDERAL UNIVERSITY

I APPROVE

Dean of the Faculty of Mathematics
and computer science named after
Professor N.I. Chervyakov,
Candidate of Physical and
Mathematical Sciences, Associate
Professor
Grobova T.A.

ASSESSMENT TOOLS FUND FOR DISCIPLINE
" DIGITAL SYSTEM DESIGN / ПРОЕКТИРОВАНИЕ ЦИФРОВЫХ СИСТЕМ
"

Direction of training	02.04.01 Mathematics and Computer Science
Directionality (profile)	Training Program for Electronic Information
Year of commencement of studies	2026
Form of study	full-time
Implemented in a semester	3

Preface

1. The purpose of this course is to conduct ongoing monitoring of academic performance and midterm assessment in the discipline " **Digital System Design / Проектирование цифровых систем** "
2. FOS is an appendix to the program of the discipline " **Digital System Design / Проектирование цифровых систем** "
3. Developer: Maria Vasilievna Valueva – Associate Professor of the Department of Computational Mathematics and Cybernetics, Candidate of Technical Sciences.
4. An examination of the FOS was carried out

Members of the expert group:

Chairman:

Poddubnaya N.A. – Chairman of the Teaching and Methodological Committee of the Faculty of Mathematics and Computer Science named after Professor N.I. Chervyakov

Members of the commission:

Gladkov A.V. – member of the teaching and methodological committee of the Department of Computational Mathematics and Cybernetics;

Andrukhiv L.V. – member of the teaching and methodological committee of the Department of Mathematical Modeling;

Kopytkova L.B. – member of the teaching and methodological committee of the department of mathematical analysis, algebra and geometry.

Representative of the employer organization: Lapin V.G. – Head of the Automated Control System Department of the Stavropol Regional Clinical Consultative and Diagnostic Center.

Expert opinion: the fund of assessment tools is recommended for assessing the level of development of competencies during ongoing monitoring of academic performance and midterm assessment of students in the discipline “**Digital System Design / Проектирование цифровых систем**” .

« 15 » April 2026

5. The validity period of the FOS is determined by the period of implementation of the educational program.

1. Description of the criteria for assessing competence at various stages of its development, description of assessment scales

Competence (ii), indicator (s)	Levels of development competence (s),			
	Minimum level not achieved (unsatisfactory) 2 points	Minimum level (satisfactorily) 3 points	Average level (Fine) 4 points	High level (excellent) 5 points
PC-4. Capable of conducting patent research, determining forms and methods of legal protection and defense of rights to the results of intellectual activity, and managing rights to them to solve problems in the field of development of science, engineering and technology				
Learning outcomes for the discipline: <i>Indicator:</i> ID-1 _{PC-4} Makes rational choices regarding methods of protecting intellectual property rights; ID-2 _{PC-4} Conducts patent research in the field of computing and communication systems.	significant problems of applied and computer mathematics at a good level using methods to solve significant problems in applied and computer mathematics at a good level	significant problems of applied and computer mathematics at a good level using methods to solve significant problems in applied and computer mathematics at a good level	significant problems of applied and computer mathematics at a good level using methods to solve significant problems in applied and computer mathematics at a good level	Able to make rational choices regarding methods of protecting intellectual property rights. Conducts patent research in the field of computing and communication systems.
PC-5 Able to present and adapt mathematical knowledge, programming methods and information technology in various ways, taking into account the level of the audience				
Learning outcomes for the discipline: <i>Indicator:</i> ID-1 _{PC-5} Assesses the level of preparation of listeners during their public speeches ID-2 _{PC-5} Adapts the presentation of mathematical knowledge and programming methods to the level of the students	Unable to apply machine learning tools, models, and methods to solve professional problems	Partially able to apply machine learning tools, models, and methods to solve professional problems	Able to apply machine learning tools, models, and methods to solve professional problems at a high level	Able to effectively apply machine learning tools, models, and methods to solve professional problems

The assessment of the level of development of competence in the discipline is carried out on the basis of the "Regulations on the current monitoring of academic performance and midterm assessment of students in higher education programs - bachelor's programs , specialist programs , master's programs - at the federal state autonomous educational institution of higher education " North Caucasus Federal University" in the current version.

Set of tasks

in the discipline " Digital System Design / Проектирование цифровых систем"

Topic: Integrated Development Environments for VLSI Xilinx ISE 14.7 and Xilinx Vivado

Progress of work

1. Organizational moment (registration in the laboratory, review of safety rules for working on a computer, preparation of the workplace, launch of the Xilinx ISE 14.7 design environment)
2. Familiarization with the basic, additional, and methodological literature, as well as Internet sources, necessary for completing laboratory work.
3. Selecting a variant of the practical work assignment, registering the selected variant with the teacher.
4. Working on the project.
 - 4.1. Develop and implement a device model in VHDL using the Xilinx ISE 14.7 design environment that calculates the values of a logical function specified by a truth table (according to the variant). Synthesize the circuit.
a test simulator of the device created in task 4.1 in the Xilinx ISE 14.7 design environment .
Obtain timing diagrams of the circuit simulation.
5. Prepare a report on the laboratory work.
6. Project protection.
7. Completion of work (disabling the design environment, tidying up the workspace)

Literature

Main:

1. Mathematical Models and Synthesis Methods in Very Large-Scale Integrated Circuits: Laboratory Workshop / Ministry of Education of the Russian Federation; Federal State Autonomous Educational Institution of Higher Education "North Caucasus Federal University"; author-compiler N. I. Chervyakov; author-compiler A. I. Galushkin; author-compiler M. G. Babenko ; author - compiler V. A. Kuchukov . - Stavropol: SKFU , 2021. - 187 p. - <http://biblioclub.ru/> . - Bibliography : p.185

Additional:

1. Digital circuit design . From logic element to control system: Practical course: Field of study 09.06.01 - Computer science and computer engineering. Profile Mathematical modeling, numerical methods and software packages. Graduate qualification Researcher. Lecturer-researcher / compiled by N. I. Chervyakov, P. A. Lyakhov, A. I. Galushkin; North- Caucasian Federal University - Stavropol: SKFU, 2015. - 191 p.
2. Chervyakov, N. I. (SKFU). Digital Circuit Engineering : Textbook: Field of study 09.06.01 - Computer Science and Engineering. Profile "Mathematical Modeling, Numerical Methods and Software Packages". Graduate Qualification - Researcher. Research Lecturer / N. I. Chervyakov, A. I. Galushkin; North- Caucasian Federal University . - Stavropol: SKFU, 2015. - 198 p.

Methodical:

1. Chervyakov, N. I. (SKFU). Digital Circuit Engineering : Textbook: Field of study 09.06.01 - Computer Science and Engineering. Profile "Mathematical Modeling, Numerical Methods and Software Packages". Graduate Qualification - Researcher. Research Lecturer / N. I. Chervyakov, A. I. Galushkin; North- Caucasian Federal University . - Stavropol: SKFU, 2015. - 198 p.

Internet resources

1. Official website of Xilinx [electronic resource] / <http://www.xilinx.com>

Setting the reproductive level

Synthesize the project, implement it , create a test bench , prepare a report, possibly skipping some points (it is allowed to use ready-made IEEE library modules for binary arithmetic)

Var.	d0	d1	d2	d3	d4	d5	d6	d7	d8	d9	d10	d11	d12	d13	d14	d15
1	1	0	0	1	0	0	1	1	1	1	0	1	0	1	1	1
2	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0
3	0	1	0	1	1	1	1	1	1	1	0	0	1	0	0	1
4	1	1	0	0	1	1	1	1	0	0	1	1	1	0	1	0
5	0	0	1	1	0	0	0	1	1	0	1	0	0	1	1	1
6	1	0	0	0	1	0	0	1	0	1	0	0	1	0	1	0
7	0	1	1	0	0	1	1	0	1	0	1	1	0	1	1	0
8	0	1	0	0	1	1	1	1	0	0	0	1	0	1	1	0
9	1	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0
10	0	0	1	1	0	1	1	0	1	1	0	0	1	0	0	0
11	1	1	1	0	1	1	0	0	1	1	1	0	1	0	1	0
12	0	0	0	0	1	0	1	0	0	1	0	0	0	0	1	1
13	0	1	0	1	1	0	0	0	1	1	0	0	0	0	0	1
14	0	1	0	0	0	1	0	1	0	0	0	0	0	0	1	0
15	0	0	0	1	1	0	1	0	1	1	0	1	1	0	0	1
16	0	0	1	0	1	1	0	1	0	0	0	0	1	0	0	1
17	0	1	1	0	1	0	0	1	1	0	1	1	0	0	0	0
18	0	0	1	0	0	0	0	0	1	1	0	0	1	1	0	0
19	0	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0
20	1	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0
21	1	1	0	0	1	0	1	0	0	0	0	1	1	0	0	1
22	1	1	0	1	1	1	0	1	1	1	1	0	1	0	1	1
23	0	0	1	1	1	1	1	1	1	0	0	0	0	0	1	0
24	1	0	0	0	1	0	0	1	1	0	0	1	1	0	1	0
25	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
26	1	0	1	0	1	1	0	1	1	1	0	1	0	1	1	1
27	0	0	0	0	1	1	0	0	1	0	1	0	1	1	1	1
28	0	0	0	1	0	0	1	0	1	1	1	1	0	1	1	1
29	1	1	0	1	1	0	0	1	0	0	1	1	0	0	0	1
30	1	1	1	0	0	1	1	0	0	0	0	0	1	1	0	1

Setting the reconstructive level

Synthesize the project, implement it , create a testbench , and prepare a report, possibly skipping some steps. Using ready-made IEEE binary arithmetic library modules is prohibited; i.e., you must create your own modules for performing arithmetic operations on binary numbers.

Creative level task

Synthesize the project, implement it , create a testbench , create firmware and flash it to the FPGA, and prepare a report. If using ready-made IEEE arithmetic modules, supplement the project with your own modules for performing arithmetic operations on binary numbers.

Subject: Development of digital information processing devices

Progress of work

1. Organizational moment (registration in the laboratory, review of safety rules for working on a computer, preparation of the workplace, launch of the Xilinx ISE 14.7 design environment)
2. Familiarization with the basic, additional, and methodological literature, as well as Internet sources, necessary for completing laboratory work.
3. Selecting a laboratory assignment option, registering the selected option with the instructor.
4. Working on the project.
- 4.1. Develop and implement a finite-state machine model in VHDL using the Xilinx ISE 14.7 design environment. This machine performs digital processing of a one-dimensional input signal using specified filter coefficients (as per the design option). Specify the filter termination signal sequence yourself. Synthesize the circuit. The input and output signal width is 32 bits. a test simulator of the device created in task 4.1 in the Xilinx ISE 14.7 design environment . Obtain timing diagrams of the circuit simulation.
5. Prepare a report on the laboratory work.
6. Project protection.
7. Completion of work (disabling the design environment, tidying up the workspace)

Literature

Main:

1. Mathematical Models and Synthesis Methods in Very Large-Scale Integrated Circuits: Laboratory Workshop / Ministry of Education of the Russian Federation; Federal State Autonomous Educational Institution of Higher Education "North Caucasus Federal University"; author-compiler N. I. Chervyakov; author-compiler A. I. Galushkin; author-compiler M. G. Babenko ; author - compiler V. A. Kuchukov . - Stavropol: SKFU , 2021. - 187 p. - <http://biblioclub.ru/> . - Bibliography : p.185

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2. Chervyakov, N. I. (SKFU). Digital Circuit Engineering : Textbook: Field of study 09.06.01 - Computer Science and Engineering. Profile "Mathematical Modeling, Numerical Methods and Software Packages". Graduate Qualification - Researcher. Research Lecturer / N. I. Chervyakov, A. I. Galushkin; North- Caucasian Federal University . - Stavropol: SKFU, 2015. - 198 p.

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Internet resources

1. Official website of Xilinx [electronic resource] / <http://www.xilinx.com>

Setting the reproductive level

Synthesize the project, implement it , create a test bench , prepare a report, possibly skipping some points.

Var.	I know	k1	k2	k3	k4	k5	k6	k7	k8
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	.								
1	3	6	0	-14	-14	-15	14	-10	-6
2	13	7	1	14	-11	8	-4	7	-9
3	14	8	-11	-2	7	-3	-6	-13	2
4	5	-5	-1	7	4	-14	-3	7	3
5	6	-4	4	4	-13	11	6	-4	10
6	8	6	7	5	-15	5	13	14	-1
7	2	-1	13	6	15	10	7	3	15
8	1	5	-13	7	8	14	-6	-15	5
9	14	-5	14	14	6	-5	-2	-3	-8
10	13	-8	0	7	-5	8	13	6	6
11	4	8	15	5	8	-6	12	7	15
12	5	-8	-3	-6	12	-8	-7	-12	-2
13	15	-14	15	-9	-12	-15	-10	-14	7
14	11	5	-2	9	0	-15	-10	1	1
15	6	10	3	7	14	10	2	0	-8
16	15	-9	-5	13	8	2	6	11	-9
17	9	-15	5	4	9	2	7	-12	-1
18	10	13	6	4	-13	6	-11	-5	1
19	6	-1	-7	-11	-11	-14	-11	13	11
20	4	-14	-9	15	8	0	1	5	-3
21	6	-1	-9	12	-12	11	4	-8	4
22	1	-2	-2	7	-1	-10	-8	-3	2
23	3	-3	-4	5	-5	4	9	-10	1
24	1	-7	-8	11	-6	-15	-10	-3	6
25	14	12	3	0	-4	0	-4	-11	-10
26	16	1	14	5	1	-11	1	-4	11
27	8	-1	-15	-8	-11	0	-3	2	2
28	5	14	-9	12	-7	4	12	13	-15
29	3	3	3	-8	-12	15	14	3	-8
30	7	7	-3	-12	-6	2	10	-12	-2

Setting the reconstructive level

Synthesize the project, implement it , create a testbench , and prepare a report, possibly skipping some steps. Using third-party libraries of binary arithmetic modules for the residual class system is prohibited; i.e., you must create your own modules for performing arithmetic operations.

Creative level task

Synthesize the project, implement it , create a testbench , create firmware and flash it to the FPGA, and prepare a report. If using ready-made binary arithmetic modules, supplement the project with your own modules for performing arithmetic operations.

Requirements for the completion of Practical Work

The laboratory work is considered completed by the student and is credited by the teacher (with points awarded proportionally to the completed points of the report, i.e. it is not necessary for the report to contain all the points) upon submission of a neatly formatted report file in . odt (OpenOffice , LibreOffice) or . doc (Microsoft) format in electronic form for defense (a paper printout is not required!!!) Office), named according to a template (if there is a discrepancy, the work is not allowed to be protected):

DSCH _ LR (work number)_V(variant number)_(surname). odt

The report file must contain the following elements in the specified order (with their numbers preserved if some items are omitted):

0. A mark on familiarization with safety precautions (rules of conduct in the computer lab (auditorium, laboratory)).

This section must include the entry “I have read and agree to comply with the safety regulations for performing laboratory work and behavior in the computer lab (classroom, laboratory) _____ (full name), _____ date.”

1. Statement of the problem (full conditions in accordance with the selected option).

2. A detailed mathematical (set of formulas and explanatory text) or informational (verbal description of the algorithm) model of the problem solution. Screenshots of calculations in computer algebra systems (SciLab , Octave , Maxima , etc.) are acceptable for this section. The use of proprietary (commercial) computer algebra systems (MathCad , MatLab , etc.) is not recommended.

3. Test sets of initial data and corresponding correct results to verify the program's functionality (this section **should include a manual solution to the problem with intermediate calculations**). Screenshots of calculations in computer algebra systems (SciLab , Octave , Maxima , etc.) are acceptable for this section. The use of proprietary (commercial) computer algebra systems (MathCad , MatLab , etc.) is not recommended.

4. Specifying the names, types and purposes of all variables and signals included in the mathematical or information model.

5. The main and auxiliary (if any) algorithms for solving the problem (a description of the algorithm in an algorithmic language, for example, Pascal , is acceptable).

6. Record the full names of the files that make up the project, indicating the purpose of each file (at a minimum, indicate the names and contents of files with the .vhd extension (what entities , procedures , functions they contain, what they do).

7. Complete source code of the project's VHDL programs (each file must contain information about the developer - full name, year, group, specialty, university).

8. RTL diagram of the project (from the Synthesize -XST section of the design environment).

9. Contents of the .syr file of the project synthesis and implementation report.

10. Power consumption of the circuit in Watts (contents of XPower tables Design Environment Analyzer).

11. A screenshot or printout of the computer program's output using the entered test data from section 3 of the report. Specifically, in this section, you must compare the obtained results with the reference test solution and write "result matches reference solution."

12. Study of the model.

In this section, you need to write down several sets of input data (define them yourself) and the corresponding modeling results (if in section 11 a complete enumeration of all possible input data was carried out, then write “matches section 11 of the report”).

13. Conclusions on the work done.

Specify the capabilities, advantages, and disadvantages of the model, and provide examples of use.

Exam questions

in the discipline: " Digital System Design / Проектирование цифровых систем"

Questions (task, assignment) to test the level of learning

Know

1. Classification of modern electronic circuits
2. Overview of Basic Microelectronics Circuits
3. Gates "not", "buffer", "and", "or", "exclusive or", "and-not", "or-not"
4. Multiplexers
5. Demultiplexers
6. Encryptors
7. Decoders
8. Triggers
9. Registers
10. Counters
11. Synthesis of universal combinational circuits based on multiplexers
12. Synthesis of universal combinational circuits based on encoders and decoders
13. Synchronous and asynchronous circuits.
14. Mealy finite state machine
15. Moore's finite state machine
16. Xilinx ISE 14.7 Ultra-Large-Scale Integrated Circuits (VLSI) Development Environment
17. Circuit simulation
18. Implementation of the scheme
19. Flashing the circuit into FPGA
20. Specifics of the hardware description language
21. VHDL Project Structure
22. VHDL data types
23. Sequential and parallel processes in VHDL
24. Implementation of branching constructs in VHDL
25. Implementation of cyclic constructs in VHDL
26. Parameterized modules in VHDL
27. Signal attributes in VHDL
28. Modular design in VHDL
29. Addition and subtraction of binary numbers
30. Multiplication of binary numbers
31. Division of binary numbers
32. Comparison of binary numbers
33. Coding negative numbers in the binary number system
34. Representation of rational numbers in the binary number system
35. Modular arithmetic
36. Digital filters
37. Direct discrete Fourier transform
38. Inverse discrete Fourier transform
39. Optimizing the power consumption of the circuit
40. High-speed circuit synthesis

Be able to

1. Using a computer with installed software, implement a circuit for a binary adder of arbitrary bit depth.
2. Using a computer with installed software, implement a binary subtractor circuit of arbitrary bit depth.
3. Using a computer with installed software, implement a circuit for a binary

multiplier of arbitrary bit depth.

4. Using a computer with installed software, implement a binary divider circuit with a remainder of arbitrary bit depth.

5. Using a computer with installed software, implement a circuit of a binary comparator of arbitrary bit capacity.

6. Using a computer with installed software, implement the adder circuit for pre-set bases.

a subtractor ROC circuit for pre-set bases.

multiplier circuit for pre-set bases.

9. Using a computer with installed software, implement a comparator SOC circuit for pre-set bases.

10. Using a computer with installed software, implement a division scheme for numbers in the RNS for a predetermined set of bases

11. Using a computer with installed software, implement a SOC-PSS translation scheme based on the Chinese remainder theorem.

12. Using a computer with installed software, implement a scheme for transferring the SOC-PSS based on the OPSS.

13. Using a computer with installed software, implement the PSS-SOK translation scheme for a predetermined set of bases.

14. Using a computer with installed software, implement a filtering circuit for a one-dimensional signal

15. Using a computer with installed software, implement a filtering scheme for a two-dimensional image

16. Using a computer with installed software, implement a direct Fourier transform circuit

17. Using a computer with installed software, implement the inverse Fourier transform circuit

18. Using a computer with installed software, implement the Mealy finite state machine circuit.

19. Using a computer with installed software, implement the Moore finite state machine circuit.

20. Using a computer with installed software, implement a scheme for generating pseudo-random binary numbers of arbitrary bit depth.

To own

1. Methods of creation and synthesis of very large-scale integrated circuits

Evaluation criteria

in the discipline: " Digital System Design / Проектирование цифровых систем"

The grade " *excellent* " is given to a student if:

He flawlessly presented the exam's theoretical material without the instructor's probing questions, solved the assigned problem, and developed an algorithm in high-level language. There may have been one or two inaccuracies in the explanation of minor issues or calculations, which the student easily corrected after the instructor's comments.

a grade of " *good* " if:

He demonstrated the systematic nature of his knowledge in the discipline and the ability to independently replenish and update it in the course of further academic work and professional activity; if one or two shortcomings were made in the presentation of the main content of the answer and the coverage of secondary issues or calculations, they were easily corrected after the teacher's comments.

The grade " *satisfactory* " is given to a student if:

he made mistakes in his answers to the exam and in completing the exam assignments, did not formulate the main provisions of the program material correctly enough, violated the sequence in its presentation, demonstrated insufficient development of the basic skills and abilities when completing the practical assignment, but possessed the necessary knowledge to correct them under the guidance of the teacher

The grade " *unsatisfactory* " is given to the student,

who discovered gaps in knowledge of the basic educational program material and made fundamental mistakes in fulfilling the practical knowledge provided by the program

Topics of abstracts

in the discipline: " Digital System Design / Проектирование цифровых систем"

1. Classification of modern electronic circuits
2. Overview of Basic Microelectronics Circuits
3. Gates "not", "buffer", "and", "or", "exclusive or", "and-not", "or-not"
4. Multiplexers and demultiplexers
5. Encryptors and decoders
6. Triggers, registers and counters
7. Synthesis of universal combinational circuits based on multiplexers
8. Synthesis of universal combinational circuits based on encoders and decoders
9. Synchronous and asynchronous circuits.
10. Mealy finite state machine
11. Moore's finite state machine
12. Xilinx ISE 14.7 Integrated Development Environment
13. Circuit simulation, circuit implementation, circuit firmware in Xilinx FPGA
14. Specifics of the VHDL hardware description language
15. Project structure and modular design in VHDL
16. Sequential and parallel processes in VHDL
17. Implementation of branching constructs in VHDL
18. Implementation of cyclic constructs in VHDL
19. Parameterized modules in VHDL
20. Data types and signal attributes in VHDL
21. Addition and subtraction of binary numbers
22. Multiplication of binary numbers
23. Division of binary numbers
24. Comparison of binary numbers
25. Coding negative numbers in the binary number system
26. Representation of rational numbers in the binary number system
27. Modular arithmetic
28. Problematic operations of modular arithmetic
29. Optimizing the power consumption of the circuit
30. High-speed circuit synthesis