

MINISTRY OF SCIENCE AND HIGHER EDUCATION OF THE RUSSIAN FEDERATION  
Federal State Autonomous Educational Institution  
higher education  
NORTH CAUCASIAN FEDERAL UNIVERSITY

**I APPROVE**

Dean of the Faculty of Mathematics  
and computer science named after  
Professor N.I. Chervyakov,  
Candidate of Physical and  
Mathematical Sciences, Associate  
Professor  
Grobova T.A.

**ASSESSMENT TOOLS FUND**

by discipline

Innovative Training Practice Course (Mathematical Modeling) / Инновационный курс  
практического обучения (математическое моделирование)

|                                 |                                             |
|---------------------------------|---------------------------------------------|
| Direction of training           | 02.04.01 Mathematics and Computer Science   |
| Directionality (profile)        | Training Program for Electronic Information |
| Year of commencement of studies | 2026                                        |
| Form of study                   | full-time                                   |
| It is implemented in semesters  | 2                                           |

## Introduction

### 1. Purpose

The assessment tools fund is intended for ongoing monitoring of academic performance and midterm assessment in the discipline "Innovative Training Practice Course (Mathematical Modeling) / Инновационный курс практического обучения (математическое моделирование)" for full-time students majoring in 02.04.01 Mathematics and computer science.

2. The FOS is an appendix to the program of the discipline "Innovative Training Practice Course (Mathematical Modeling) / Инновационный курс практического обучения (математическое моделирование)".

3. Developer: Ionisyan A.S., Candidate of Physical and Mathematical Sciences, Associate Professor of the Department of Mathematical Modeling.

4. An examination of the organophosphorus compounds was carried out.  
Members of the expert group:

Chairman:

Poddubnaya N.A. – Chairman of the Teaching and Methodological Committee of the Faculty of Mathematics and Computer Science named after Professor N.I. Chervyakov

Members of the commission:

Gladkov A.V. – member of the teaching and methodological committee of the Department of Computational Mathematics and Cybernetics;

Andrukhiv L.V. – member of the teaching and methodological committee of the Department of Mathematical Modeling;

Kopytkova L.B. – member of the teaching and methodological committee of the department of mathematical analysis, algebra and geometry.

Representative of the employer organization: Lapin V.G. – Head of the Automated Control System Department of the Stavropol Regional Clinical Consultative and Diagnostic Center.

Expert opinion: The FOS for the discipline "Innovative Training Practice Course (Mathematical Modeling) / Инновационный курс практического обучения (математическое моделирование)" allows for assessing the level of development of competencies. Recommended for use in the educational process.

April 15 , 2026

5. The validity period of the FOS is determined by the period of implementation of the educational program.

## 1. Description of the criteria for assessing competence at various stages of its development, description of assessment scales

| Competence(s),<br>indicator(s)                                                                                                                                                                                                                                                                                                                                                                                                                | Levels of development of competencies                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                               | The minimum level has not been reached (Unsatisfactory)<br>2 points                                                                                                                                                                                                                                                                                                                                                                                                | Minimum level (satisfactorily)<br>3 points                                                                                                                                                                                                                                                                                                                                                                | Intermediate level (Fine)<br>4 points                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | High level (excellent)<br>5 points                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| <b>Competence: UK-1</b><br>Able to carry out a critical analysis of problematic situations based on a systems approach and develop an action strategy                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ID-1 <small>UK-1</small> Selects information resources for searching for information in accordance with the assigned educational task.<br>ID-2 <small>UK-1</small> Systematizes information obtained from various sources in accordance with the requirements for completing the educational assignment.<br>ID-3 <small>UK-1</small> Formulates and argues conclusions and judgments, including using the philosophical conceptual apparatus. | does not know the classification of modern logic circuits, basic logic circuits of microelectronics,<br>Synchronous and asynchronous circuits, Mealy state machine, Moore state machine, Addition and subtraction of binary numbers, Multiplication of binary numbers, Division of binary numbers, Comparison of binary numbers, Encoding of negative numbers in the binary number system, Representation of rational numbers in the binary number system, Modular | has a satisfactory knowledge of the classification of modern logic circuits, basic logic circuits of microelectronics, Synchronous and asynchronous circuits, Mealy state machine, Moore state machine, Addition and subtraction of binary numbers, Multiplication of binary numbers, Division of binary numbers, Comparison of binary numbers, Encoding of negative numbers in the binary number system, | has a good knowledge of the classification of modern logic circuits, basic logic circuits of microelectronics, Synchronous and asynchronous circuits, Mealy state machine, Moore state machine, Addition and subtraction of binary numbers, Multiplication of binary numbers, Division of binary numbers, Comparison of binary numbers, Encoding of negative numbers in the binary number system, Representation of rational numbers in the binary number system, Modular arithmetic, Digital filters . | has excellent knowledge of the classification of modern logic circuits, basic logic circuits of microelectronics, Synchronous and asynchronous circuits, Mealy state machine, Moore state machine, Addition and subtraction of binary numbers, Multiplication of binary numbers, Division of binary numbers, Comparison of binary numbers, Encoding of negative numbers in the binary number system, Representation of rational numbers in the binary number system, Modular arithmetic, Digital filters. |

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|                                                                                                                                                                                                                                                              | arithmetic,<br>Digital filters.                                                                                                                                                                                                              | Representatio<br>n of rational<br>numbers in<br>the binary<br>number<br>system,<br>Modular<br>arithmetic,<br>Digital<br>filters.                                                                                                                    |                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                              |
| <b>Competence: PC-1</b><br>Able to demonstrate fundamental knowledge of mathematics and natural sciences, programming and information technology.                                                                                                            |                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                              |
| ID-1 <sub>PC-1</sub><br>In his professional activities, he demonstrates fundamental knowledge of mathematics and natural sciences.<br>ID-2 <sub>PC-1</sub> Solves problems of professional activity using programming and information technology tools       | is also unable to use modern methods of data processing in the field of information technology for the synthesis of universal combinational circuits based on multiplexers, universal combinational circuits based on encoders and decoders, | is able to satisfactorily use modern methods of data processing in the field of information technology for the synthesis of universal combinational circuits based on multiplexers, universal combinational circuits based on encoders and decoders | is proficient in using modern methods of data processing in the field of information technology to synthesize universal combinational circuits based on multiplexers, universal combinational circuits based on encoders and decoders | He is highly skilled in using modern methods of data processing in the field of information technology to synthesize universal combinational circuits based on multiplexers, universal combinational circuits based on encoders and decoders |
| <b>Competence: PC-2</b><br>Able to conduct scientific research based on existing methods in a specific area of professional activity                                                                                                                         |                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                              |
| ID-1 <sub>PC-2</sub><br>Conducts scientific research in the field of parallel computer technologies.<br>ID-2 <sub>PC-2</sub><br>Conducts reviews of scientific articles, abstracts and dissertations in the fields of mathematics and information technology | does not know Xilinx ISE 14.7, Circuit Simulation, Circuit Implementation, FPGA Circuit Flashing, Hardware Description Language Specifics, VHDL Project Structure, VHDL Data                                                                 | has satisfactory knowledge of the integrated development environment for very large-scale integrated circuits Xilinx ISE 14.7, circuit simulation, circuit                                                                                          | Has good knowledge of the Xilinx ISE 14.7 integrated development environment for very large-scale integrated circuits, circuit simulation, circuit implementation, circuit firmware in FPGA,                                          | Excellent knowledge of the Xilinx ISE 14.7 integrated development environment for very large-scale integrated circuits, circuit simulation, circuit implementation, circuit firmware in FPGA,                                                |

|                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                             |
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|                                                                                                                                                                                                                                                        | Types, Sequential and Parallel Processes in VHDL, Implementation of Branching Constructs in VHDL, Implementation of Cyclic Constructs in VHDL, Parameterized Modules in VHDL, Signal Attributes in VHDL, Modular Design in VHDL. | implementation, circuit firmware in FPGA, hardware description language specifics, VHDL project structure, VHDL data types, sequential and parallel processes in VHDL, implementation of branching constructs in VHDL, implementation of cyclic constructs in VHDL, parameterized modules in VHDL, signal attributes in VHDL, modular design in VHDL. | hardware description language specifics, VHDL project structure, VHDL data types, sequential and parallel processes in VHDL, implementation of branching constructs in VHDL, implementation of cyclic constructs in VHDL, parameterized modules in VHDL, signal attributes in VHDL, modular design in VHDL. | hardware description language specifics, VHDL project structure, VHDL data types, sequential and parallel processes in VHDL, implementation of branching constructs in VHDL, implementation of cyclic constructs in VHDL, parameterized modules in VHDL, signal attributes in VHDL, modular design in VHDL. |
| <b>Competence: PC-3</b><br>Capable of conducting methodological and expert work in the field of mathematics and computer science                                                                                                                       |                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                             |
| ID-1 <sub>PC-3</sub><br>Conducts expert work in mathematics.<br>ID-2 <sub>PC-3</sub><br>Conducts expert work in the field of computer science<br>ID-2 <sub>PC-3</sub><br>Prepares teaching materials in the fields of mathematics and computer science | does not know how to develop software and information support for computer systems, services, computing complexes, databases for the synthesis of very large-scale integrated circuits                                           | has satisfactory skills in developing software and information support for computer systems, services, computing complexes, and databases for the                                                                                                                                                                                                     | is proficient in developing software and information support for computer systems, services, computing complexes, and databases for the synthesis of very large-scale integrated circuits                                                                                                                   | is excellent at developing software and information support for computer systems, services, computing complexes, and databases for the synthesis of very large-scale integrated circuits                                                                                                                    |

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|  |  | synthesis of<br>very large-<br>scale<br>integrated<br>circuits |  |  |
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The assessment of the level of development of competence in the discipline is carried out on the basis of the “Regulations on the current monitoring of academic performance and midterm assessment of students in higher education programs - bachelor's programs, specialist programs, master's programs - at the federal state autonomous educational institution of higher education "North Caucasus Federal University" in the current version.

### ASSESSMENT TOOLS FOR CHECKING THE LEVEL OF DEVELOPMENT OF COMPETENCIES

| Task number | Correct answer                                                                                                                             | Contents of the question                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Competence                   |
|-------------|--------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
|             |                                                                                                                                            | <b>Form of study - full-time, Semester - 2</b>                                                                                                                                                                                                                                                                                                                                                                                                                                               |                              |
| 1.          | high and low voltage levels                                                                                                                | Binary numbers in computers are usually represented<br>"high and low voltage levels"<br>"voltages of opposite polarity"<br>_____ (type the correct version without quotation marks)                                                                                                                                                                                                                                                                                                          | UK-1<br>PC-1<br>PC-2<br>PC-3 |
| 2.          | This is a well-optimized operation built into most microprocessors.                                                                        | Addition of binary numbers<br>"It is a well-optimized operation built into most microprocessors."<br>"This operation is well optimized, but due to the high consumption of gates on simple microprocessors and microcontrollers, it is not implemented at the hardware level."<br>"This operation is built only into complex arithmetic logic units of computers due to its insufficient optimization at the hardware level."<br>_____ (type the correct version without quotation marks)    | UK-1<br>PC-1<br>PC-2<br>PC-3 |
| 3.          | This is a well-optimized operation built into most microprocessors.                                                                        | Subtraction of binary numbers<br>"It is a well-optimized operation built into most microprocessors."<br>"This operation is well optimized, but due to the high consumption of gates on simple microprocessors and microcontrollers, it is not implemented at the hardware level."<br>"This operation is built only into complex arithmetic logic units of computers due to its insufficient optimization at the hardware level."<br>_____ (type the correct version without quotation marks) | UK-1<br>PC-1<br>PC-2<br>PC-3 |
| 4.          | This operation is built only into complex arithmetic logic devices of computers due to its insufficient optimization at the hardware level | Division of binary numbers<br>"It is a well-optimized operation built into most microprocessors."<br>"This operation is well optimized, but due to the high consumption of gates on simple microprocessors and microcontrollers, it is not implemented at the hardware level."<br>"This operation is built only into complex arithmetic logic units of computers due to its insufficient optimization at the hardware level."<br>_____ (type the correct version without quotation marks)    | PC-3                         |
| 5.          | can be accomplished with additional code                                                                                                   | Coding negative numbers in the binary number system<br>"can be accomplished with additional code"<br>"can be done by indirect code"                                                                                                                                                                                                                                                                                                                                                          | PC-5                         |

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|    |                                                                                                                                                                                                                                                        | can be performed by direct code                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |      |
| 6. | This is binary logic, the result of which depends only on the state of the inputs.                                                                                                                                                                     | <p>What is a combinational circuit?</p> <p>"This is binary logic, the result of which depends only on the state of the inputs."</p> <p>"This is binary logic, the result of which depends not only on the state of the inputs, but also on the operating history of the digital device."</p> <p>_____ (type the correct version without quotation marks)</p>                                                                                                                                                                                                                                                                                                             | PC-5 |
| 7. | de Morgan basis                                                                                                                                                                                                                                        | <p>The combination of AND, OR, NOT elements is also called</p> <p>"de Morgan basis"</p> <p>Schaeffer's stroke</p> <p>Pierce's arrow</p> <p>_____ (type the correct version without quotation marks)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | PC-5 |
| 8. | A device with multiple signal inputs, one or more control inputs, and one output. It allows a signal from one of the inputs to be transmitted to the output. The desired input is selected by applying the appropriate combination of control signals. | <p>Multiplexer is</p> <p>A device with multiple signal inputs, one or more control inputs, and one output. It allows a signal from one of the inputs to be transmitted to the output. Selection of the desired input is accomplished by applying the appropriate combination of control signals.</p> <p>"A logical device designed to switch a signal from one information input to one of the information outputs"</p> <p>"A logic unit that converts a positional n-bit code into an m-bit code"</p> <p>"A combinational circuit that converts an n-bit binary code into a k-ary single-unit code"</p> <p>_____ (type the correct version without quotation marks)</p> | PC-5 |
| 9. | A logic unit that converts a positional n-bit code into an m-bit code                                                                                                                                                                                  | <p>The encoder is</p> <p>A device with multiple signal inputs, one or more control inputs, and one output. It allows a signal from one of the inputs to be transmitted to the output. Selection of the desired input is accomplished by applying the appropriate combination of control signals.</p> <p>"A logical device designed to switch a signal from one information input to one of the information outputs"</p> <p>"A logic unit that converts a positional n-bit code into an m-bit code"</p> <p>"A combinational circuit that converts an n-bit binary code into a k-ary single-unit code"</p>                                                                 | PC-5 |

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|     |                                                                                                   | _____ (type the correct version without quotation marks)                                                                                                                                                                                                                                                                                                     |      |
| 10. | VERILOG                                                                                           | Select hardware description languages<br>"VERILOG"<br>PASCAL<br>BASIC<br>_____ (type the correct version without quotation marks)                                                                                                                                                                                                                            | PC-5 |
| 11. | ENTITY and<br>ARCHITECTURE<br>blocks                                                              | A simple VHDL program contains<br>ENTITY and ARCHITECTURE blocks<br>"the main function and auxiliary subroutine functions"<br>"language statements can appear in any order and are not required to have an explicit<br>entry point function"<br>_____ (type the correct version without quotation marks)                                                     | PC-5 |
| 12. | the most common typical<br>descriptions of signals,<br>functions and operations<br>on them        | The IEEE VHDL library contains<br>"the most frequently encountered typical descriptions of signals, functions, and<br>operations on them"<br>"the most common descriptions of signals and operations on them""device-specific<br>FPGA descriptions of signals, functions and operations on them"<br>_____ (type the correct version without quotation marks) | PC-3 |
| 13. | This is a built-in VHDL<br>Boolean type that<br>contains only the binary<br>logic values 0 and 1. | BIT data type of VHDL language.<br>"It is a universal logical type that describes all possible real-world values of binary<br>logic."<br>"This is a built-in VHDL Boolean type that contains only the binary logic values 0 and<br>1."<br>_____ (type the correct version without quotation marks)                                                           | PC-3 |
| 14. | describes a special<br>physical type of electrical<br>impulse data                                | The SIGNAL keyword in VHDL.<br>"describes a special physical type of electrical impulse data"<br>"describes a special logical data type of electrical impulses"<br>_____ (type the correct version without quotation marks)                                                                                                                                  | PC-3 |
| 15. | NOT                                                                                               | The "INV" component in VHDL stands for operation<br>"NOT"<br>"AND"<br>"OR"<br>"EXCLUSIVE OR"                                                                                                                                                                                                                                                                 | PC-5 |

|     |                                                                       |                                                                                                                                                                                                                                                                                                      |      |
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|     |                                                                       | AND-NOT<br>"OR-NOT"<br>_____ (type the correct version without quotation marks)                                                                                                                                                                                                                      |      |
| 16. | EXCLUSIVE OR                                                          | The component " XOR 2" in VHDL stands for operation<br>"NOT"<br>"AND"<br>"OR"<br>"EXCLUSIVE OR"<br>AND-NOT<br>"OR-NOT"<br>_____ (type the correct version without quotation marks)                                                                                                                   | PC-3 |
| 17. | Assigns a specific state to a signal                                  | The VHDL Plug <= operator<br>"Assigns a specific state to a signal"<br>"Assigns a specific state to a variable"<br>"Assigns a specific state to a process"<br>_____ (type the correct version without quotation marks)                                                                               | PC-3 |
| 18. | EXCLUSIVE OR                                                          | The " XOR " operator in VHDL means operation<br>"NOT"<br>"AND"<br>"OR"<br>"EXCLUSIVE OR"<br>AND-NOT<br>"OR-NOT"<br>_____ (type the correct version without quotation marks)                                                                                                                          | PC-5 |
| 19. | Allows you to create projects for SPARTAN 3rd generation FPGA devices | The XILINX ISE 14.7 design environment allows<br>Create projects for all SPARTAN 3rd generation FPGA devices<br>Create projects for all SPARTAN 7th-generation FPGA devices<br>Create designs for all VIRTEX 8th-generation FPGA devices<br>_____ (type the correct version without quotation marks) | PC-5 |
| 20. | Located in the SYNTHESIZE section                                     | Synthesis of a circuit in XILINX ISE 14.7 environment from a ready-made VHDL file.<br>"Located in the SYNTHESIZE section"<br>"Located in the IMPLEMENT DESIGN section"<br>"Located in the GENERATE section PROGRAMMING FILE »                                                                        | PC-5 |

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|     |                                                                                                                                                                                    | _____ (type the correct version without quotation marks)                                                                                                                                                                                                                                                                                                                                                                                                                           |      |
| 21. | It is designed to test the operation of the device before its actual firmware is installed in the FPGA.                                                                            | Simulation of the circuit in XILINX ISE 14.7 environment.<br>"It is designed to test the operation of the device before it is actually flashed into the FPGA."<br>"It is designed to test the operation of the device after its actual firmware is flashed into the FPGA."<br>_____ (type the correct version without quotation marks)                                                                                                                                             | PC-5 |
| 22. | It is implemented inside the BEGIN ... END block of the ARCHITECTURE section                                                                                                       | Schema initialization section in Testbench<br>"Implemented in the descriptive part of the ARCHITECTURE section"<br>"Implemented within the BEGIN ... END block of the ARCHITECTURE section"<br>_____ (type the correct version without quotation marks)                                                                                                                                                                                                                            | PC-5 |
| 23. | Allows you to see the states of signals in the circuit being debugged at any simulated point in time.                                                                              | Timing diagram of circuit signals in the ISIM simulator<br>"Allows you to see the signal states in the circuit you are debugging at any simulated point in time."<br>"Allows you to see the signal states in the circuit being debugged at any point during debugging after flashing to the FPGA."<br>_____ (type the correct version without quotation marks)                                                                                                                     | PC-3 |
| 24. | This is a trigger that remembers the state of the input and outputs it.                                                                                                            | D-trigger.<br>"This is an asynchronous trigger that maintains its previous state when both inputs are inactive and changes its state when an active level is applied to one of its inputs."<br>"This is a trigger that remembers the state of the input and outputs it."<br>"This is a trigger that changes its logical state to the opposite at each clock cycle at input C."<br>_____ (type the correct version without quotation marks)                                         | PC-3 |
| 25. | Changes its state immediately at the moment the corresponding information signal appears, with some delay equal to the sum of the delays on the elements that make up this trigger | Asynchronous trigger.<br>"It changes its state immediately at the moment the corresponding information signal appears, with some delay equal to the sum of the delays on the elements that make up the given trigger."<br>"It changes its state only at a specific transition of the clock signal. If the signal level at the clock input remains constant, no changes at the data inputs affect the trigger's state."<br>_____ (type the correct version without quotation marks) | PC-3 |

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| 26. | It is a device for writing, storing and reading n-bit binary data and performing other operations on them.                                                                                                                    | Register<br>"This is a device for writing, storing and reading n-bit binary data and performing other operations on it."<br>"This is a device whose outputs produce a binary or binary-decimal code determined by the number of incoming pulses."<br>_____ (type the correct version without quotation marks)                                                                                                                         | PC-3 |
| 27. | This is a device whose outputs produce a binary or binary-coded decimal code determined by the number of incoming pulses.                                                                                                     | Counter<br>"This is a device for writing, storing and reading n-bit binary data and performing other operations on it."<br>"This is a device whose outputs produce a binary or binary-coded decimal code determined by the number of incoming pulses."<br>_____ (type the correct version without quotation marks)                                                                                                                    | PC-5 |
| 28. | This is a ring counter in which one of the connections between the triggers is made cross-connected, i.e. the input of one of the triggers is connected not to the direct, but to the inverse output of the previous trigger. | Johnson counter.<br>"These are closed-loop shift registers whose trigger states are changed by input shift pulses."<br>"This is a ring counter in which one of the connections between the triggers is made cross-connected, i.e. the input of one of the triggers is connected not to the direct, but to the inverse output of the previous trigger."<br>_____ (type the correct version without quotation marks)                    | PC-3 |
| 29. | combinational logic circuit, calculating the sum of two bits without taking into account the input carry                                                                                                                      | Half adder is<br>"combinational logic circuit that calculates the sum of two bits without taking into account the input carry"<br>"combinational logic circuit that calculates the sum of two bits without taking into account the output carry"<br>"a combinational logic circuit that calculates the sum of two bits, taking into account the input and output carries"<br>_____ (type the correct version without quotation marks) | PC-3 |
| 30. | It is a multi-bit adder consisting of several single-bit full adders                                                                                                                                                          | Carry-propagating or successive carry adder<br>"It is a multi-bit adder consisting of several single-bit full adders connected in a chain."<br>"This is a circuit designed to generate carry bits in parallel when adding binary                                                                                                                                                                                                      | PC-5 |

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|     | connected in a chain.                                                                               | numbers in an adder."<br>_____ (type the correct version without quotation marks)                                                                                                                                                                                                                                                                                       |      |
| 31. | combinational logic circuit for finding the larger of two binary numbers                            | The magnitude check comparator is<br>"combinational logic circuit for finding the larger of two binary numbers"<br>Combinational logic circuit, binary equality checks<br>_____ (type the correct version without quotation marks)                                                                                                                                      | PC-5 |
| 32. | is considered a slow algorithm for multiplying numbers                                              | Algorithm for multiplying numbers in a column<br>"is considered a fast algorithm for multiplying numbers"<br>"is considered a slow algorithm for multiplying numbers"<br>_____ (type the correct version without quotation marks)                                                                                                                                       | PC-5 |
| 33. | is considered a slow algorithm for dividing numbers                                                 | The "corner" binary division algorithm<br>"is considered a fast algorithm for dividing numbers"<br>"is considered a slow algorithm for dividing numbers"<br>_____ (type the correct version without quotation marks)                                                                                                                                                    | PC-5 |
| 34. | Karatsuba's algorithm                                                                               | Algorithm for multiplying binary numbers<br>Karatsuba's Algorithm<br>Algorithm with successive carry<br>"Algorithm in a Corner"<br>_____ (type the correct version without quotation marks)                                                                                                                                                                             | PC-5 |
| 35. | In addition to the data types of conventional programming languages, physical types have been added | VHDL data types<br>"They are no different from the data types of conventional programming languages."<br>"In addition to the data types of conventional programming languages, physical types have been added."<br>"They have nothing in common with the data types of conventional programming languages."<br>_____ (type the correct version without quotation marks) | PC-5 |
| 36. | They are performed in a strictly defined order                                                      | Sequential operators of the VHDL language<br>"All are performed simultaneously"<br>"They are performed in a strictly defined order."<br>_____ (type the correct version without quotation marks)                                                                                                                                                                        | PC-5 |
| 37. | It is a processor unit that, under the control of a control unit, serves to                         | Arithmetic logic unit of a microprocessor<br>"It is a unit of the processor which, under the control of the control unit, serves to perform arithmetic and logical transformations on data called operands."                                                                                                                                                            | PC-3 |

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|  | perform arithmetic and logical transformations on data called operands. | "This is a section of high-speed memory of a microprocessor for storing several operands."<br>_____ (type the correct version without quotation marks) |  |
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### **Competency assessment criteria \***

**"excellent"** grade is awarded to a student who demonstrates a deep and comprehensive *knowledge* of the subject, presents the material in a coherent and logical manner, *is able to* accurately and logically justify a point of view, and *has a confident* command of methodological concepts and accepted symbols.

**"good"** grade is given to a student if he demonstrates a solid *knowledge* of the subject and presents the material in a reasoned manner;

*knows how* to apply knowledge to analyze specific situations, but at the same time slightly violates the sequence of presentation of the material, provides an insufficiently complete, although correct, definition of concepts;

*has a command* of basic methodological concepts and symbols.

**"satisfactory"** grade is given to a student if he or she *knows* the subject in general, but presents the program material fragmentarily and inconsistently;

*knows how* to apply his knowledge in practice, allows for individual mistakes and errors when solving problems;

a poor *command* of basic mathematical concepts and the use of mathematical symbols.

The grade **"unsatisfactory"** is given to a student if he has not sufficiently mastered the main content of the subject and shows *ignorance* of most of the educational material, makes gross errors in formulating definitions and concepts;

*is not able to* logically analyze and solve practical problems;

*does not have sufficient knowledge* of mathematical symbols and their correct application.